FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12515-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89630 Series

MB89635/T635/636/637/T637/P637/W637/PV630

■ DESCRIPTION

The MB89630 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- High-speed operating capability at low voltage
- Minimum execution time: 0.4 µs/3.5 V, 0.8 µs/2.7 V
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Five types of timers
  8-bit PWM timer: 2 channels (Also usable as a reload timer)
  8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
  16-bit timer/counter
  21-bit time-base timer
- UART
  CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  Activation by an external input capable

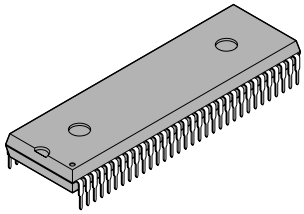
(Continued)

(Continued)

- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Bus interface function
  With hold and ready function

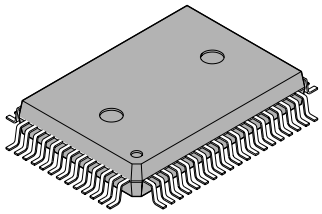
■ PACKAGE

64-pin Plastic SH-DIP



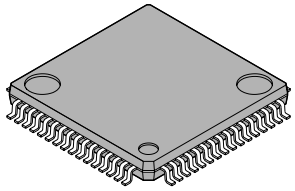
(DIP-64P-M01)

64-pin Plastic QFP



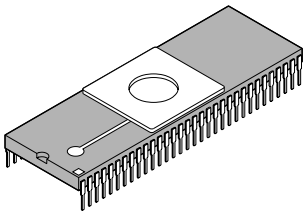
(FPT-64P-M06)

64-pin Plastic QFP



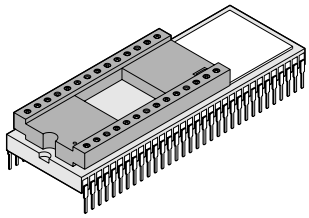
(FPT-64P-M09)

64-pin Ceramic SH-DIP



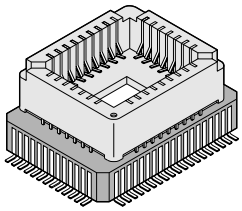
(DIP-64C-A06)

64-pin Ceramic MDIP



(MDP-64C-P02)

64-pin Ceramic MQFP



(MQP-64C-P01)

■ PRODUCT LINEUP

Parameter \ Part number	MB89635	MB89636	MB89637	MB89T635	MB89T637	MB89P637	MB89W637	MB89PV630
Classification	Mass production products (mask ROM products)			External ROM products		One-time PROM product	EPROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	Fixed to external ROM		32 K × 8 bits (Internal PROM, programming with general-purpose EPROM programmer)		32 K × 8 bits (external ROM)
RAM size	512 × 8 bits	768 × 8 bits	1024 × 8 bits	512 × 8 bits	1024 × 8 bits			
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 to 6.4 µs/10 MHz, 61 µs/32.768 kHz Interrupt processing time: 3.6 to 57.6 µs/10 MHz, 562.5 µs/32.768 kHz							
Ports	Input ports: 5 (All also serve as peripherals.) Output ports (N-ch open-drain): 8 (All also serve as peripherals.) I/O ports (N-ch open-drain): 4 (All also serve as peripherals.) Output ports (CMOS): 8 (All also serve as bus control.) I/O ports (CMOS): 28 (27 ports also serve as bus pins and peripherals.) Total: 53							
Clock timer	21 bits × 1 (in main clock)/15 bits × 1 (at 32.768 kHz)							
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 3.3 ms) × 2 channels 7/8-bit resolution PWM operation (conversion cycle: 51.2 µs to 839 ms) × 2 channels							
8-bit pulse width count timer	8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 µs) 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 µs) 8-bit pulse width measurement operation (continuous measurement capable, measurement of "H" pulse width/ "L" pulse width/ from ↑ to ↑/from ↓ to ↓ capable)							
16-bit timer/ counter	16-bit timer operation (operating clock cycle: 0.4 µs) 16-bit event counter operation (rising edge/falling edge/both edge selectability)							
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)							
UART	Switching two I/O systems by software capable Transfer data length (6, 7, and 8 bits) Transfer rate (300 to 62500 bps. at 10 MHz osciliation)							
10-bit A/D converter	10-bit resolution × 8 channels A/D conversion mode (conversion time: 13.2 µs) Sense mode (conversion time: 7.2 µs) Continuous activation by an external activation or an internal timer capable							

(Continued)

(Continued)

Part number / Parameter	MB89635	MB89636	MB89637	MB89T635	MB89T637	MB89P637	MB89W637	MB89PV630
External interrupt input	4 independent channels (edge selection, interrupt vector, source flag). Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)							
Standby mode	Sleep mode, stop mode, watch mode, and subclock mode							
Process	CMOS							
Operating voltage*1	2.2 V to 6.0 V			2.7 V to 6.0 V				
EPROM for use								MBM27C256A-20

*1: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
In the case of the MB89PV630, the voltage varies with the restrictions of the EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89635 MB89T635	MB89636 MB89637 MB89T637	MB89P637	MB89W637	MB89PV630
DIP-64P-M01	○	○	○	×	×
DIP-64C-A06	×	×	×	○	×
FPT-64P-M06	○	○	○	×	×
FPT-64P-M09	○	○	×*	×*	×*
MDP-64C-P02	×	×	×	×	○
MQP-64C-P01	×	×	×	×	○

○ : Available × : Not available

* : To convert pin pitches, an adapter socket (manufacturer: Sun Hayato Co., Ltd.) is available.
64SD-64QF2-8L: For conversion from (DIP-64P-M01, DIP-64C-A06, or MDP-64C-P02) to FPT-64P-M09
Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

On the MB89P637/W637, the program area starts from address 8007_H but on the MB89PV630 and MB89637 starts from 8000_H.

(On the MB89P637/W637, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637/W637.)

- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following points:

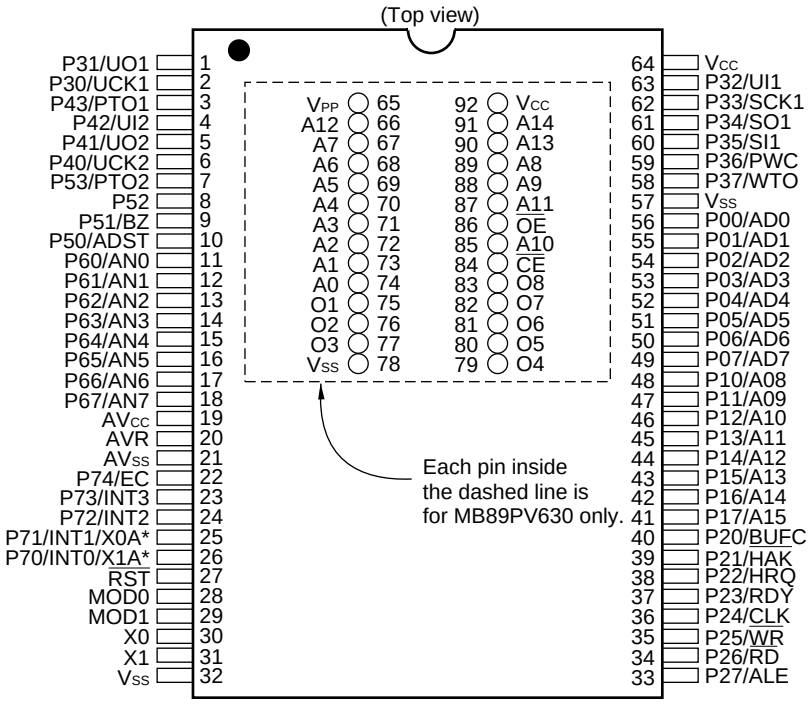
- A pull-up resistor cannot be set for P50 to P53 on the MB89P637 and MB89W637.
- Options are fixed on the MB89PV630, MB89T635, and MB89T637.

■ CORRESPONDENCE BETWEEN THE MB89630 AND MB89630R SERIES

- The MB89630R series is the reduction version of the MB89630 series. For their differences, refer to the MB89630R series data sheet.
- The the MB89630 and MB89630R series consist of the following products:

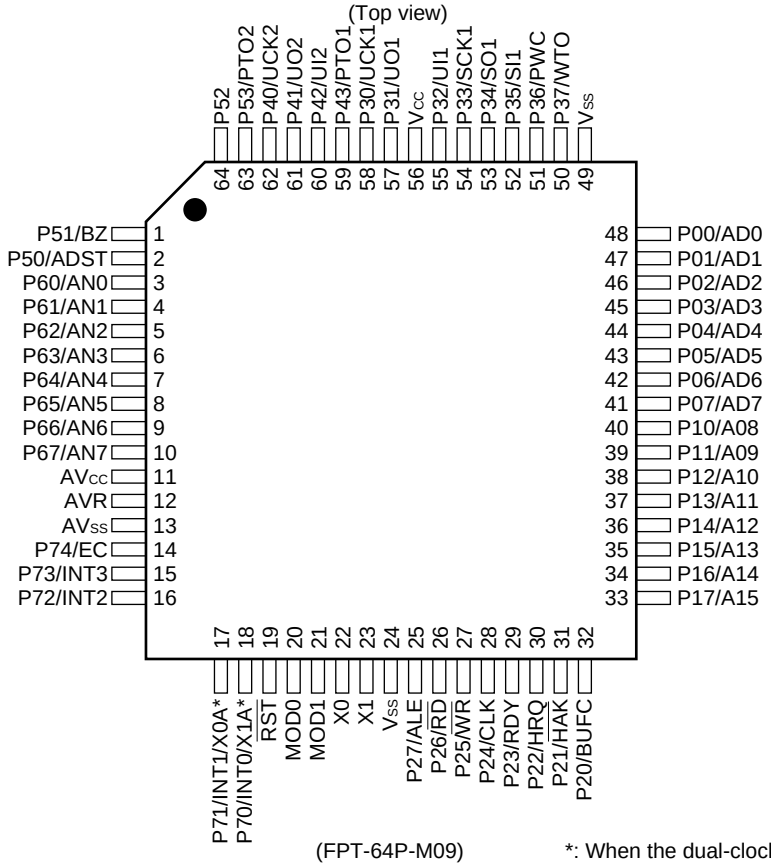
MB89630 series	MB89635	MB89T635	MB89636	MB89637	MB89P637	MB89W637	MB89PV630
MB89630R series	MB89635R	MB89T635R	MB89636R	MB89T637R			

■ PIN ASSIGNMENT



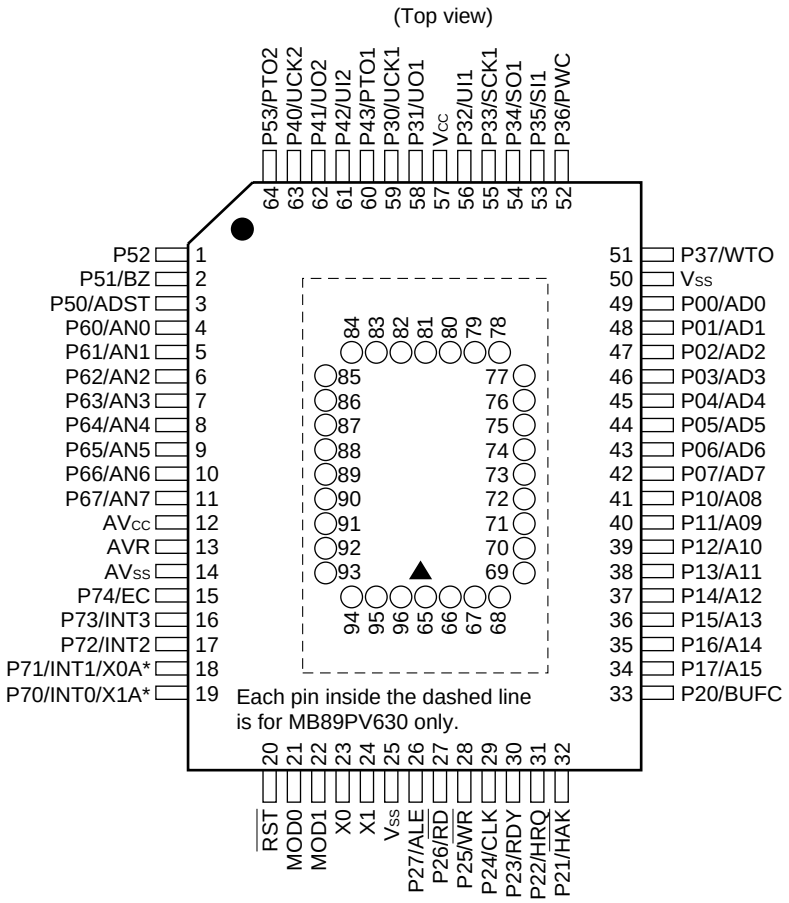
(DIP-64P-M01)
(DIP-64C-A06)
(MDP-64C-P02)

*: When the dual-clock system is selected.



(FPT-64P-M09)

*: When the dual-clock system is selected.



(FPT-64P-M06)
(MQP-64C-P01)

*: When the dual-clock system is selected.

- **Pin assignment on package top (MB89PV630 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
30	22	23	X0	A	Main clock crystal oscillator pins
31	23	24	X1		
28	20	21	MOD0	D	Operating mode selection pins Connect directly to V_{CC} or V_{SS}
29	21	22	MOD1		
27	19	20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
56 to 49	48 to 41	49 to 42	P00/AD0 to P07/AD7	F	General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O.
48 to 41	40 to 33	41 to 34	P10/A08 to P17/A157	F	General-purpose I/O ports When an external bus is used, these ports function as an upper address output.
40	32	33	P20/BUFC	H	General-purpose output-only port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	31	32	P21/$\overline{HAK}$	H	General-purpose output-only port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR.
38	30	31	P22/HRQ	F	General-purpose output-only port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	29	30	P23/RDY	F	General-purpose output-only port When an external bus is used, this port functions as a ready input.
36	28	29	P24/CLK	H	General-purpose output-only port When an external bus is used, this port functions as a clock output.
35	27	28	P25/$\overline{WR}$	H	General-purpose output-only port When an external bus is used, this port functions as a write signal output.
34	26	27	P26/$\overline{RD}$	H	General-purpose output-only port When an external bus is used, this port functions as a read signal output.

(Continued)

*1: DIP-64P-M01, DIP-64C-A06
*2: MDP-64C-P02
*3: FPT-64P-M09
*4: FPT-64P-M06
*5: MQP-M64C-P01

(Continued)

Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
33	25	26	P27/ALE	H	General-purpose output-only port When an external bus is used, this port functions as an address latch signal output.
2	58	59	P30/UCK1	G	General-purpose I/O port Also serves as the clock I/O 1 for the UART. This port is a hysteresis input type.
1	57	58	P31/UO1	F	General-purpose I/O port Also serves as the data output 1 for the UART.
63	55	56	P32/UI1	G	General-purpose I/O port Also serves as the data input 1 for the UART. This port is a hysteresis input type.
62	54	55	P33/SCK1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
61	53	54	P34/SO1	F	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O.
60	52	53	P35/SI1	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
59	51	52	P36/PWC	G	General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type.
58	50	51	P37/WTO	F	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter.
6	62	63	P40/UCK2	G	General-purpose I/O port Also serves as the clock I/O 2 for the UART. This port is a hysteresis input type.
5	61	62	P41/UO2	F	General-purpose I/O port Also serves as the data output 2 for the UART.
4	60	61	P42/UI2	G	General-purpose I/O port Also serves as the data input 2 for the UART. This port is a hysteresis input type.
3	59	60	P43/PTO1	F	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer.
10	2	3	P50/ADST	K	General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type.
9	1	2	P51/BZ	J	General-purpose I/O port Also serves as a buzzer output.

*1: DIP-64P-M01, DIP-64C-A06
*2: MDP-64C-P02
*3: FPT-64P-M09
*4: FPT-64P-M06
*5: MQP-M64C-P01

(Continued)

(Continued)

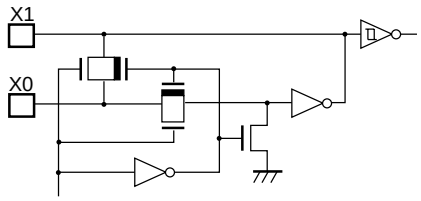
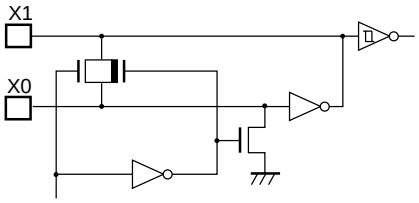
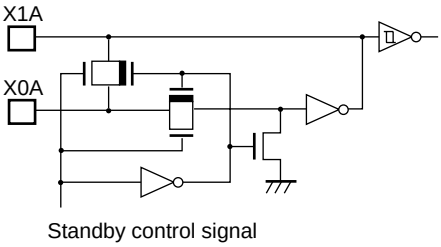
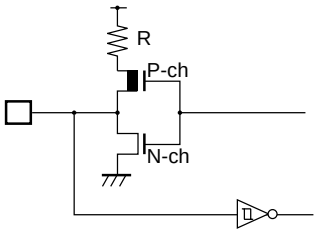
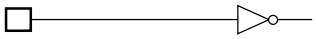
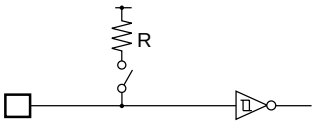
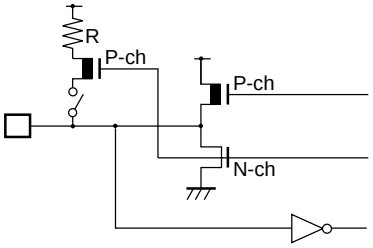
Pin no.			Pin name	Circuit type	Function
SH-DIP*1 MDIP*2	QFP2*3	QFP1*4 MQFP*5			
8	64	1	P52	J	General-purpose I/O port
7	63	64	P53/PTO2	J	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer.
11 to 18	3 to 10	4 to 11	P60/AN0 to P67/AN7	I	N-ch open-drain output-only ports Also serve as an A/D converter analog input.
26, 25	18, 17	19, 18	P70/INT0/X1A, P71/INT1/X0A	B/E	Input-only ports These ports are a hysteresis input type. Also serve as an external interrupt input (at single-clock operation). Subclock crystal oscillator pins (at dual-clock operation)
24, 23	16, 15	17, 16	P72/INT2, P73/INT3	E	Input-only ports Also serve as an external interrupt input. These ports are a hysteresis input type.
22	14	15	P74/EC	E	General-purpose input port Also serves as the external clock input for the 16-bit timer/counter. This port is a hysteresis input type.
64	56	57	V_{CC}	—	Power supply pin
32, 57	24,49	25, 50	V_{SS}	—	Power supply (GND) pin
19	11	12	AV_{CC}	—	A/D converter power supply pin
20	12	13	AVR	—	A/D converter reference voltage input pin
21	13	14	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.

*1: DIP-64P-M01, DIP-64C-A06
*2: MDP-64C-P02
*3: FPT-64P-M09
*4: FPT-64P-M06
*5: MQP-M64C-P01

- **External EPROM pins (MB89PV630 only)**

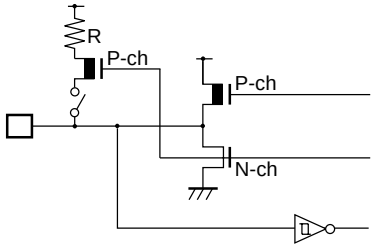
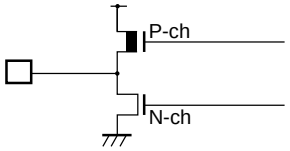
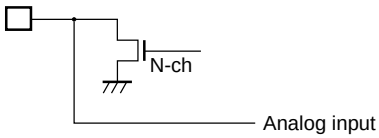
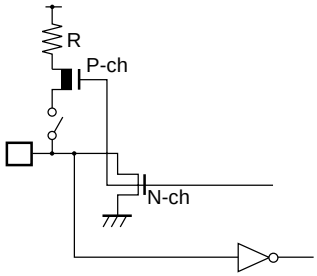
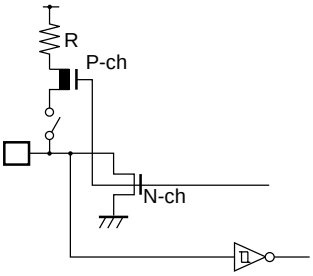
Pin no.		Pin name	I/O	Function
MDIP	MQFP			
65	66	V_{PP}	O	"H" level output pin
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
84	87	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
85	88	A10	O	Address output pin
86	89	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) External clock input selection versions of MB89PV630, MB89P637, MB89W637, MB89635, MB89T635, MB89636, MB89637, and MB89T637 At an oscillation feedback resistor of approximately 1 MΩ/5 V
		• Crystal or ceramic oscillation type (main clock) Oscillation selection versions of MB89PV630, MB89P637, MB89W637, MB89635, MB89T635, MB89636, MB89637, and MB89T637 At an oscillation feedback resistor of approximately 1 MΩ/5 V
B		• Crystal or ceramic oscillation type (subclock) MB89PV630, MB89P637, MB89W637, MB89635, MB89636, and MB89637 with dual-clock system At an oscillation feedback resistor of approximately 4.5 MΩ/5 V
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5 V • Hysteresis input
D		
E		• Hysteresis input • Pull-up resistor optional (except P70 and P71)
F		• CMOS output • CMOS input • Pull-up resistor optional (except P22 and P23)

(Continued)

(Continued)

Type	Circuit	Remarks
G		• CMOS output • Hysteresis input • Pull-up resistor optional
H		• CMOS output
I		• Analog input
J		• CMOS input • Pull-up resistor optional
K		• Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (option selection) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P637

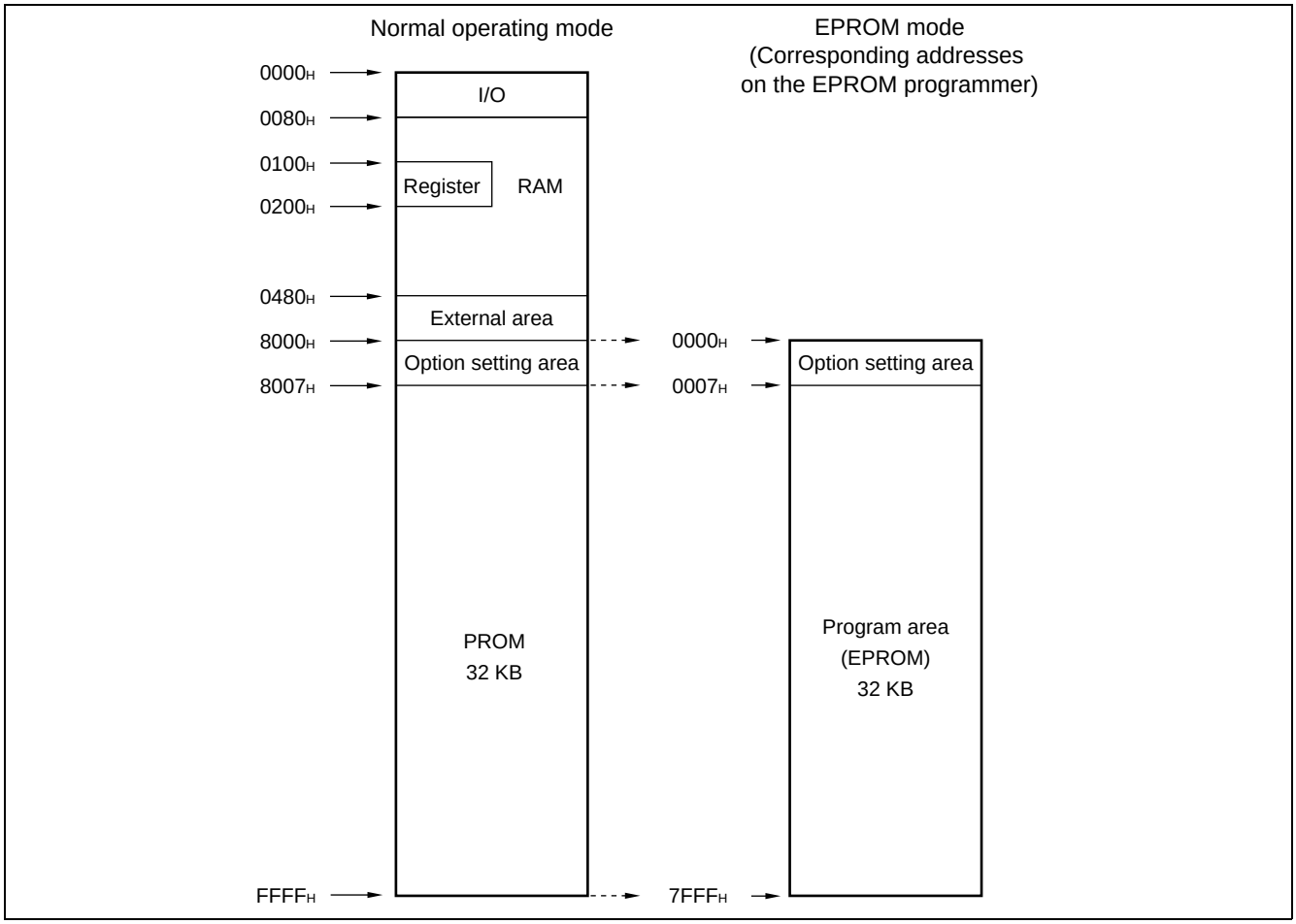
The MB89P637 is an OTPROM version of the MB89630 series.

1. Features

- 32-Kbytes PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode is illustrated below.



3. Programming to the EPPROM

In EPROM mode, the MB89P637 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter.

However, the electronic signature mode cannot be used.

When the operating ROM area for a single chip is 32 Kbytes (8007_H to $FFFF_H$) the EPROM can be programmed as follows:

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

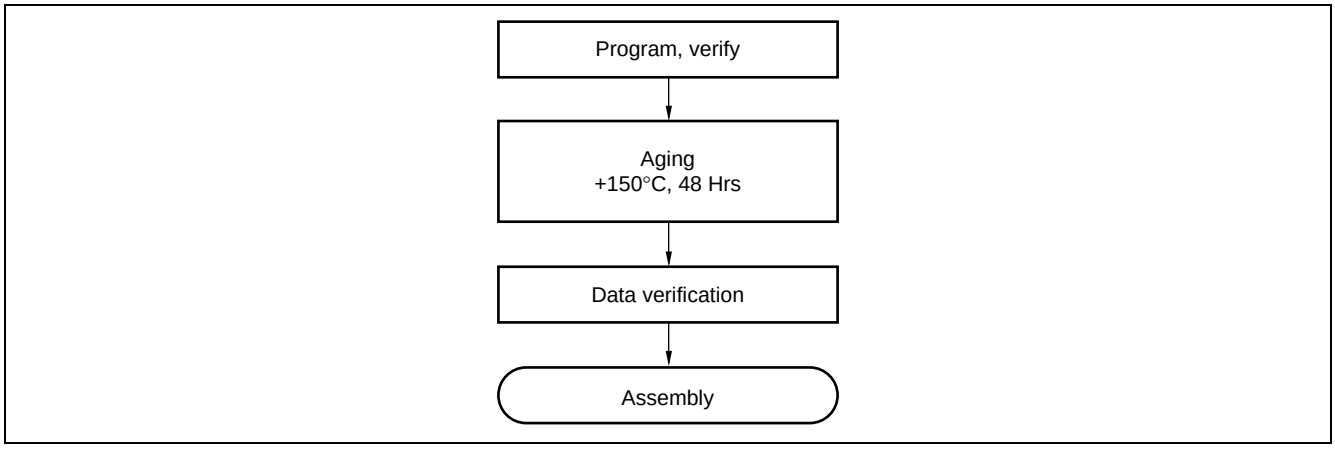
(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$.
(Note that addresses 8000_H to $FFFF_H$ in the operating mode assign to 0000_H to $7FFF_H$ in EPROM mode).

(3) Load option data into addresses 0000_H to 0006_H of the EPROM programmer.
(For information about each corresponding option, see “8. OTPROM Option Bit Map.”).

(4) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm^2 is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 μW/cm^2 for 15 to 21 minutes. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure time will be much longer than with UV source at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

7. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
DIP-64C-M01	ROM-64SD-28DP-8L
FPT-64P-M06	ROM-64QF-28DP-8L
FPT-64P-M09	ROM-64QF2-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

8. OTPROM Option Bit Map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single/dual-clock system 1: Dual clock 0: Single clock	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization (F/CH) $11:2^{18}$ $10:2^{14}$	 $01:2^{17}$ $00:2^{4}$
0001_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0003_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0004_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0005_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	Vacancy Readable and writable	Vacancy Readable and writable
0006_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Reserved bit Readable and writable

Notes:
- Set each bit to 1 to erase.
- Do not write 0 to the blank bit.
  The read value of the vacant bit is 1, unless 0 is written to it.
- Always write 1 to the reserved bit.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV, MBM27C256A-20CZ

2. Programming Socket Adapter

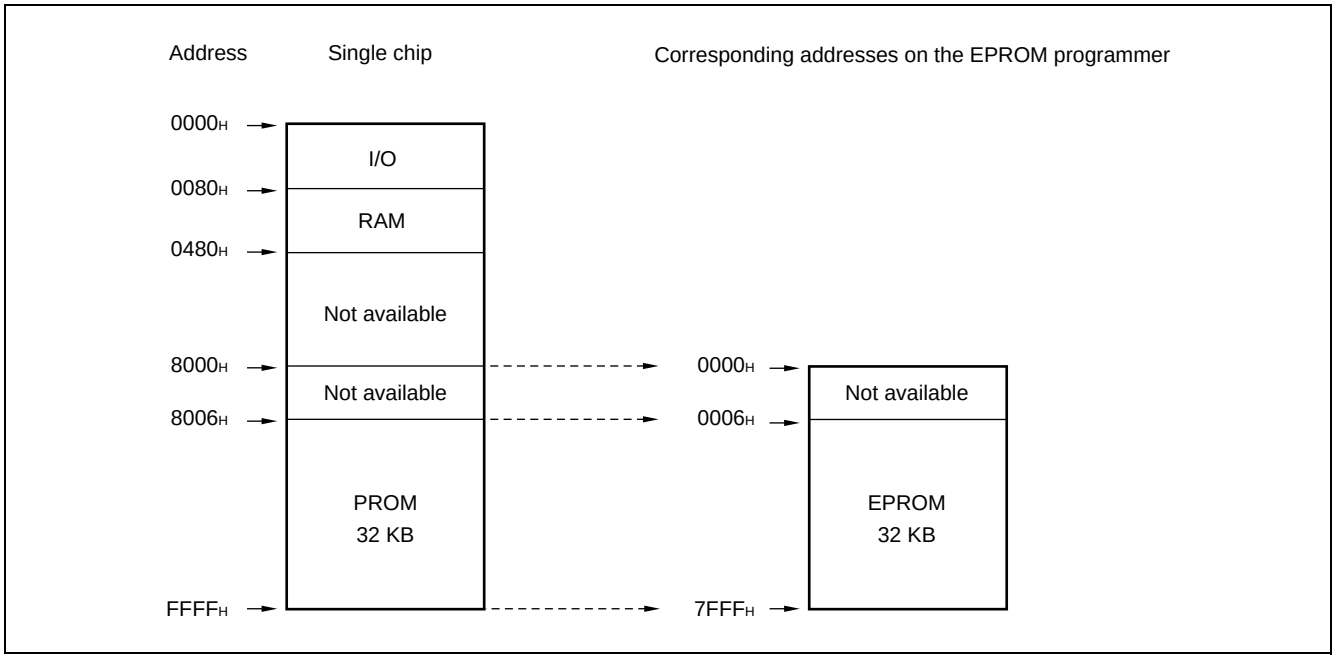
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



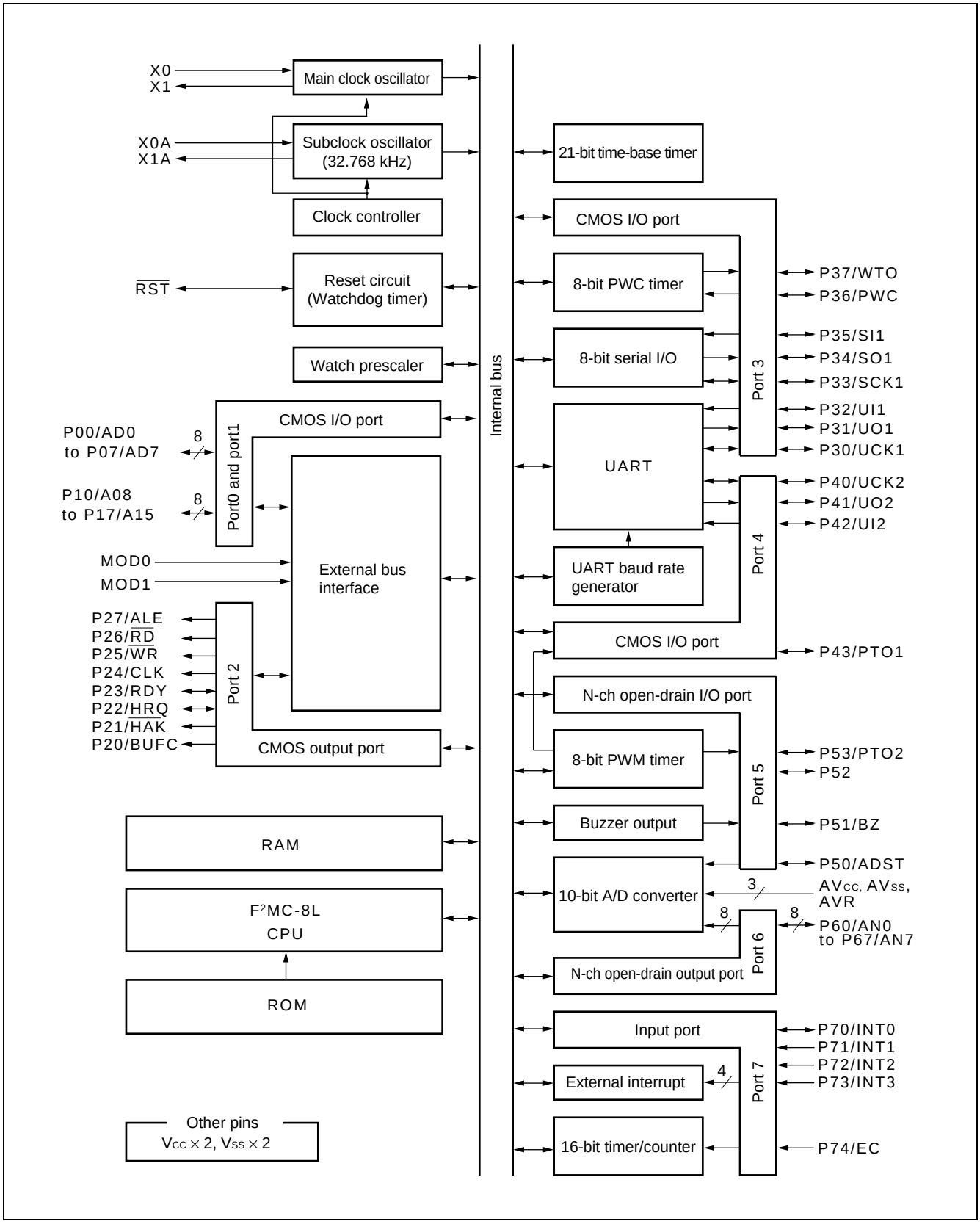
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0006_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

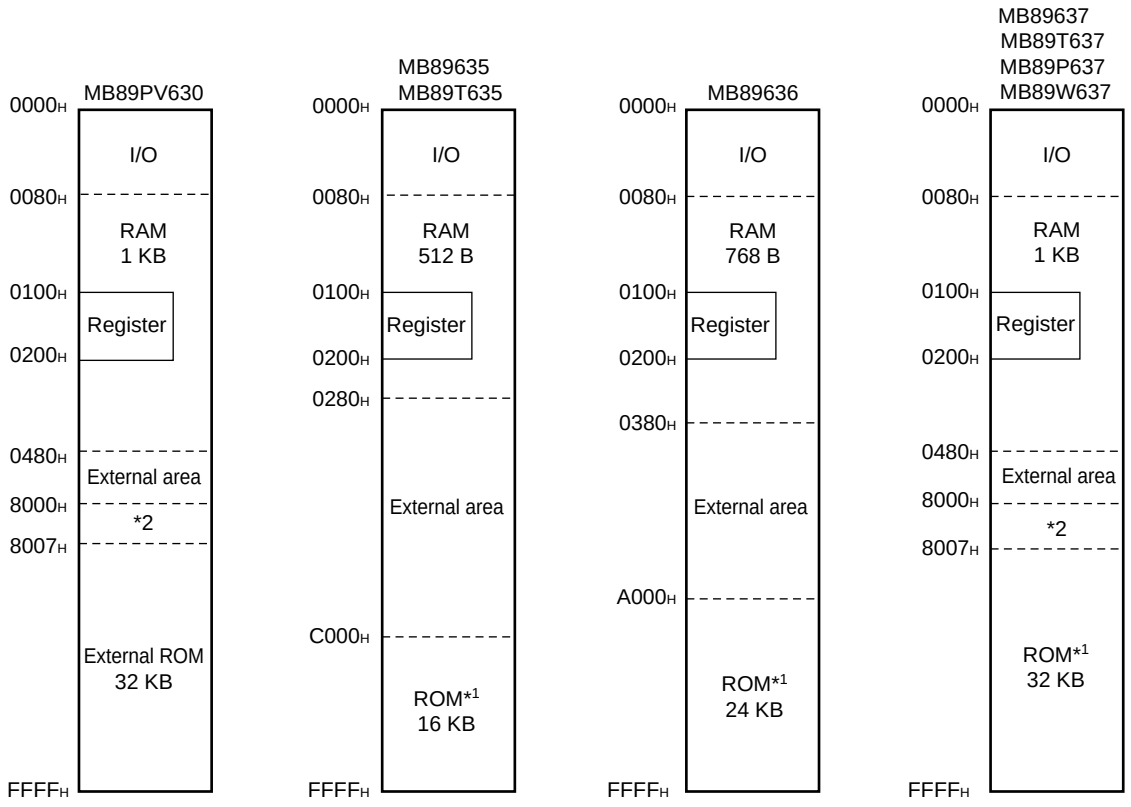


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89630 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89630 series is structured as illustrated below.

Memory Space



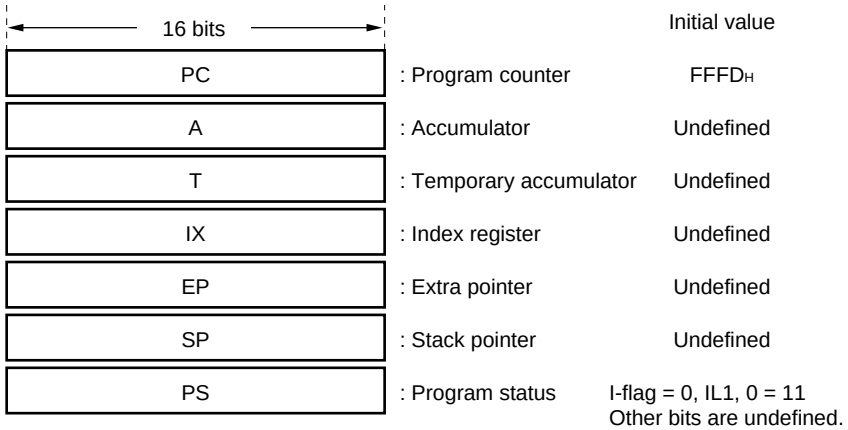
*1: The ROM area is an external area depending on the mode.
The internal ROM cannot be used on the MB89T635 and MB89T637.

*2: Addresses 8000H to 8006H for the MB89P637 and MB89W637 comprise an option area, do not use this area for the MB89PV630 and MB89637.

2. Registers

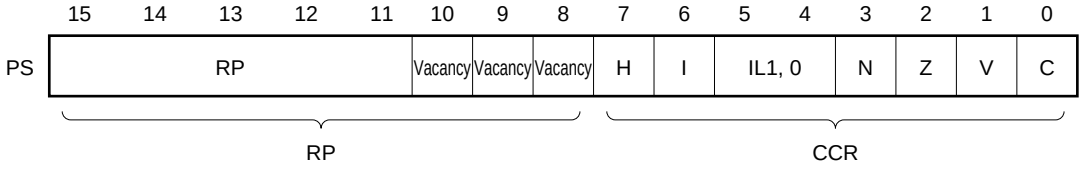
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A16-bit register for index modification
Extra pointer (EP):	A16-bit pointer for indicating a memory address
Stack pointer (SP):	A16-bit register for indicating a stack area
Program status (PS):	A16-bit register for storing a register pointer, a condition code



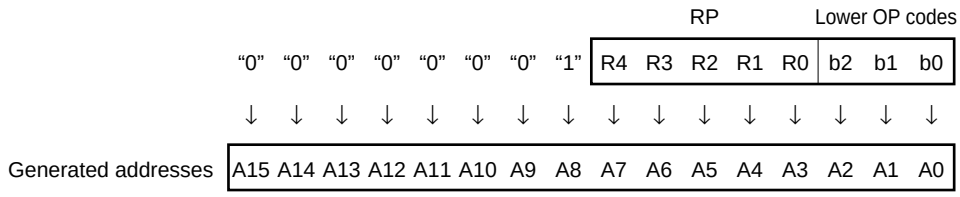
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

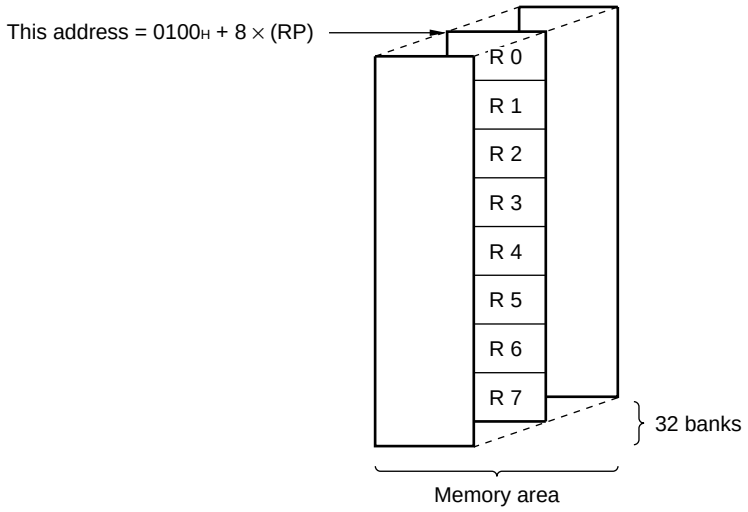
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89653A (RAM 512 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuraiton



■ I/O MAP

Address	Read/ write	Register name	Register description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	(R/W)	PDR0	Port 0 data register	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
01H	(W)	DDR0	Port 0 data direction register	DD07	DD06	DD05	DD04	DD03	DD02	DD01	DD00
02H	(R/W)	PDR1	Port 1 data register	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10
03H	(W)	DDR1	Port 1 data direction register	DD17	DD16	DD15	DD14	DD13	DD12	DD11	DD10
04H	(R/W)	PDR2	Port 2 data register	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20
05H	(W)	BCTR	External bus pin control register	—	—	—	—	—	—	HLD	BUF
06H	Vacancy										
07H	(R/W)	SYCC	System clock control register	SMC	—	—	WT1	WT0	SCS	CS1	CS0
08H	(R/W)	STBC	System clock control register	STP	SLP	SPL	RST	TMD	—	—	—
09H	(R/W)	WDTE	Watchdog timer control register	CS	—	—	—	WTE3	WTE2	WTE1	WTE0
0AH	(R/W)	TBCR	Time-base timer control register	TBOF	TBIE	—	—	—	TBC1	TBC0	TBR
0BH	(R/W)	WPCR	Watch prescaler control register	WIF	WIE	—	—	—	WS1	WS0	WCLR
0CH	(R/W)	CHG3	Port 3 switching register	—	—	CG35	CG34	CG33	—	—	—
0DH	(R/W)	PDR3	Port 3 data register	PD37	PD36	PD35	PD34	PD33	PD32	PD31	PD30
0EH	(W)	DDR3	Port 3 data direction register	DD37	DD36	DD35	DD34	DD33	DD32	DD31	DD30
0FH	(R/W)	PDR4	Port 4 data register	—	—	—	—	PD43	PD42	PD41	PD40
10H	(W)	DDR4	Port 4 data direction register	—	—	—	—	DD43	DD42	DD41	DD40
11H	(R/W)	BUZR	Buzzer register	—	—	—	—	—	—	BUZ1	BUZ0
12H	(R/W)	PDR5	Port 5 data register	—	—	—	—	PD53	PD52	PD51	PD50
13H	(R/W)	PDR6	Port 6 data register	PD67	PD66	PD65	PD64	PD63	PD62	PD61	PD60
14H	(R)	PDR7	Port 7 data register	—	—	—	PD74	PD73	PD72	PD71	PD70
15H	(R/W)	PCR1	PWC pulse width control register 1	EN	TOE	IE	—	—	UF	IR	BF
16H	(R/W)	PCR2	PWC pulse width control register 2	FC	RM	TO	—	C1	C0	W1	W0
17H	(R/W)	RLBR	PWC reload buffer register	RLB7	RLB6	RLB5	RLB4	RLB3	RLB2	RLB1	RLB0
18H	(R/W)	TMCR	16-bit timer control register	—	—	TCR	TCS1	TCS0	TCEF	TCIE	TCS
19H	(R/W)	TCHR	16-bit timer count register (H)	TC15	TC14	TC13	TC12	TC11	TC10	TC09	TC08
1AH	(R/W))	TCLR	16-bit timer count register (L)	TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00
1BH	Vacancy										
1CH	(R/W)	SMR1	Serial mode register	SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST
1DH	(R/W)	SDR1	Serial data register	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00
1EH	Vacancy										
1FH	Vacancy										

(Continued)

(Continued)

Address	Read/ write	Register name	Register description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20H	(R/W)	ADC1	A/D converter control register 1	ANS3	ANS2	ANS1	ANS0	ADI	ADMV	SIFM	AD
21H	(R/W)	ADC2	A/D converter control register 2	—	TIM1	TIM0	ADCK	ADIE	ADMD	EXT	TEST
22H	(R/W)	ADDH	A/D converter data register (H)	—	—	—	—	—	—	ADD9	ADD8
23H	(R/W)	ADDL	A/D converter data register (L)	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
24H	(R/W)	EIC1	External interrupt control register 1	EIR1		SEL1	EIE1	EIR0	INTE	SEL0	EIE0
25H	(R/W)	EIC2	External interrupt control register 2	EIR3	—	SEL3	EIE3	EIR2	—	SEL2	EIE2
26H	Vacancy										
27H	Vacancy										
28H	(R/W)	CNTR1	PWM timer control register 1	PTX1	PTX2	P7M1	P7M2	SC11	SC10	SC21	SC20
29H	(R/W)	CNTR2	PWM timer control register 2	TPE1	TPE2	CK12	—	TIR1	TIR2	TIE1	TIE2
2AH	(R/W)	CNTR3	PWM timer control register 3	—	OE2	OE3	CH12	—	—	—	—
2BH	(W)	COMR1	PWM timer compare register 1	CM17	CM16	CM15	CM14	CM13	CM12	CM11	CM10
2CH	(W)	COMR2	PWM timer compare register 2	CM27	CM26	CM25	CM24	CM23	CM22	CM21	CM20
2DH	(R/W)	SMC	UART serial mode control register	PEN	SBL	MC1	MC0	SMDE	—	UCKE	UOE
2EH	(R/W)	SRC	UART serial rate control register	—	—	CR	SCS1	SCS0	RC2	RC1	RC0
2FH	(R/W)	SSD	UART serial status and data register	RDRF	ORFE	TDRE	TIE	RIE	PSEL	TD8/ TP	RD8/ RP
30H	(R) (W)	SIDR SODR	UART serial input data register UART serial output data register	SID7 SOD7	SID6 SOD6	SID5 SOD5	SID4 SOD4	SID3 SOD3	SID2 SOD2	SID1 SOD1	SID0 SOD0
31H to 7BH	Vacancy										
7CH	(W)	ILR1	Interrupt level setting register 1	L31	L30	L21	L20	L11	L10	L01	L00
7DH	(W)	ILR2	Interrupt level settingregister 2	L71	L70	L61	L60	L51	L50	L41	L40
7EH	(W)	ILR3	Interrupt level setting register 3	LB1	LB0	LA1	LA0	L91	L90	L81	L80
7FH	Vacancy										

Notes: • Do not use vacancies.
• — represents a vacant bit.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed AV_{CC} + 0.3.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P50 to P53
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P50 to P53
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P50 to P53
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P50 to P53
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89635/637
		2.7*	6.0*	V	Normal operation assurance range* MB89PV630/P637/ W637/T635/T637
	AV_{CC}	1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	3.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and “5. A/D Converter Electrical Characteristics.”

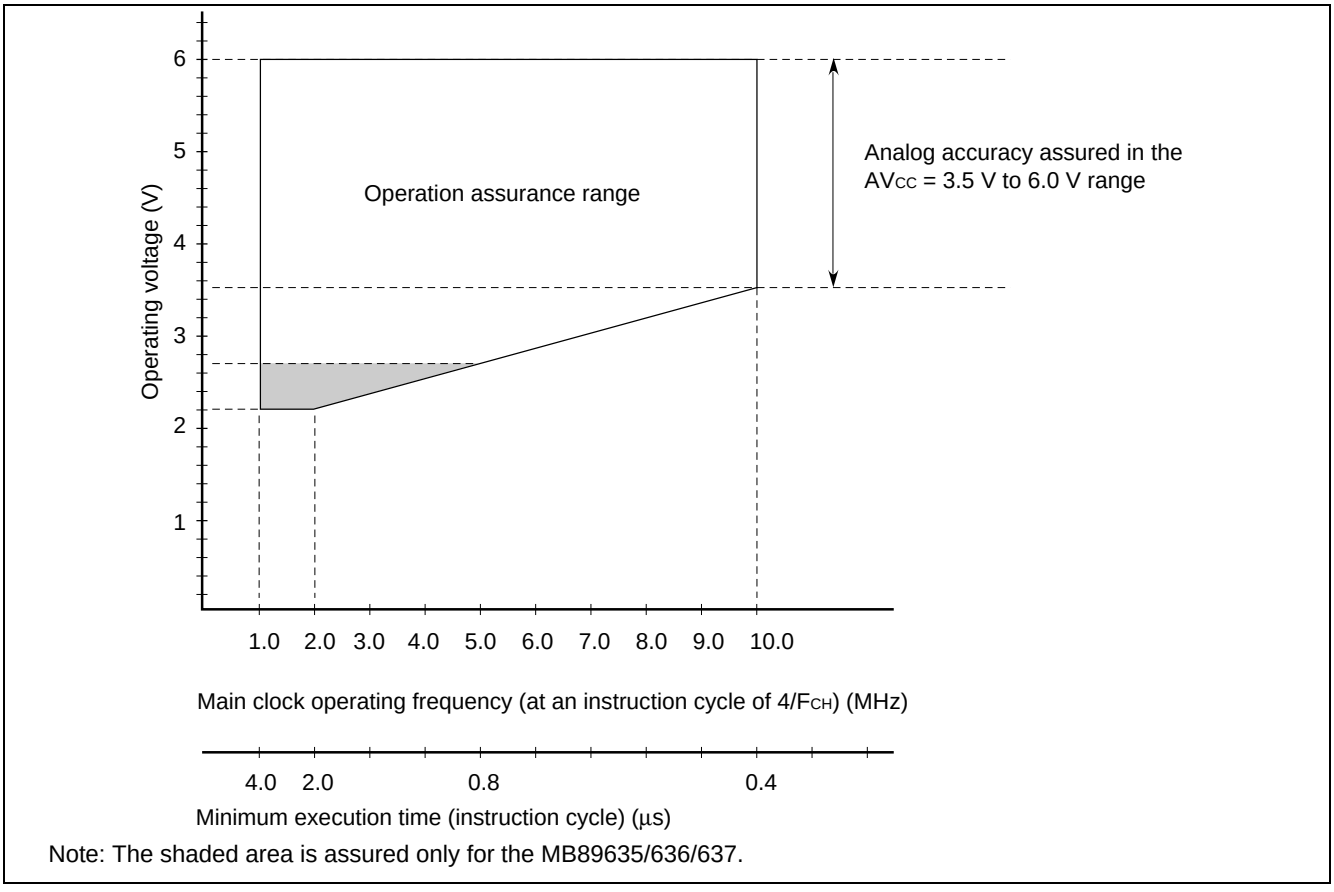


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_{CH}.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH1}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P51 to P53 with pull-up resistor
	V_{IH2}	P51 to P53		0.7 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42,P50, P72 to P74		0.8 V_{CC}	—	V_{CC} + 0.3	V	P50 with pull-up resistor
	V_{IHS2}	P50, P70, P71		0.8 V_{CC}	—	V_{SS} + 6.0	V	Without pull-up resistor
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P30, P32, P33, P35, P36, P40, P42, P50 to P53, P70 to P74, $\overline{RST}$, MOD0, MOD1		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P50 to P53		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27 P30 to P37, P40 to P43, P50 to P53, P60 to P67, RST	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1.0	2	mA	MB89635/T635/636/637/T637/PV630
				—	1.5	2.5	mA	MB89P637/W637
	I_{CCS1}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_{CH} = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	0.5	1.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock mode	—	50	100	µA	MB89635/T635/636/637/T637/PV630
				—	500	700	µA	MB89P637/W637
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual-clock system	—	3	15	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode at single-clock system	—	—	1	µA	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_A	AV_{CC}	F_{CH} = 10 MHz, when A/D conversion is activated	—	6	—	mA	
	I_{AH}		F_{CH} = 10 MHz, T_A = +25°C, when A/D conversion is stopped	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not included.

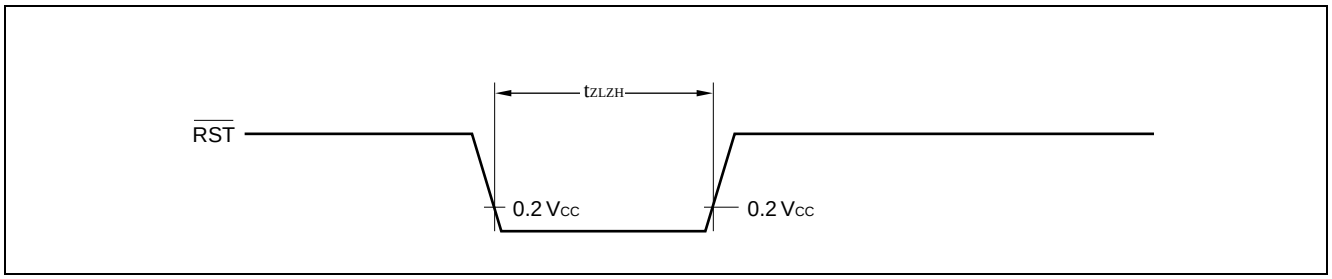
*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ “L” pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

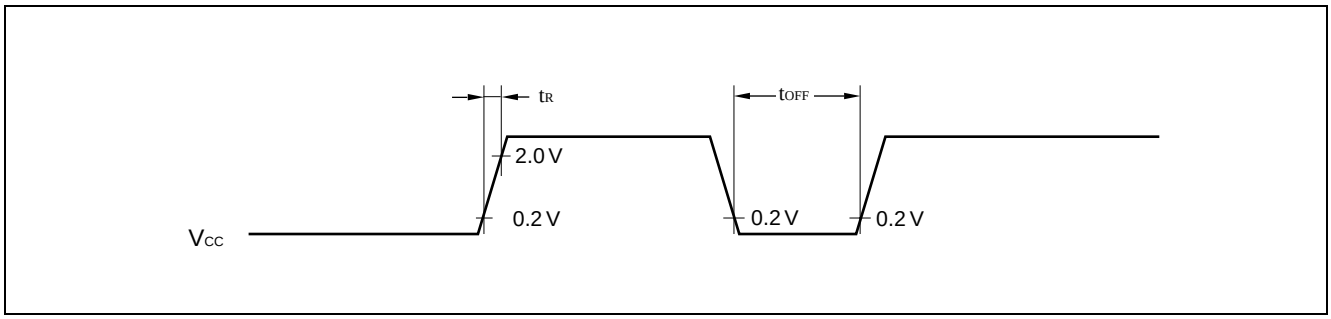


(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

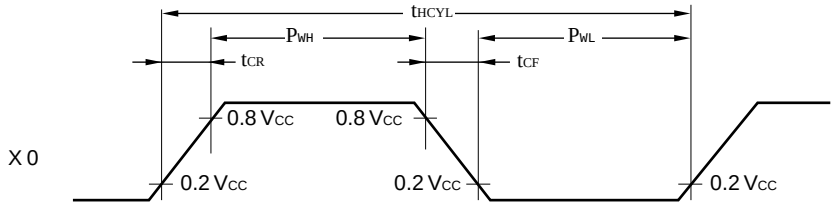


(3) Clock Timing

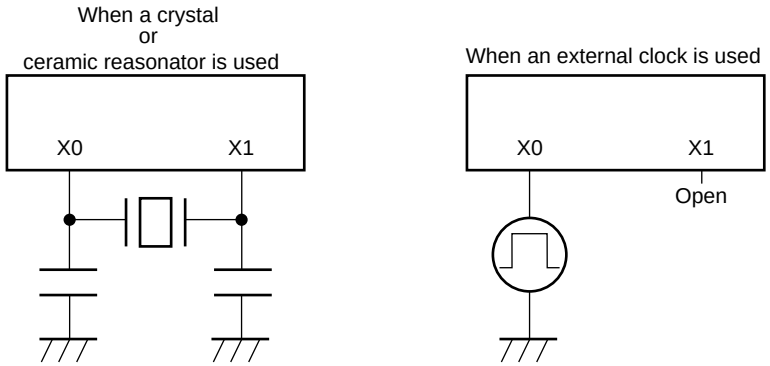
($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

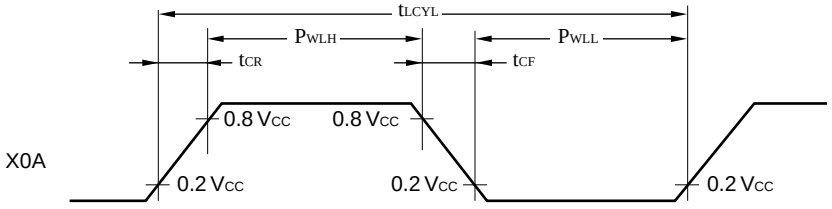
X0 and X1 Timing and Conditions



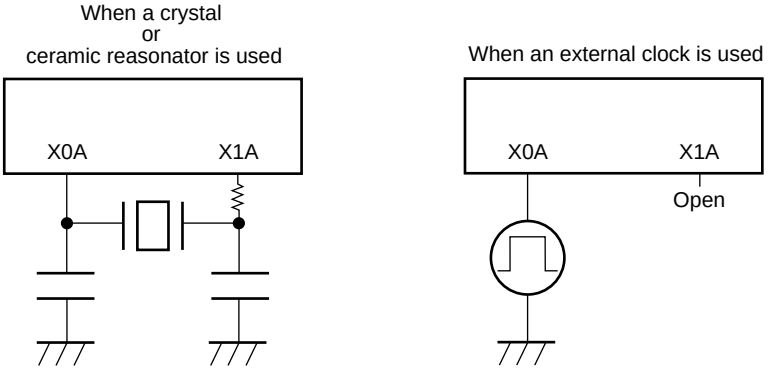
Main Clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 0.4 µs when operating at F_{CH} = 10 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

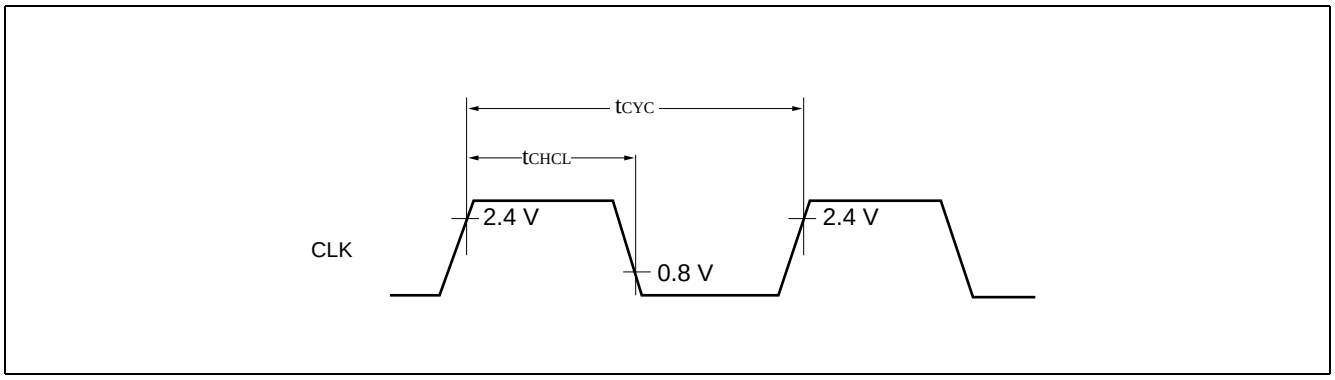
Note: When operating at 10 MHz, the cycle varies with the set execution time.

(5) Clock Output Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock time	t_{CYC}	CLK	—	1/2 t_{inst}*	—	µs	
CLK ↑ → CLK ↓	t_{CHCL}	CLK		1/4 t_{inst}* – 70 ns	1/4 t_{inst}*	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

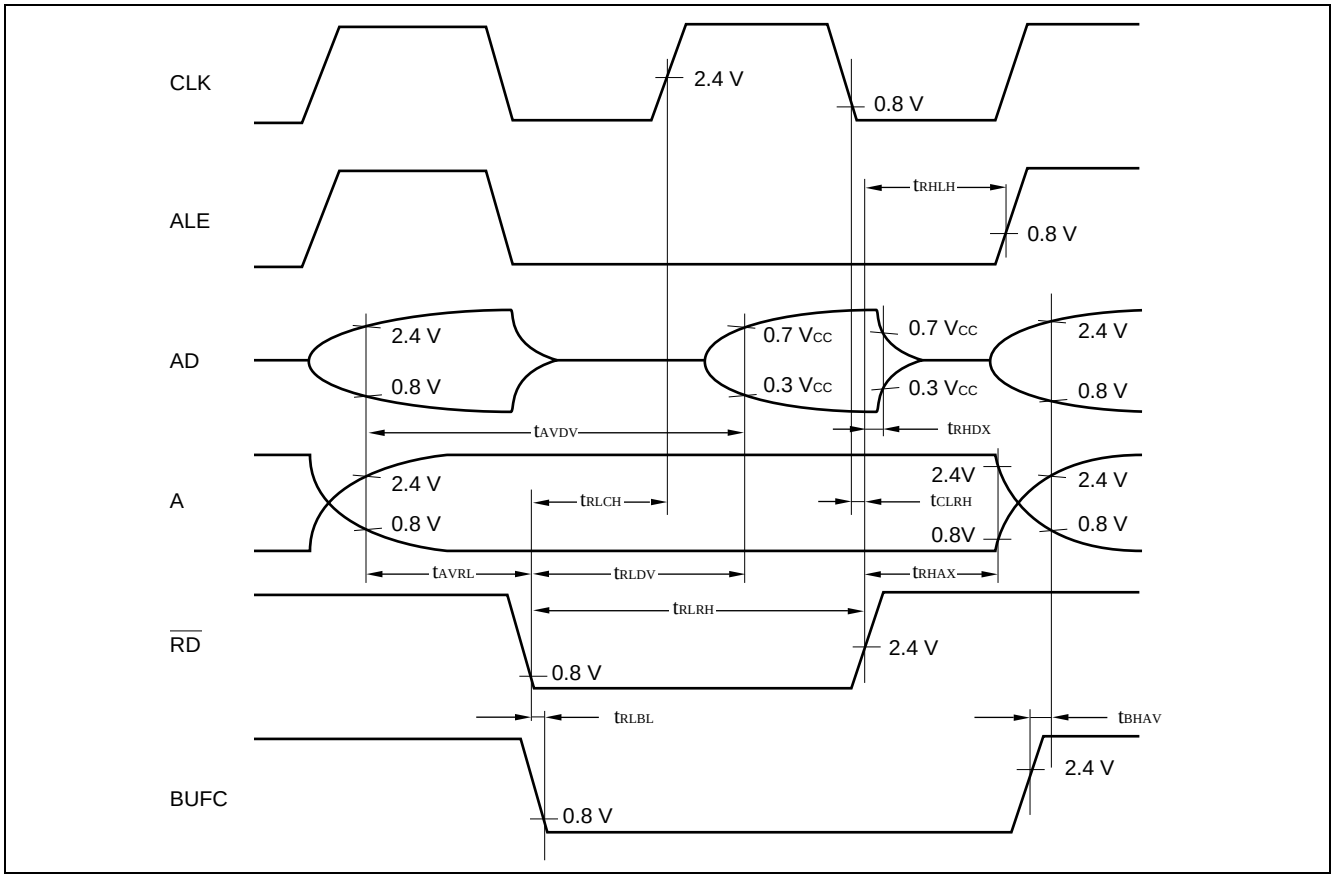


(6) Bus Read Timing

(V_{CC} = +5.0 V±10%, 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to 08, AD7 to 0	—	1/4 t_{inst}*– 64 ns	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst}*– 20 ns	—	µs	
Valid address → data read time	t_{AVDV}	AD7 to 0, A15 to 08		1/2 t_{inst}*	200	µs	No wait
$\overline{RD}$ ↓ → data read time	t_{RLDV}	$\overline{RD}$, AD7 to 0		1/2 t_{inst}*– 80 ns	120	µs	No wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to 0, $\overline{RD}$		0	—	µs	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}*– 40 ns	—	µs	
$\overline{RD}$ ↑ → address loss time	t_{RHAX}	$\overline{RD}$, A15 to 08		1/4 t_{inst}*– 40 ns	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}*– 40 ns	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}			0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	ns	
BUFC ↑ → valid address time	t_{BHAV}	A15 to 08, AD7 to 0, BUFC		5	—	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



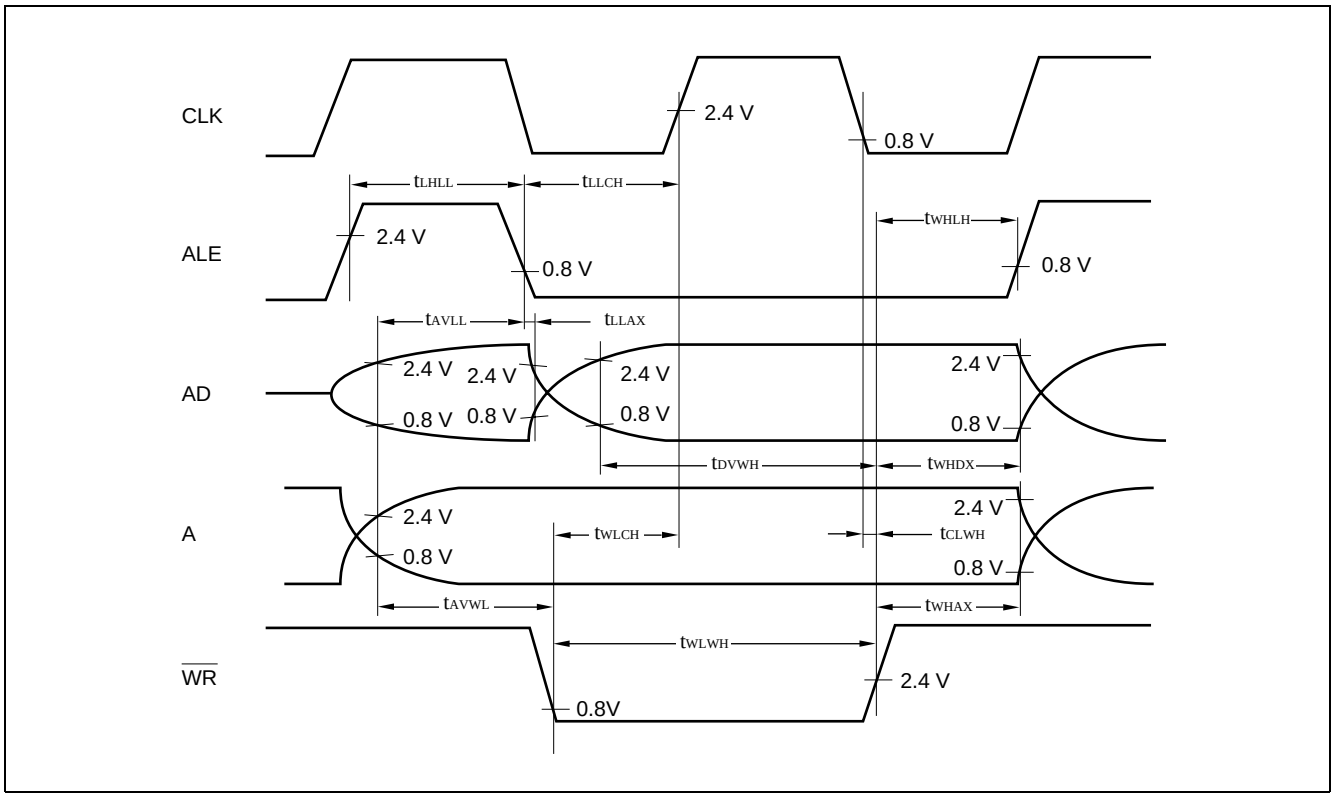
(7) Bus Write Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to 0, ALE A15 to 08	—	1/4 t_{inst}*1 – 64 ns	—	µs	
ALE ↓ time → address loss time	t_{LLAX}	AD7 to 0, ALE A15 to 08		5	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 60 ns	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*1 – 20 ns	—	µs	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to 0, WR		1/2 t_{inst}*1 – 60 ns	—	µs	
$\overline{WR}$ ↑ → address loss time	t_{WHAX}	$\overline{WR}$, A15 to 08		1/4 t_{inst}*1 – 40 ns	—	µs	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to 0, WR		1/4 t_{inst}*1 – 40 ns	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 40 ns	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*1 – 40 ns	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}			0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*1 – 35 ns	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE,CLK		1/4 t_{inst}*1 – 30 ns	—	µs	

*1: For information on t_{inst}, see “(4) Instruction Cycle.”

*2: This characteristics are also applicable to the bus read timing.

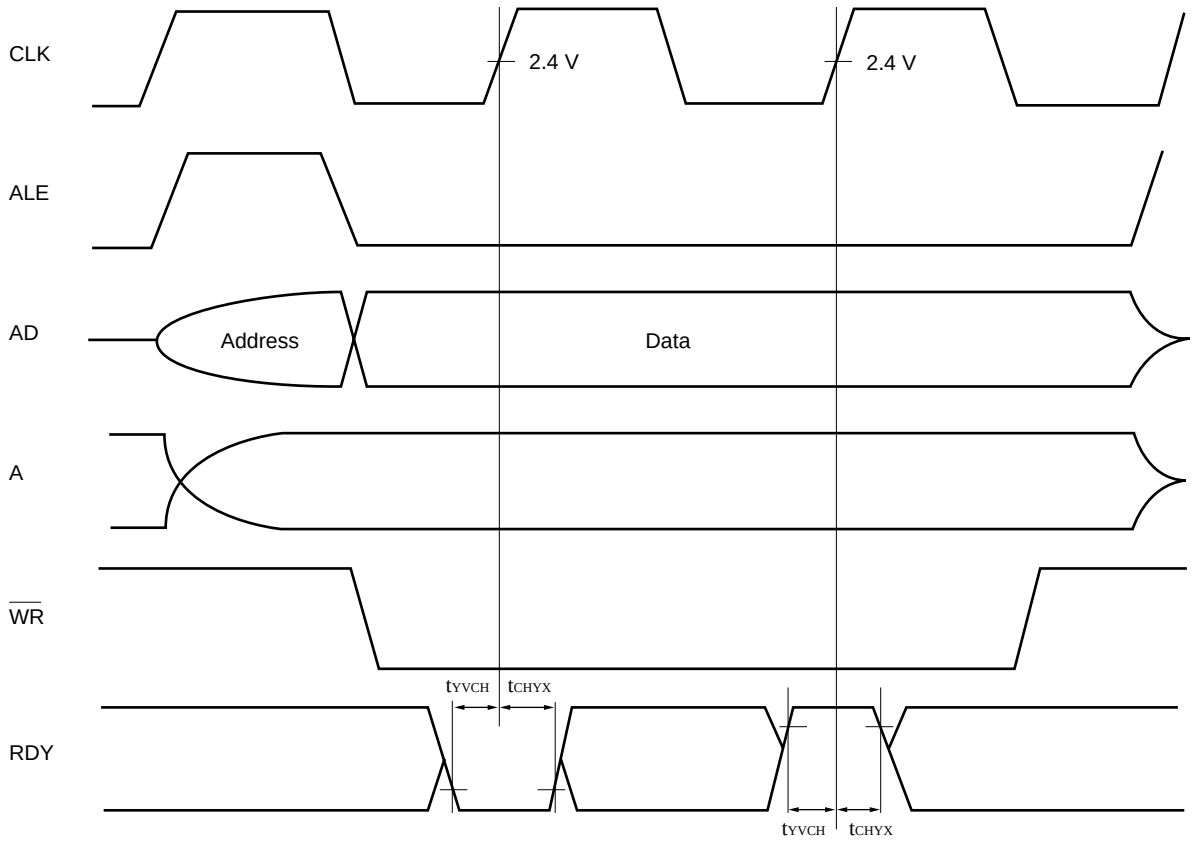


(8) Ready Input Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY loss time	t_{CHYX}			0	—	ns	*

* : This characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

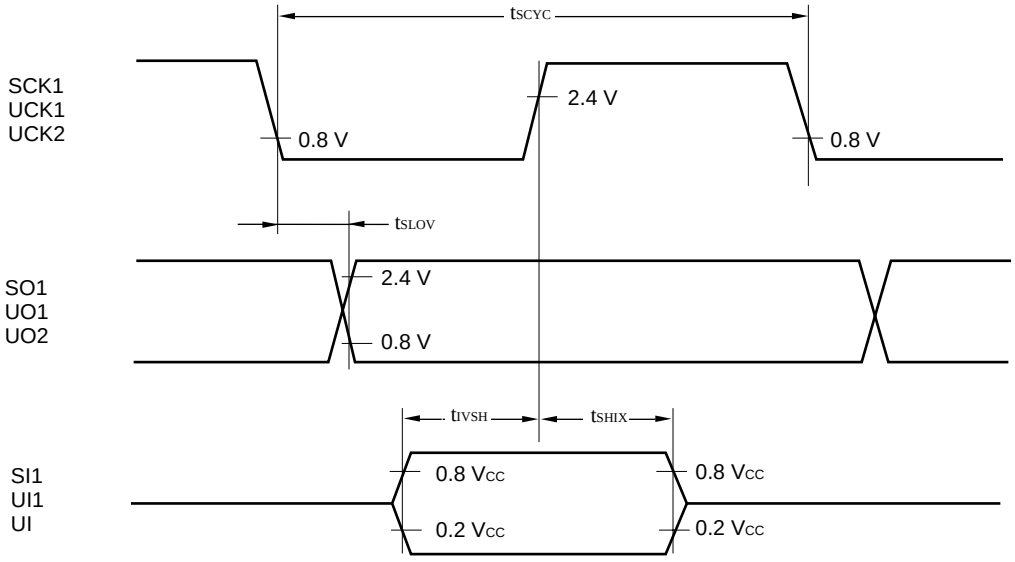
(9) Serial I/O Timing

(V_{CC} = +5.0 V±10%, F_{CH} = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

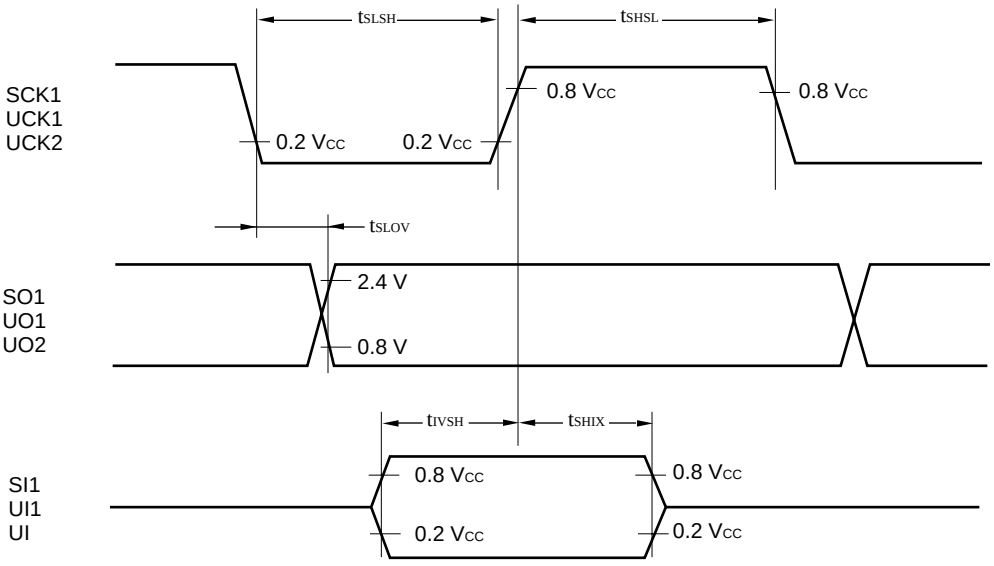
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, UCK1, UCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time UCK1 ↑ → valid UI1 hold time UCK2 ↑ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, UCK1, UCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, UCK1, UCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time UCK1 ↓ → UO1 time UCK2 ↓ → UO2 time	t_{SLOV}	SCK1, SO1 UCK1, UO1 UCK2, UO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid UI1 → UCK1 ↑ Valid UI2 → UCK2 ↑	t_{IVSH}	SI1, SCK1 UI1, UCK1 UI2, UCK2		1/2 t_{inst}*	—	µs	
SCK1 ↓ → valid SI1 hold time UCK1 ↓ → valid UI1 hold time UCK2 ↓ → valid UI2 hold time	t_{SHIX}	SCK1, SI1 UCK1, UI1 UCK2, UI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

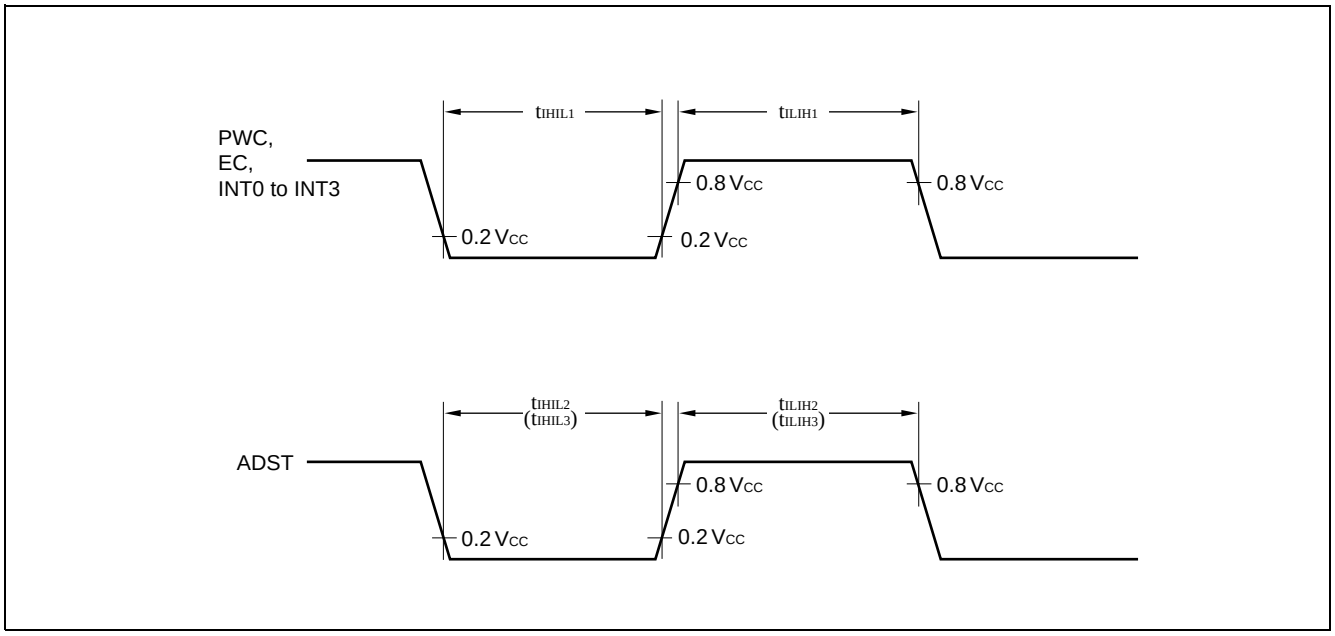


(10) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	PWC, INT0 to INT3,EC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	ADST	2^8 t_{inst}*	—	µs	A/D mode
Peripheral input “L” pulse width 2	t_{IHIL2}		2^8 t_{inst}*	—	µs	A/D mode
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	2^8 tin_{st}*	—	µs	Sense mode
Peripheral input “L” pulse width 3	t_{IHIL3}		2^8 t_{inst}*	—	µs	Sense mode

* : For information on t_{inst}, see “(4) Instruction Cycle.”



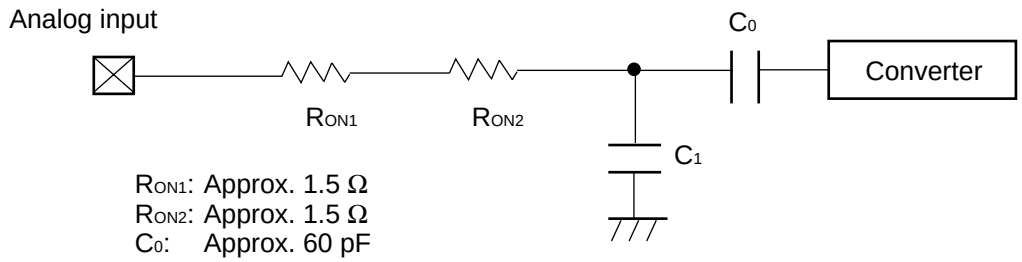
5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC}$ = 3.5 V to 6.0 V, F_{CH} = 10 MHz, $AV_{SS} = V_{SS}$ = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	At $AV_{CC} = V_{CC}$
Linearity error			—	—	±2.0	LSB	
Differential linearity error			—	—	±1.5	LSB	
Total error			—	—	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	
Interchannel disparity	—	—	—	—	4	LSB	
A/D mode conversion time			—	13.2	—	µs	At 10 MHz oscillation
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	—		0.0	—	AVR	V	
Reference voltage		AVR	0.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		—	200	—	µA	AVR = 5.0 V

Precautions:
- The smaller the | AVR–AV_{SS} |, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions:
  Output impedance of the external circuit < Approx. 10 kΩ
  If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10MHz oscillation.)

Analog Input Circuit Model

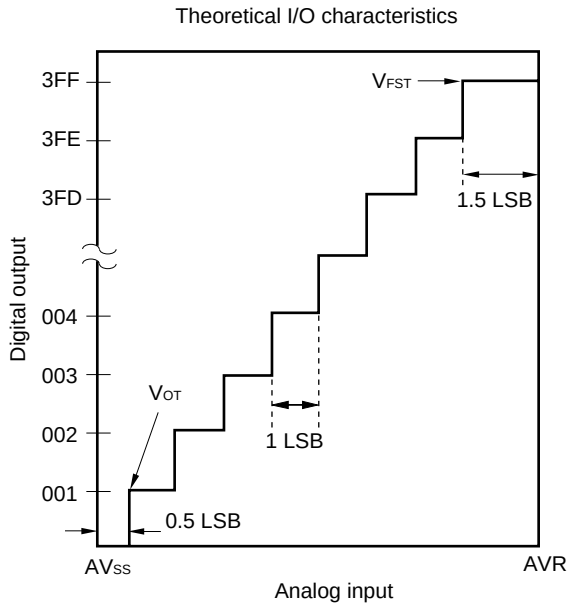


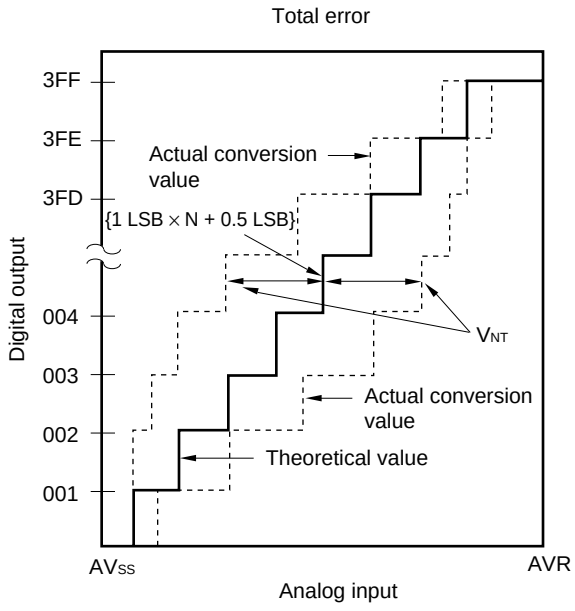
R_{ON1}: Approx. 1.5 Ω
R_{ON2}: Approx. 1.5 Ω
C_0: Approx. 60 pF
C_1: Approx. 4 pF

Note: The values mentioned here should be used as a guideline.

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise





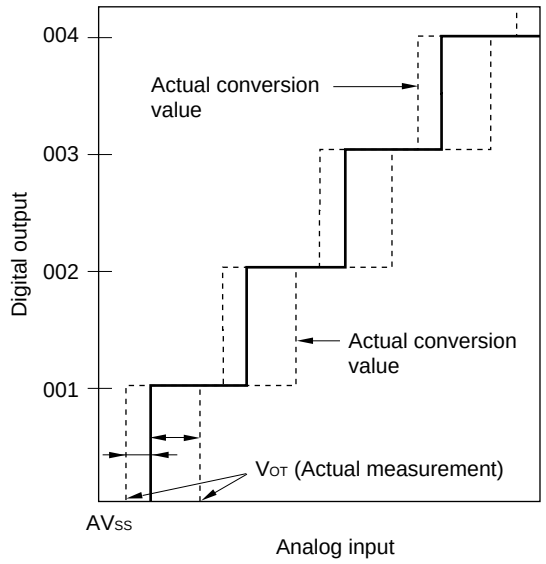
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

$$\text{Digital output N total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

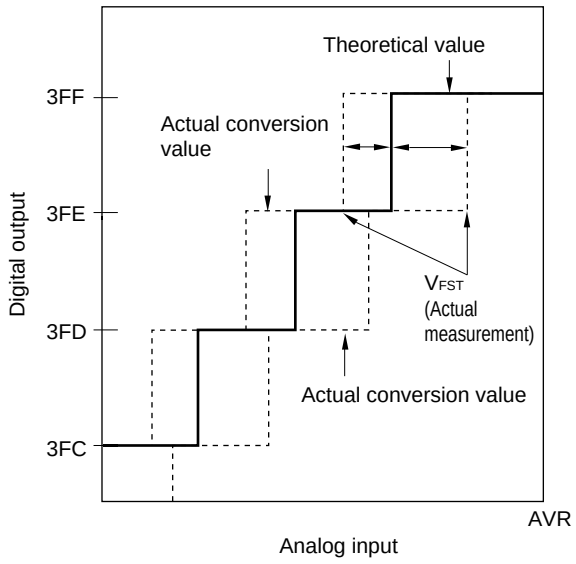
(Continued)

(Continued)

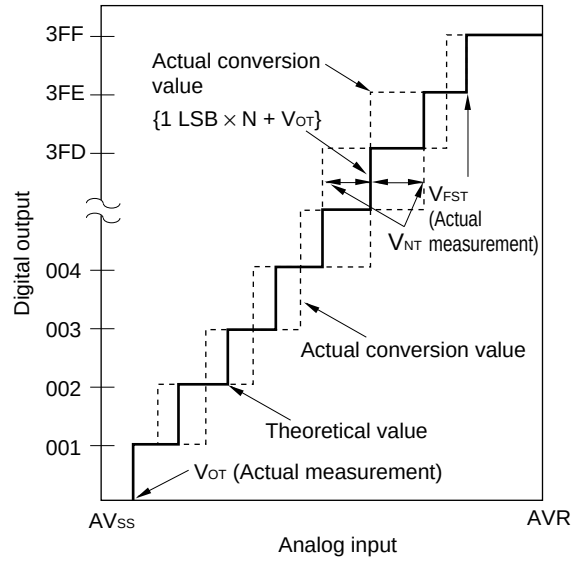
Zero transition error



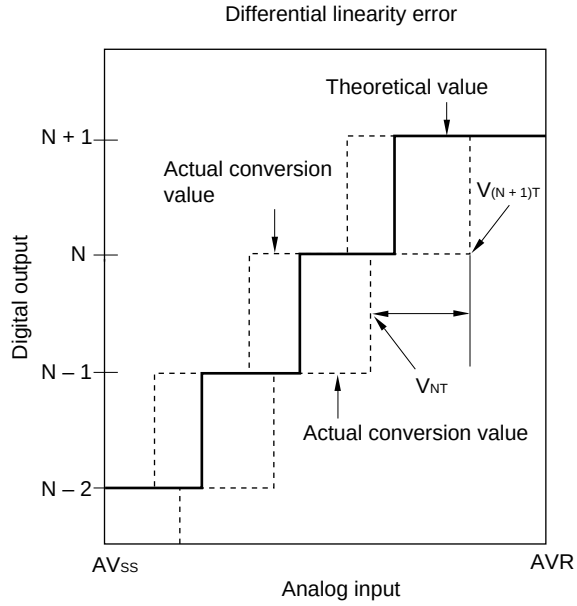
Full-scale transition error



Linearity error



Differential linearity error

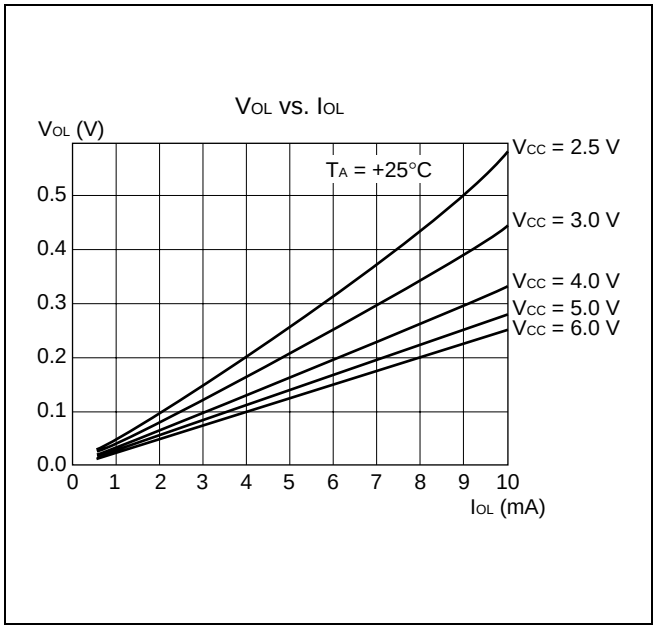


$$\text{Digital output N linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

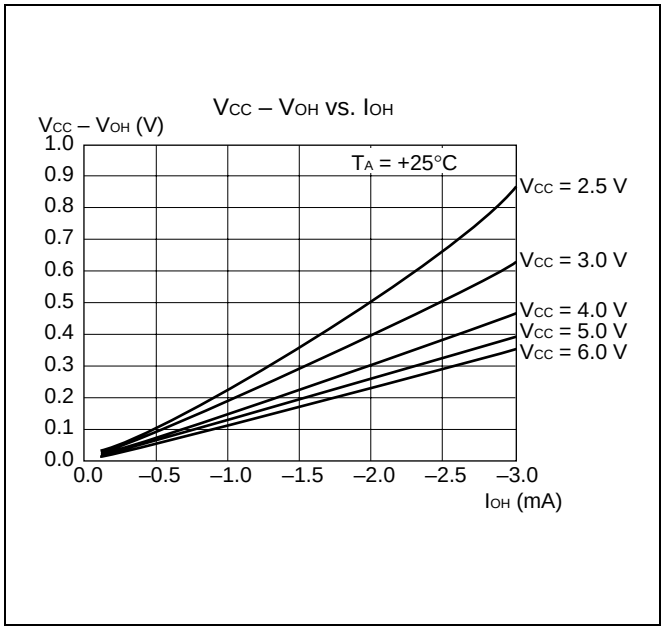
$$\text{Digital output N differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

■ EXAMPLE CHARACTERISTICS

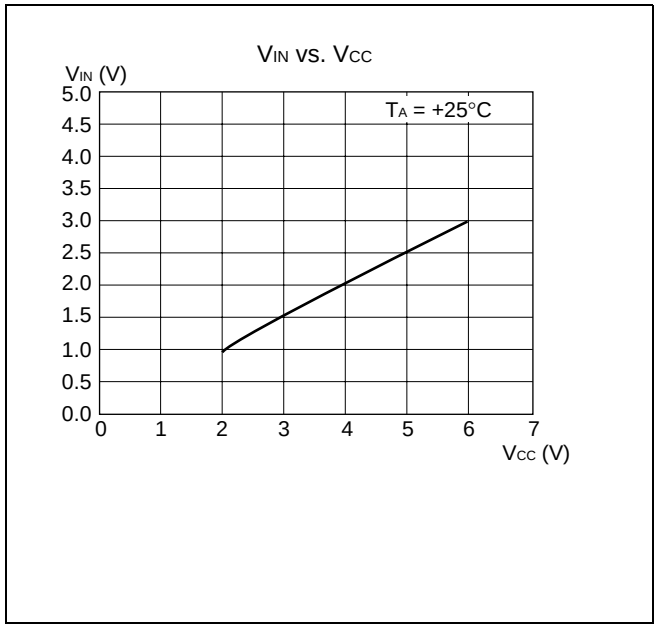
(1) “L” Level Output Voltage



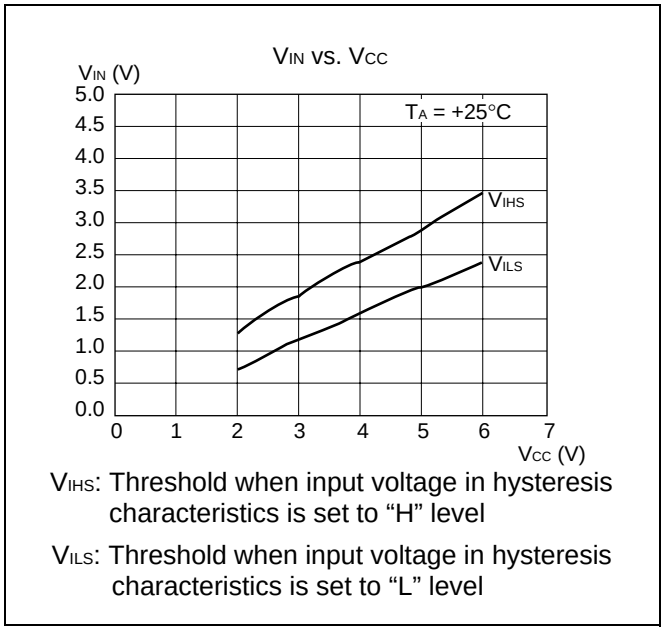
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

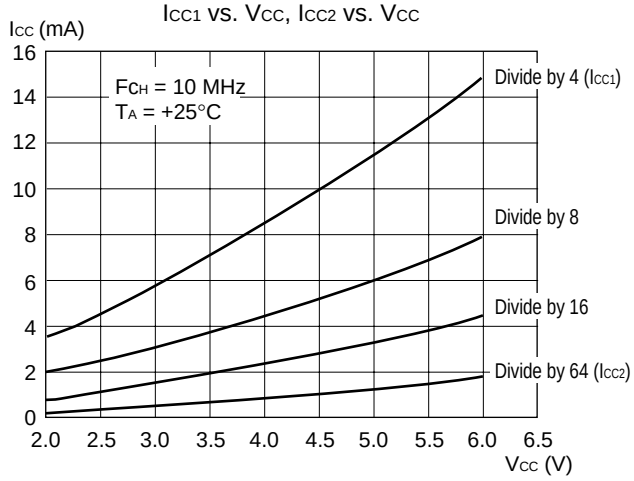


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

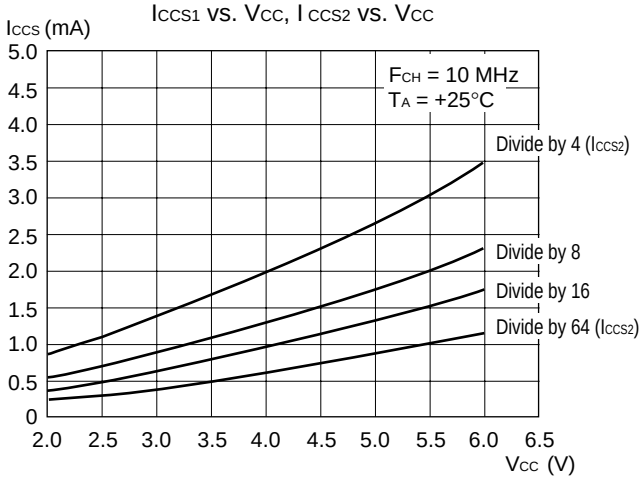
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)

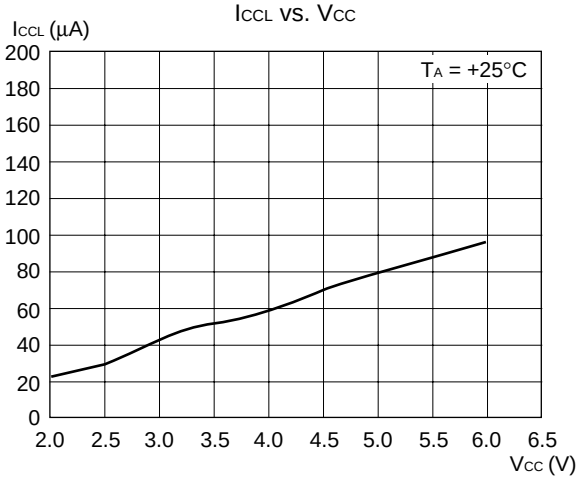
I_{CC1} vs. V_{CC}, I_{CC2} vs. V_{CC}



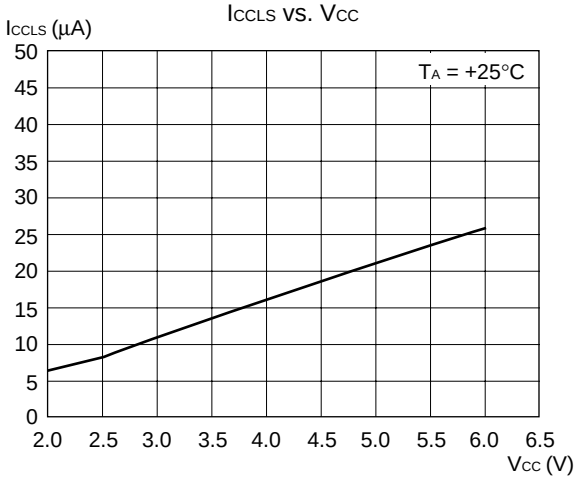
I_{CCS1} vs. V_{CC}, I_{CCS2} vs. V_{CC}



I_{CCL} vs. V_{CC}

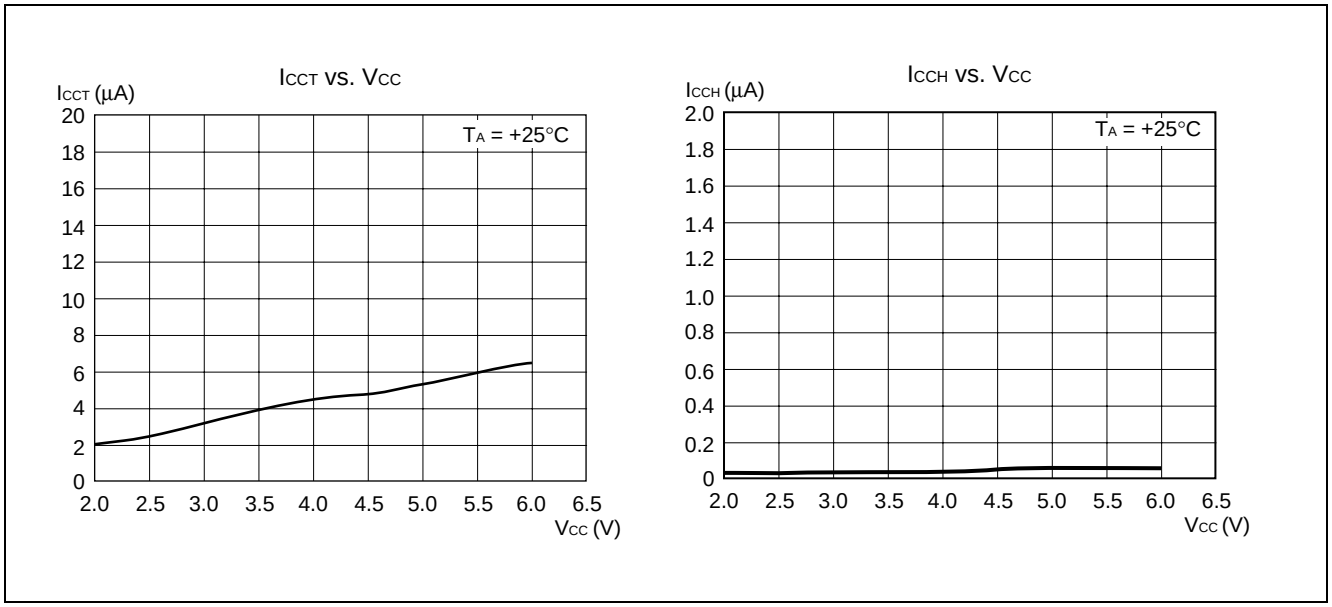


I_{CCLS} vs. V_{CC}

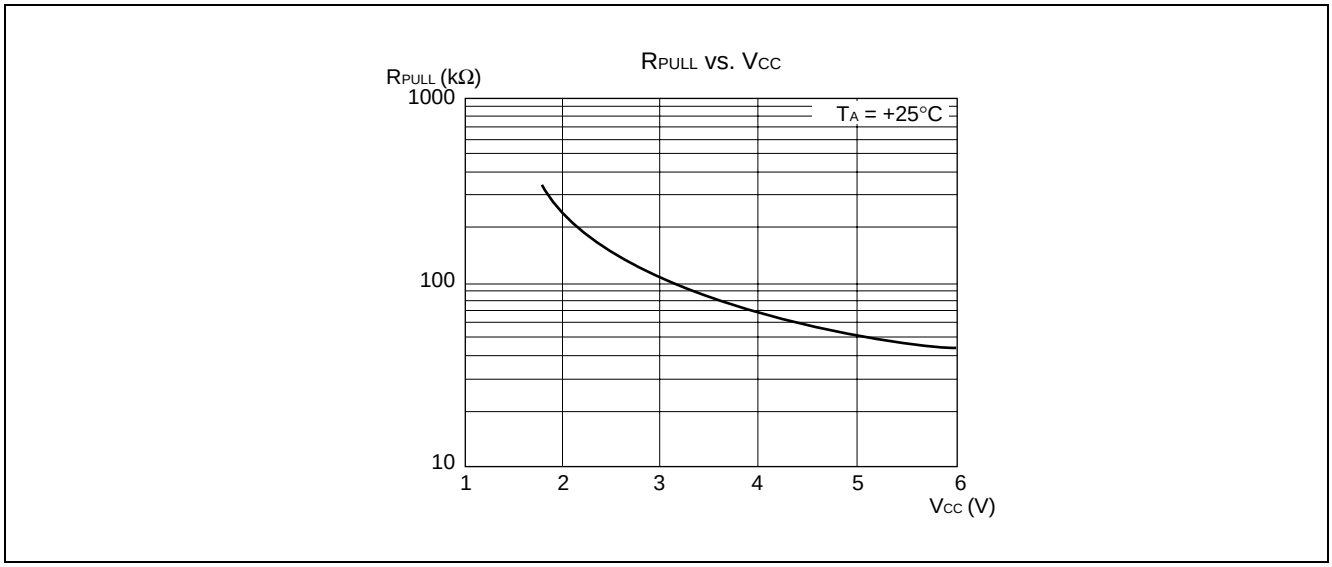


(Continued)

(Continued)



(6) Pull-up Resistance



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:
- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:
- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Note: During byte transfer to A, T ← A is restricted to low bytes.
Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89635 MB89636 MB89637	MB89P637 MB89W637	MB89PV630 MB89T635 MB89T637
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors 〈 P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74	Selectable by pin	Can be set per pin*	Fixed to without pull-up resistor
2	Power-on reset selection 〈 With power-on reset Without power-on reset	Selectable	Setting possible	Fixed to with power-on reset
3	Selection of the main clock oscillation stabilization time (at 10 MHz) 〈 Approx. $2^{18}/F_{CH}$ (Approx. 26.2 ms) Approx. $2^{17}/F_{CH}$ (Approx. 13.1 ms) Approx. $2^{14}/F_{CH}$ (Approx. 1.6 ms) Approx. $2^{4}/F_{CH}$ (Approx. 0 ms) F_{CH} : Main clock frequency	Selectable	Setting possible	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)
4	Reset pin output 〈 Reset output provided No reset output	Selectable	Setting possible	Fixed to with reset output
5	Single/dual-clock system 〈 Single clock Dual clock	Selectable	Setting possible	MB89PV630-101Single-clock system MB89T635-101 Single-clock system MB89T637-101 Single-clock system MB89PV630-102Dual-clock systems MB89T635-102 Dual-clock systems MB89T637-101 Dual-clock systems

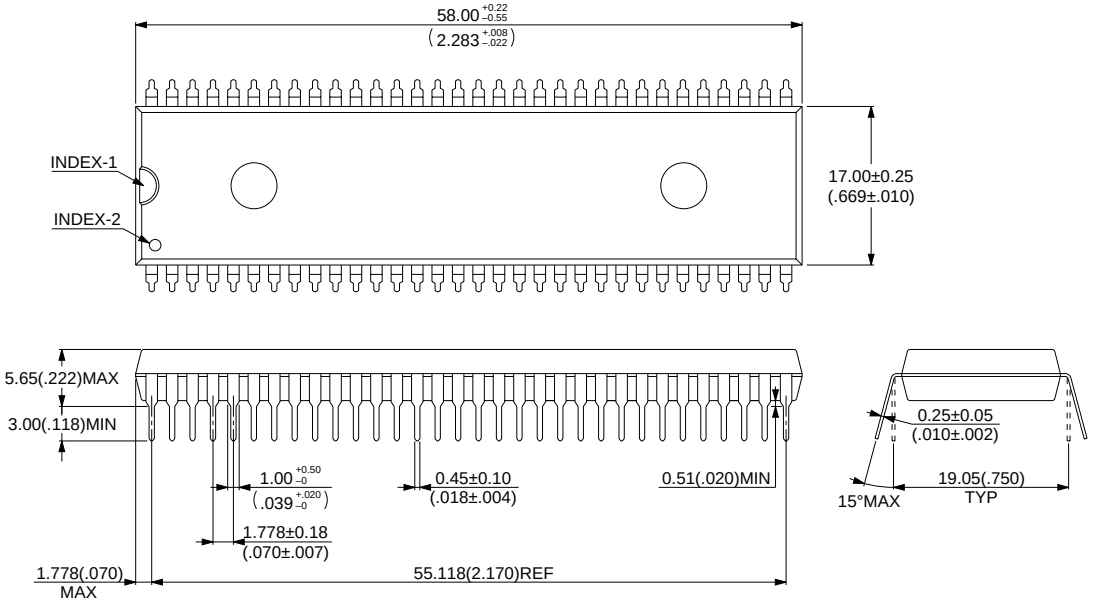
* : Pull-up resistors cannot be set for P50 to P53.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89635P-SH MB89T635P-SH MB89636P-SH MB89637P-SH MB89P637-SH MB89T637P-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89635PF MB89T635PF MB89636PF MB89637PF MB89P637PF MB89T637PF	64-pin Plastic QFP (FPT-64P-M06)	
MB89635PFM MB89T635PFM MB89636PFM MB89637PFM MB89T637PFM	64-pin Plastic QFP (FPT-64P-M09)	
MB89W637C-SH	64-pin Ceramic SH-DIP (DIP-64C-A06)	
MB89PV630C-SH	64-pin Ceramic MDIP (MDP-64C-P02)	
MB89PV630CF	64-pin Ceramic MQFP (MQP-64C-P01)	

■ PACKAGE DIMENSIONS

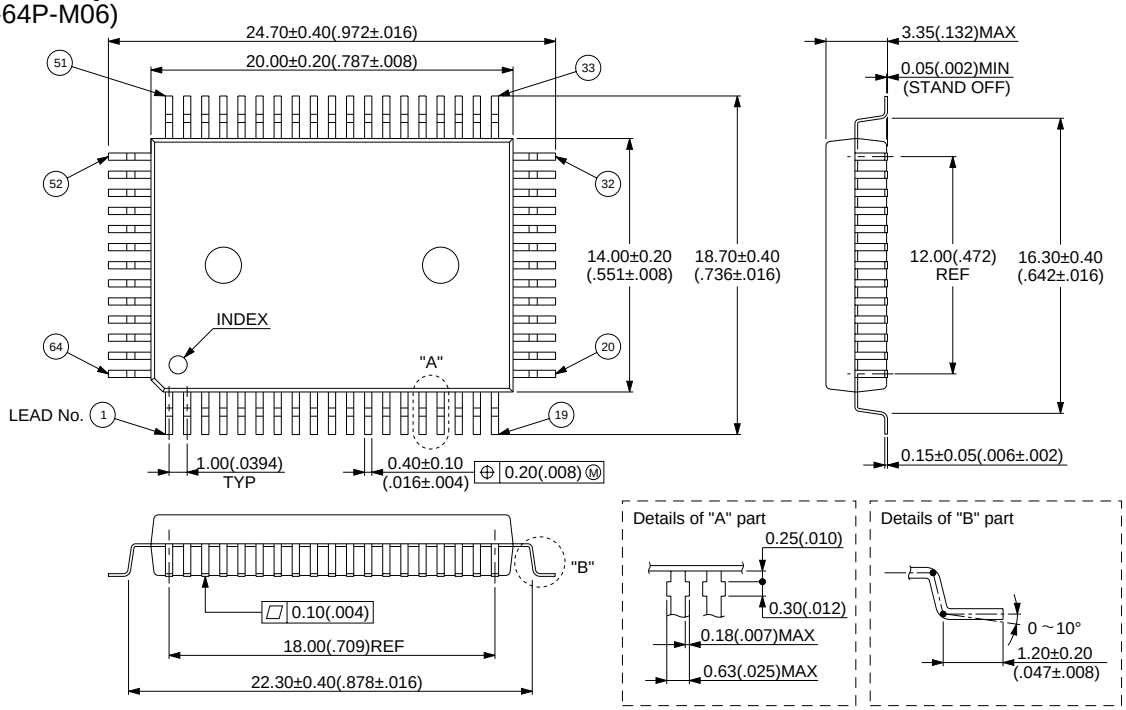
64-pin Plastic SH-DIP
(DIP-64P-M01)



© 1994 FUJITSU LIMITED D64001S-3C-4

Dimensions in mm (inches)

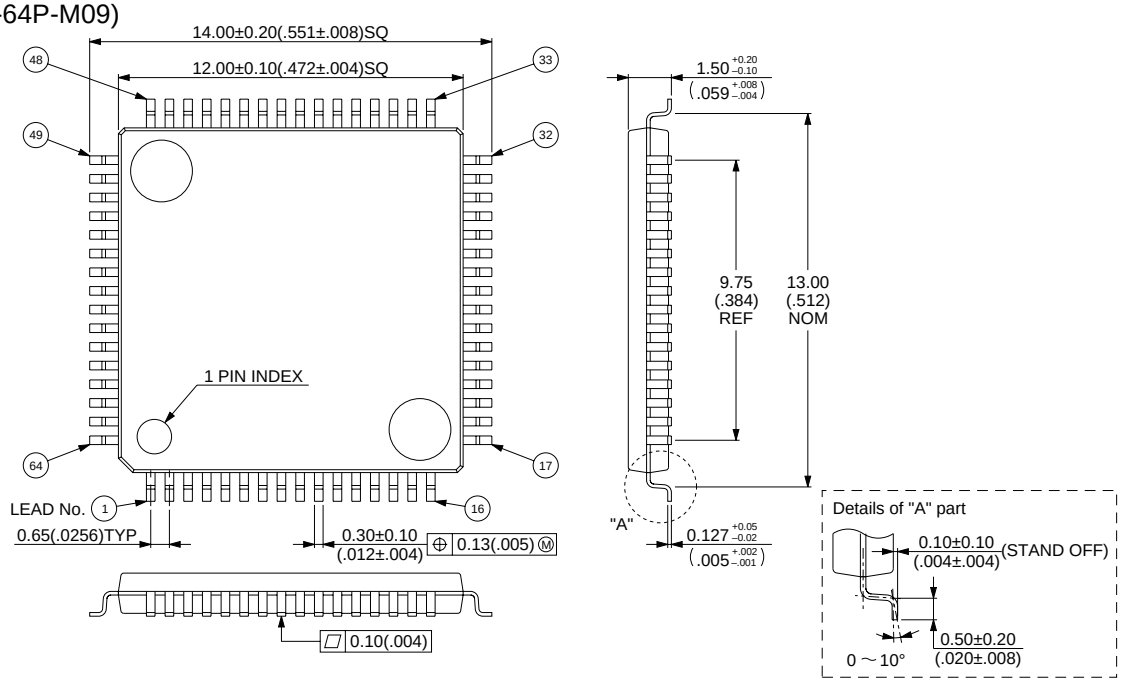
64-pin Plastic QFP
(FPT-64P-M06)



© 1994 FUJITSU LIMITED F64013S-3C-2

Dimensions in mm (inches)

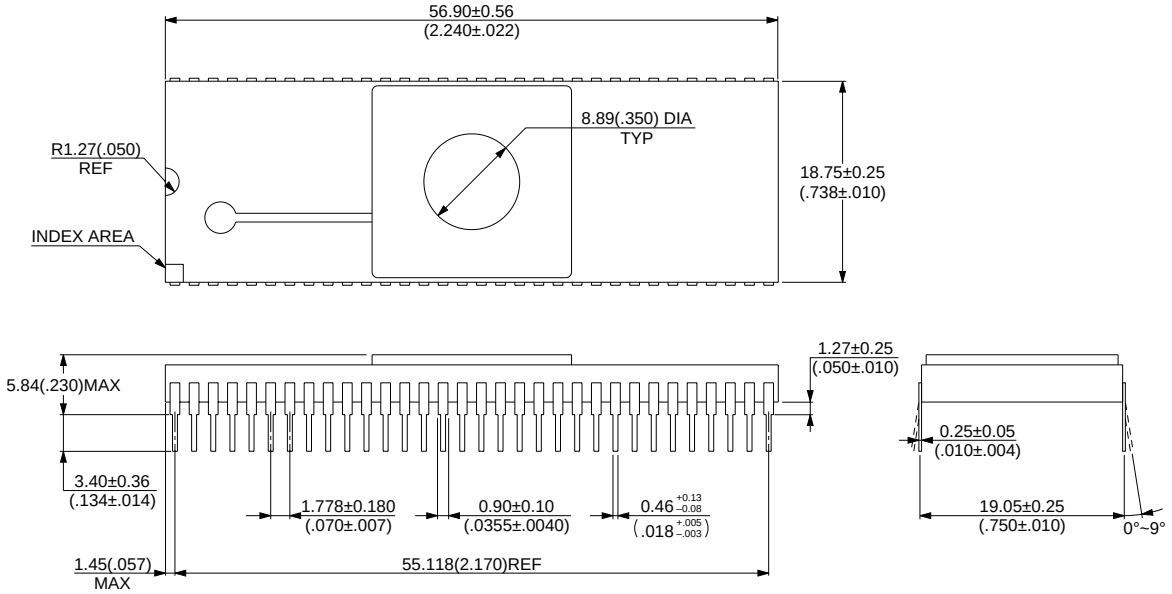
64-pin Plastic QFP
(FPT-64P-M09)



© 1994 FUJITSU LIMITED F64018S-1C-2

Dimensions in mm (inches)

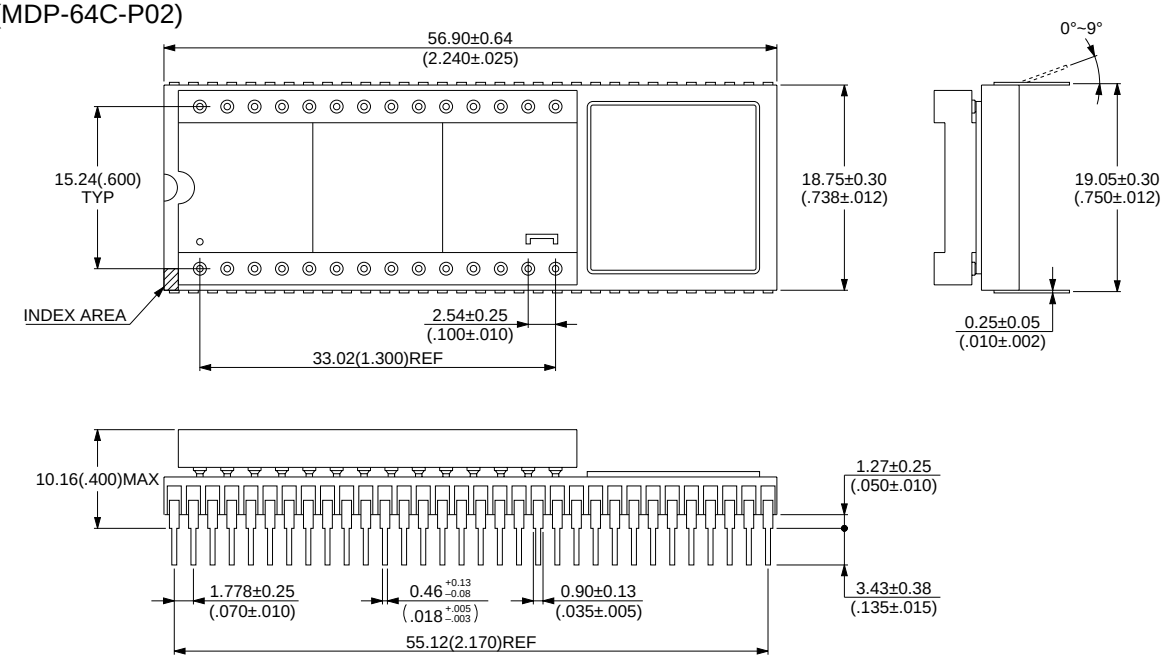
64-pin Ceramic SH-DIP
(DIP-64C-A06)



© 1994 FUJITSU LIMITED D64006SC-1-2

Dimensions in mm (inches)

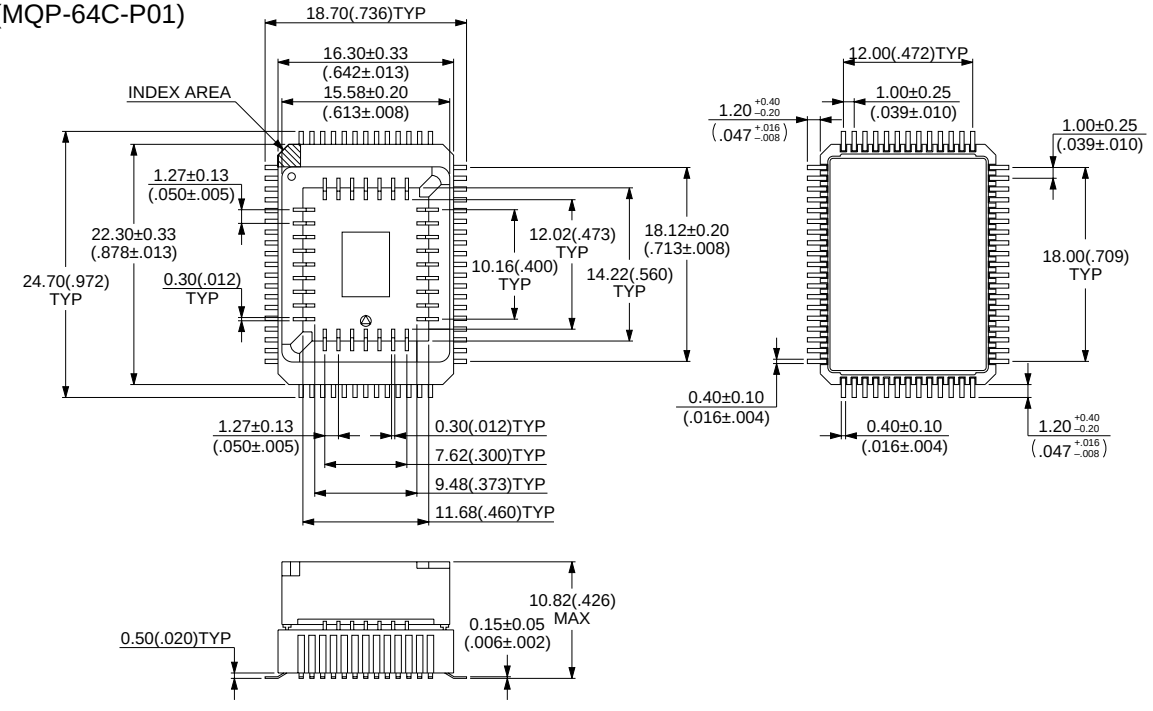
64-pin Ceramic MDIP
(MDP-64C-P02)



© 1994 FUJITSU LIMITED M64002SC-1-4

Dimensions in mm (inches)

64-pin Ceramic MQFP
(MQP-64C-P01)



© 1994 FUJITSU LIMITED M64004SC-1-3

Dimensions in mm (inches)

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F9602
© FUJITSU LIMITED Printed in Japan