MH51208SN-70L,-85L,-10L,-12L,-15L/ MH51208SN-70H,-85H,-10H,-12H,-15H

4194304-BIT(524288-WORD BY 8-BIT) CMOS STATIC RAM MODULE

DESCRIPTION

The MH51208SN is a 4194304 bits CMOS static RAM module organized as 524288-words by 8-bits. It consists of sixteen industry standard 32K x 8 static RAMs.

The stand-by current is low enough for a battery backup application. It is mounted a flat package on a 64-pin single in line package.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH51208SN-70L	70ns	80mA	800 μA
MH51208SN-85L	85ns		
MH51208SN-10L	100ns		
MH51208SN-12L	120ns		
MH51208SN-15L	150ns		
MH51208SN-70H	70ns		250 μA
MH51208SN-85H	85ns		
MH51208SN-10H	100ns		
MH51208SN-12H	120ns		
MH51208SN-15H	150ns		

- 64 Pins single in-line package
- Single +5V power supply
- No clocks, No refresh
- Data-hold on +2V power supply
- Directly TTL compatible: all inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expantion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

APPLICATION

Small capacity memory units.

FUNCTION

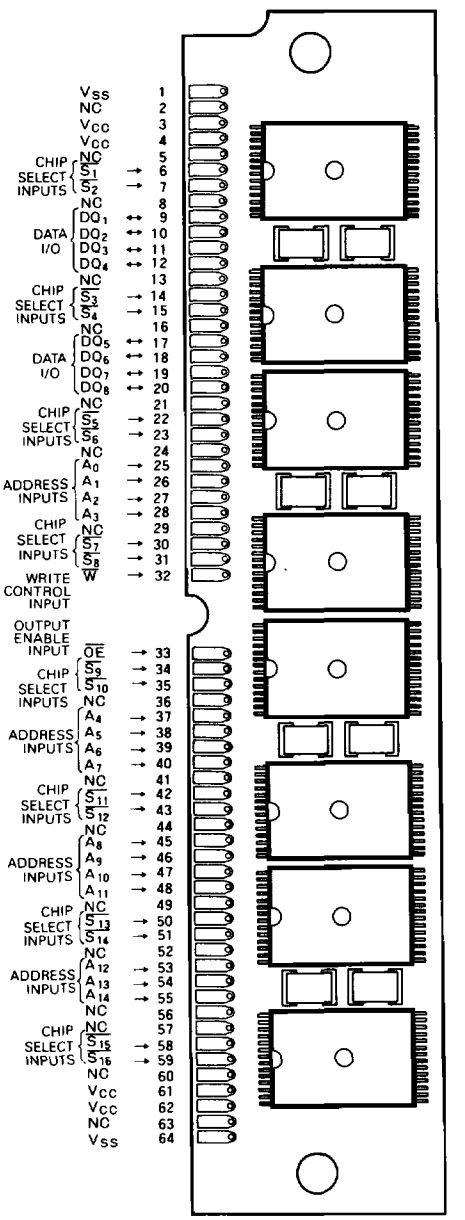
The operation mode of the MH51208SN is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

PIN CONFIGURATION (TOP VIEW)



Outline 64N9W NC NO CONNECTION

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

MITSUBISHI ELECTRIC

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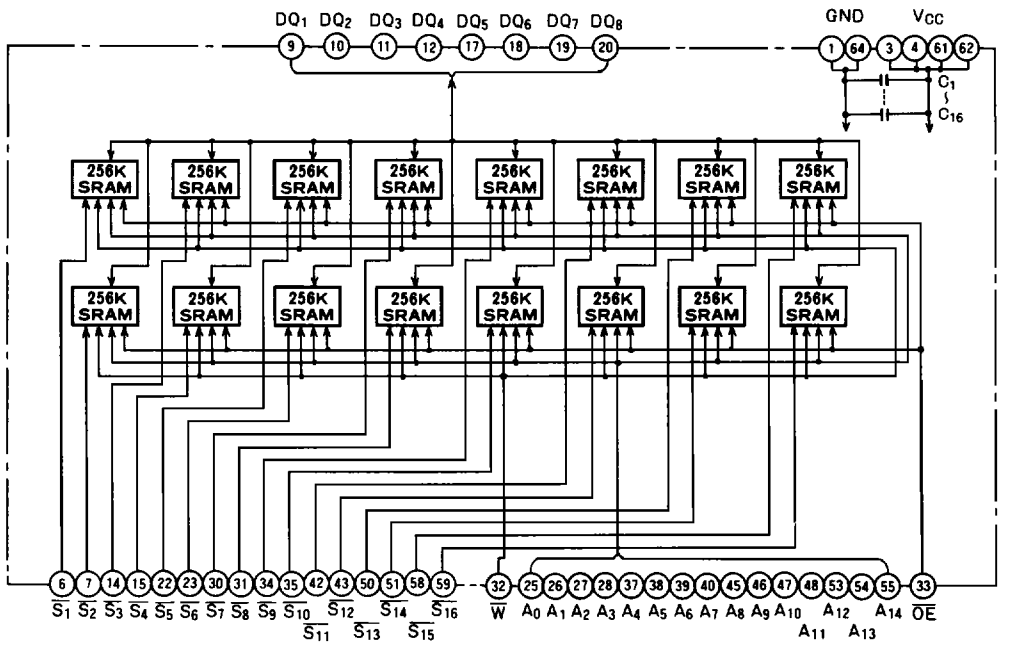
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−40～100	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low input voltage	−0.3		0.8	V
V_{IH}	High input voltage	2.2		V_{CC}+0.3	V

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage	I_{OH}=−1mA		2.4			V
V_{OL}	Low output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0～V_{CC}				±1	μA
I_{OZH}	High level output current in off-state	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}				1	μA
I_{OZL}	Low level output current in off-state	$V_{I/O}$=0−V_{CC}				−1	μA
I_{CC1}	Active supply current (AC. MOS level)	$\overline{S}$<0.2, $\overline{W}$>V_{CC}−0.3 output open other input<0.2 or >V_{CC}−0.3 Min. cycle			40	75	mA
I_{CC2}	Active supply current (AC. TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} output open other input =V_{IL} or V_{IH} Min. cycle			45	80	mA
I_{CC3}	Stand-by supply current	$\overline{S}$≧V_{CC}−0.2V	SN-L			800	μA
		Other inputs=0～V_{CC}	SN-H			250	
I_{CC4}	Stand-by supply current	$\overline{S}$=V_{IH}, Other inputs=0～V_{CC}				18	mA
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS}, V_I=25mVrms, f=1MHz Ta=25°C			80	100	pF
$C_{I(W)}$	Input capacitance, write control input				80	100	pF
$C_{I(OE)}$	Input capacitance, $\overline{OE}$ input				70	90	pF
$C_{I(S)}$	Input capacitance, chip select inputs				8	12	pF
$C_{(DQ)}$	Data input/data output capacitance				75	95	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
2: Typical value is V_{CC} = 5V, T_a = 25°C

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits										Unit
		MH51208SN -70L/-70H		MH51208SN -85L/-85H		MH51208SN -10L/-10H		MH51208SN -12L/-12H		MH51208SN -15L/-15H		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		150		ns
$t_{a(A)}$	Address access time		70		85		100		120		150	ns
$t_{a(S)}$	Chip select access time		70		85		100		120		150	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60		75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		30		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		30		30		35		40		45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5		10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		10		10		10		10		ns
$t_{v(A)}$	Data valid time after address change	20		20		20		20		20		ns

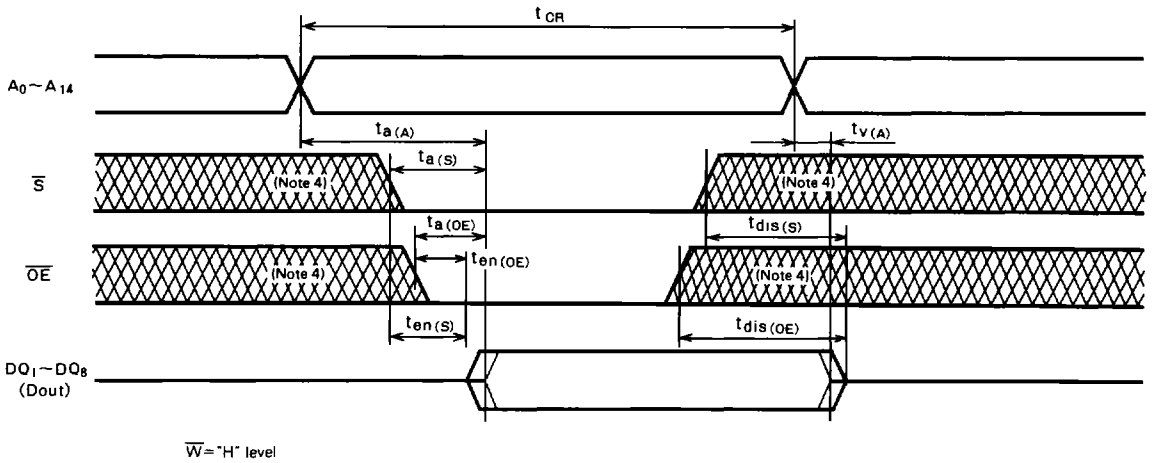
TIMING REQUIREMENTS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits										Unit
		MH51208SN -70L/-70H		MH51208SN -85L/-85H		MH51208SN -10L/-10H		MH51208SN -12L/-12H		MH51208SN -15L/-15H		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		60		60		70		80		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address set up time with respect to $\overline{W}$ high	65		75		80		85		90		ns
$t_{su(S)}$	Chip select set up time	65		75		80		85		90		ns
$t_{su(D)}$	Data set up time	30		35		35		40		50		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		25		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		10		10		10		10		ns

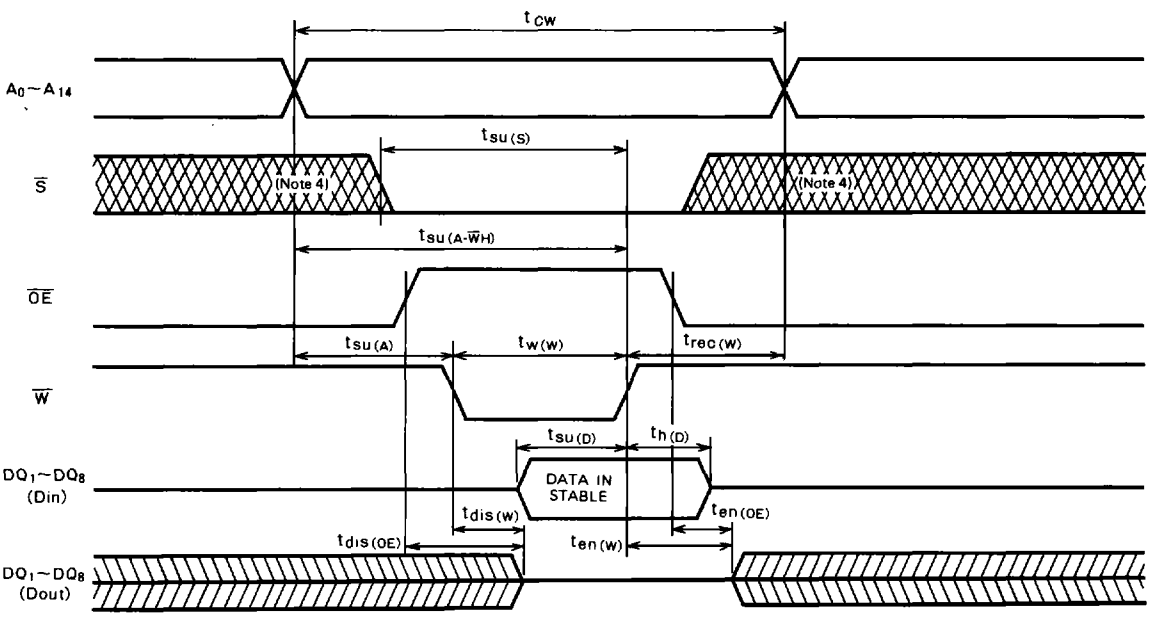
TIMING DIAGRAM

Read cycle

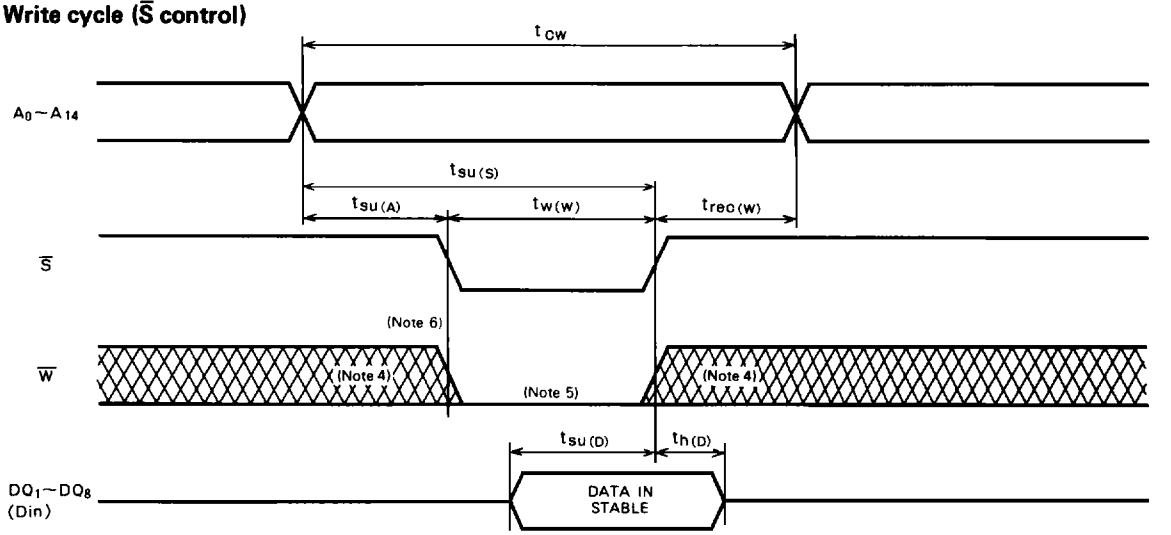


W="H" level

Write cycle (W control)



Write cycle ($\overline{S}$ control)



Note 3: Test condition
Input pulse level: 0.6 ~ 2.4V
Input pulse rise fall time: 10ns
Load 1 TTL. C_L = 100pF
Conditions of assessment: 1.5V
4: Hatching indicates the state is don't care.
5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6: If W goes low simultaneously with or prior to $\overline{S}$, the output remains in the high, impedance state.
7: Don't active inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		V
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, Other inputs = 3V	SN-L			550	μA
			SN-H			110	

TIMING REQUIREMENTS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS