BURR-BROWN®

# ADC80

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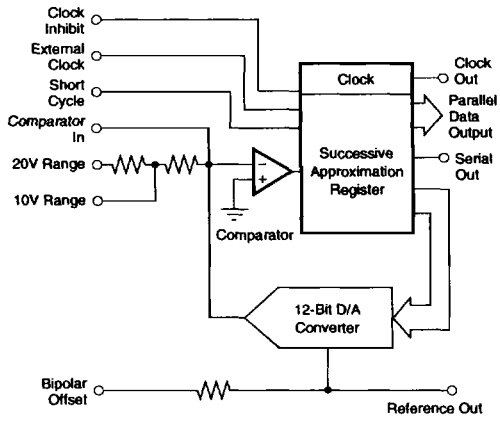
# General Purpose ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- ±0.012% LINEARITY
- 25µs max CONVERSION TIME
- ±12V OR ±15V OPERATION
- NO MISSING CODES: –25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL AND SERIAL OUTPUTS
- 595mW max DISSIPATION




## DESCRIPTION

The ADC80 is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25µs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = +25°C, $\pm V_{CC}$ = 12V or 15V, $V_{DD}$ = +5V, unless otherwise specified.

| PARAMETER | ADC80AG MIN | ADC80AG TYP | ADC80AG MAX | UNITS |
|---|---|---|---|---|
| **RESOLUTION** | | | | |
| ADC80AG-12, ADC80-AGZ-12[1] | | | 12 | Bits |
| ADC80AG-10 | | | 10 | Bits |
| **INPUT** | | | | |
| **ANALOG** | | | | |
| Voltage Ranges: Unipolar | | 0 to +5, 0 to +10 | | V |
| Bipolar | | ±2.5, ±5, ±10 | | V |
| Impedance: 0 to +5V, ±2.5V | 2.45 | 2.5 | 2.55 | kΩ |
| 0 to +10V, +5V | 4.9 | 5 | 5.1 | kΩ |
| ±10V | 9.8 | 10 | 10.2 | kΩ |
| **DIGITAL** | | | | |
| Logic Characteristics (Over specification temperature range) | | | | |
| $V_{IH}$ (Logic "1") | 2 | | 5.5 | V |
| $V_{IL}$ (Logic "0") | −0.3 | | +0.8 | V |
| $I_{IH}$ ($V_{IN}$ = +2.7V) | | | −150 | µA |
| $I_{IL}$ ($V_{IN}$ = +0.4V) | | | 500 | µA |
| Convert Command Pulse Width[2] | 100 | | 2000 | ns |
| **TRANSFER CHARACTERISTICS** | | | | |
| **ACCURACY** | | | | |
| Gain Error[2] | | ±0.1 | ±0.3 | % of FSR[4] |
| Offset Error[3]: Unipolar | | ±0.05 | ±0.2 | % of FSR |
| Bipolar | | ±0.1 | ±0.3 | % of FSR |
| Linearity Error: ADC80AG-12, ADC80AGZ-12 | | | ±0.012 | % of FSR |
| ADC80AG-10 | | | ±0.048 | % of FSR |
| Differential Linearity Error | | ±1/2 | ±3/4 | LSB |
| Inherent Quantization Error | | ±1/2 | | LSB |
| **POWER SUPPLY SENSITIVITY** | | | | |
| 11.4V ≤ $\pm V_{CC}$ ≤ 16.5V | | ±0.003 | ±0.009 | % of FSR/%$V_{CC}$ |
| +4.5V ≤ $V_{DD}$ ≤ +5.5V | | ±0.002 | ±0.005 | % of FSR/%$V_{DD}$ |
| **DRIFT** | | | | |
| Total Accuracy, Bipolar[5] | | ±10 | ±23 | ppm/°C |
| Gain | | ±15 | ±30 | ppm/°C |
| Offset: Unipolar | | ±3 | | ppm of FSR/°C |
| Bipolar | | ±7 | ±15 | ppm of FSR/°C |
| Linearity Error Drift | | ±1 | ±3 | ppm of FSR/°C |
| Differential Linearity over Temperature Range | | | ±3/4 | LSB |
| No Missing Code Temperature Range | −25 | | +85 | °C |
| Monotonicity Over Temperature Range | | Guaranteed | | |
| **CONVERSION TIME[6]** | | | | |
| ADC80AG-12, ADC80-AGZ-12 | 15 | 22 | 25 | µs |
| ADC80AG-10 | 13 | 20 | 22 | µs |
| **OUTPUT** | | | | |
| **DIGITAL** (Bits 1-12 , Clock Out, Status, Serial Out) | | | | |
| Output Codes[7] | | | | |
| Parallel: Unipolar | | CSB | | |
| Bipolar | | COB, CTC | | |
| Serial (NRZ)[8] | | CSB, COB | | |
| Logic Levels: Logic 0 ($I_{SINK}$ ≤ 3.2mA) | | | +0.4 | V |
| Logic 1 ($I_{SOURCE}$ ≤ 80µA) | +2.4 | | | V |
| Internal Clock Frequency | | 545 | | kHz |
| **INTERNAL REFERENCE VOLTAGE** | | | | |
| Voltage | +6.2 | +6.3 | +6.4 | V |
| Source Current Available for External Loads[9] | 200 | | | µA |
| Temperature Coefficient | | ±10 | ±30 | ppm/°C |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = +25°C, $\pm V_{CC}$ = 12V or 15V, $V_{DD}$ = +5V, unless otherwise specified.

| PARAMETER | ADC80AG MIN | ADC80AG TYP | ADC80AG MAX | UNITS |
|---|---|---|---|---|
| **POWER SUPPLY REQUIREMENTS** (For all models) | | | | |
| Voltage: $\pm V_{CC}$ | ±11.4 | ±15 | ±16.5 | V |
| $V_{DD}$ | +4.5 | +5 | +5.5 | V |
| Current: $+I_{CC}$ | | 5 | 8.5 | mA |
| $-I_{CC}$ | | 21 | 26 | mA |
| $I_{DD}$ | | 11 | 15 | mA |
| Power Dissipation ($\pm V_{CC}$ = 15V) | | 450 | 595 | mW |
| Thermal Resistance, $\theta_{JA}$ | | 50 | | °C/W |
| **TEMPERATURE RANGE** (Ambient) | | | | |
| Specification | –25 | | +85 | °C |
| Operating (derated specs) | –55 | | +125 | °C |
| Storage | –65 | | +150 | °C |

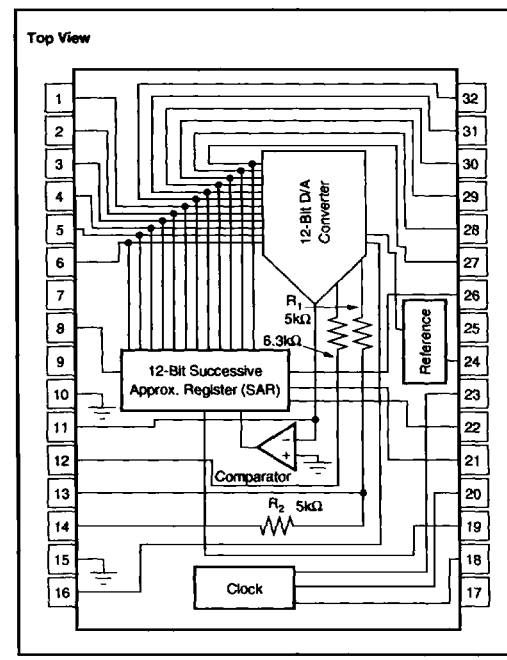
NOTES: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12. (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 2µs (max) to assure the specified conversion time. (3) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drifts. (6) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time: see "Short Cycle Feature" section. (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table 1 for additional information. (8) NRZ means Non-Return-to-Zero coding. (9) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

## PIN ASSIGNMENTS

| PIN | DESCRIPTION | PIN | DESCRIPTION |
|---|---|---|---|
| 1 | Bit 6 | 32 | Bit 7 |
| 2 | Bit 5 | 31 | Bit 8 |
| 3 | Bit 4 | 30 | Bit 9 |
| 4 | Bit 3 | 29 | Bit 10 (LSB-10 Bits) |
| 5 | Bit 2 | 28 | Bit 11 |
| 6 | Bit 1 (MSB) | 27 | Bit 12 (LSB-12 Bits) |
| 7 | NC(1) | 26 | Serial Out |
| 8 | Bit 1 ($\overline{MSB}$) | 25 | $-V_{CC}$ |
| 9 | +5V Digital Supply | 24 | Reference Out (+6.3V) |
| 10 | Digital Common(2) | 23 | Clock Out |
| 11 | *Comparator In* | 22 | *Status* |
| 12 | Bipolar Offset | 21 | Short Cycle |
| 13 | $R_1$ 10V Range | 20 | Clock Inhibit |
| 14 | $R_2$ 20V Range | 19 | External Clock |
| 15 | Analog Common | 18 | Convert Command |
| 16 | Gain Adjust | 17 | $+V_{CC}$ |

NOTE: (1) +5V applied to pin 7 has no effect on circuit. (2) Metal lid of package is connected to pin 10.

## CONNECTION DIAGRAM




## ELECTROSTATIC DISCHARGE SENSITIVITY

*This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.*

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $+V_{CC}$ to Analog Common | 0 to +16.5V |
| $-V_{CC}$ to Analog Common | 0 to −16.5V |
| $V_{DD}$ to Digital Common | 0 to +7V |
| Analog Common to Digital Common | ±0.5V |
| Logic Inputs (Convert Command, Clock In) to Digital Common | −0.3V to $+V_{DD}$ +0.5V |
| Analog Inputs (Analog In, Bipolar Offset) to Analog Common | ±16.5V |
| Reference Output | Indefinite Short to Common, Momentary Short to $V_{CC}$ |
| Lead Temperature, (soldering, 10s) | +300°C |

**CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.**

**Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.**

## ORDERING INFORMATION

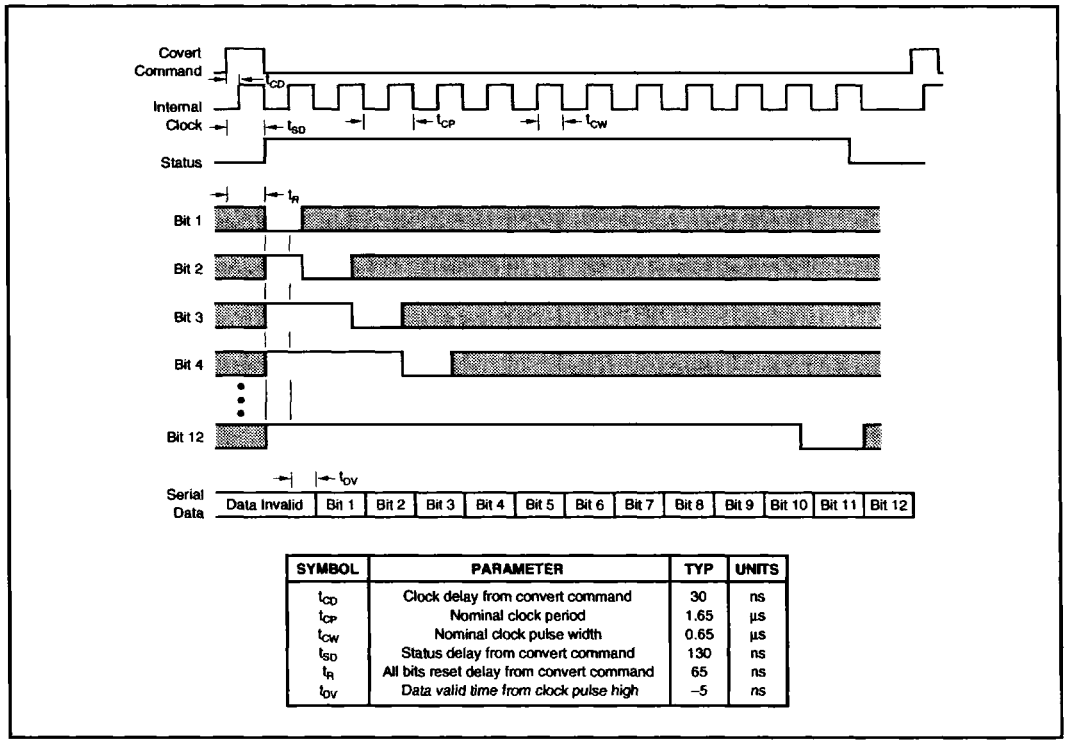
| PRODUCT | RESOLUTION (Bits) |
|---|---|
| ADC80AG-10 | 10 |
| ADC80G-12 | 12 |
| ADC80GZ-12[1] | 12 |

NOTE: (1) ADC80AGZ-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12.

## PACKAGE INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|
| ADC80AG-10 | 32-Pin Hermetic | 172 |
| ADC80G-12 | 32-Pin Hermetic | 172 |
| ADC80AZ-12[1] | 32-Pin Hermetic | 172 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.




| SYMBOL | PARAMETER | TYP | UNITS |
|---|---|---|---|
| $t_{CD}$ | Clock delay from convert command | 30 | ns |
| $t_{CP}$ | Nominal clock period | 1.65 | µs |
| $t_{CW}$ | Nominal clock pulse width | 0.65 | µs |
| $t_{SD}$ | Status delay from convert command | 130 | ns |
| $t_R$ | All bits reset delay from convert command | 65 | ns |
| $t_{DV}$ | *Data valid time from clock pulse high* | −5 | *ns* |

FIGURE 1. ADC80 Timing Diagram (nominal values at +25°C with internal clock).