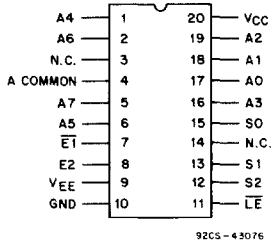
CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

File Number **2145**



CD54/74HC/HCT4351
TERMINAL ASSIGNMENT

Analog Multiplexers/Demultiplexers With Latch

Type Features:

- *Wide analog input voltage range: ± 5 V max.*
- *Low "on" resistance:*
  70 Ω type (V_{CC}-V_{EE} = 4.5 V)
  40 Ω type (V_{CC}-V_{EE} = 9 V)
- *Low crosstalk between switches*
- *Fast switching and propagation speeds*
- *"Break-before-make" switching*

The RCA CD54/74HC/HCT4351, 4352, and 4353 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers are, in essence, the HC/HCT4051, 4052, and 4053 preceded by address latches that are controlled by on active low Latch Enable input ($\overline{LE}$). Two Enable inputs, one active low ($\overline{E1}$), and the other active high (E2) are provided allowing enabling with either input voltage level.

The CD54HC/HCT4351, 4352, and 4353 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT4351, 4352, and 4353 are supplied in 20-lead plastic packages (E suffix) and in 20-lead surface mount plastic packages (M suffix). All devices are also available in chip form (H suffix).

Family Features:

- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40° C to +125° C
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation, control; 0 to 10 V, switch
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation, control; 0 to 10 V, switch
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

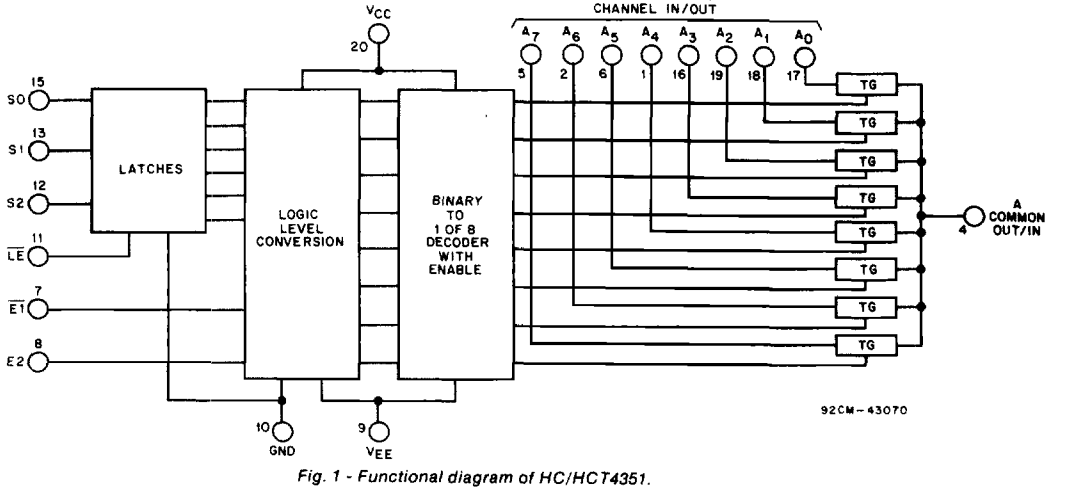


Fig. 1 - Functional diagram of HC/HCT4351.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD/74HC4353, CD54/74HCT4353

TRUTH TABLE
CD54/74HC/HCT4351

INPUT STATES					"ON" SWITCHES
$\overline{E1}$	E2	S2	S1	S0	$\overline{LE}$ = H *
L	H	L	L	L	A_0
L	H	L	L	H	A_1
L	H	L	H	L	A_2
L	H	L	H	H	A_3
L	H	H	L	L	A_4
L	H	H	L	H	A_5
L	H	H	H	L	A_6
L	H	H	H	H	A_7
H	L	X	X	X	None

X = Don't Care.
* When $\overline{LE}$ is low S0-S2 data are latched and switches cannot change state.

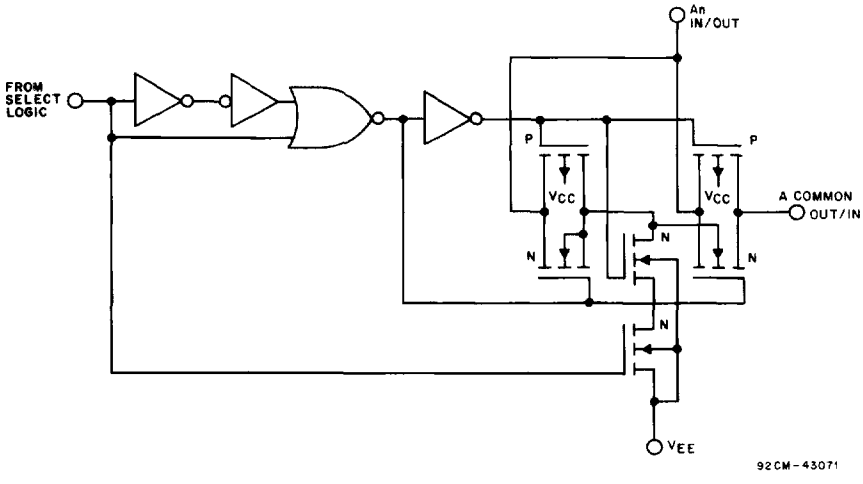
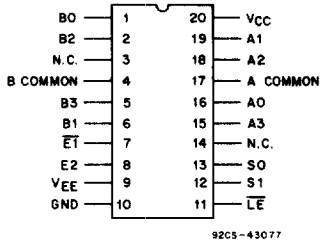


Fig. 2 - Detail of one HC/HCT4351 switch.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353



CD54/74HC/HCT4352
TERMINAL ASSIGNMENT

TRUTH TABLE
CD54/74HC/HCT4352

INPUT STATES				"ON" CHANNELS
$\overline{E1}$	E2	S1	S0	$\overline{LE}$ = H *
L	H	L	L	A_0, B_0
L	H	L	H	A_1, B_1
L	H	H	L	A_2, B_2
L	H	H	H	A_3, B_3
H	L	X	X	None

X = Don't Care.
* When Latch Enable is "Low" channel-select data is latched and switches cannot change state.

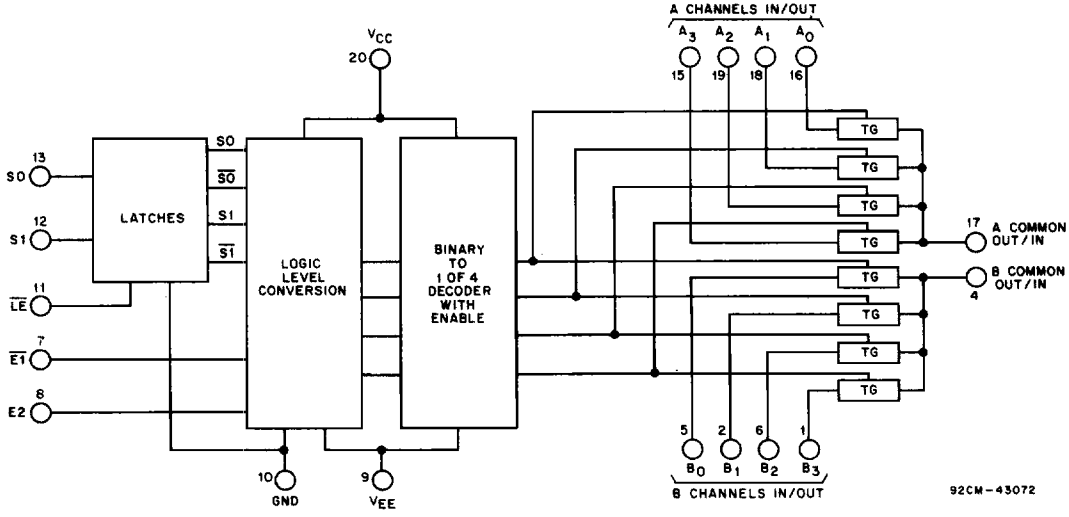


Fig. 3 - Functional diagram of HC/HCT4352.

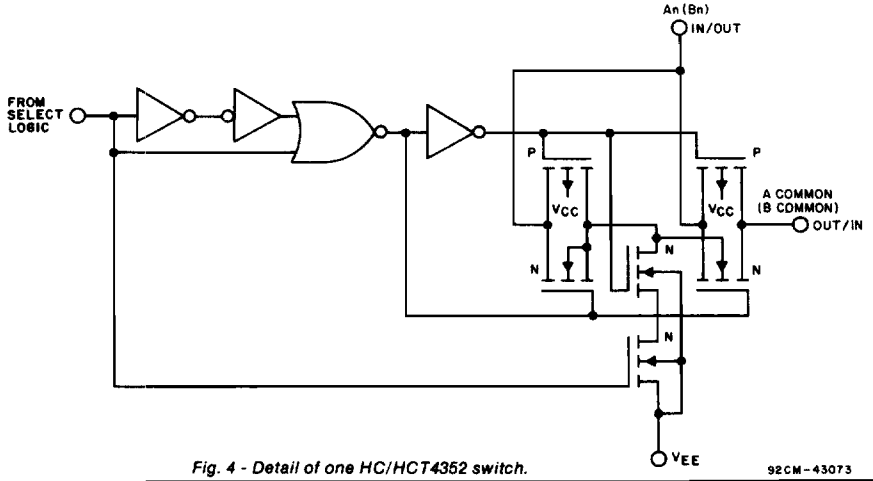
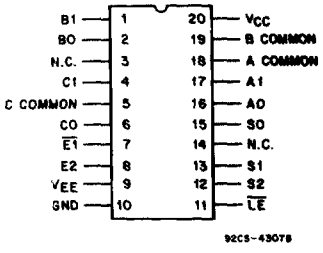


Fig. 4 - Detail of one HC/HCT4352 switch.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353



CD54/74HC/HCT4353
TERMINAL ASSIGNMENT

TRUTH TABLE CD54/74HC/HCT4353

INPUT STATES					"ON" CHANNELS
$\overline{E1}$	E2	S2	S1	S0	$\overline{LE}$ = H *
L	H	L	L	L	C_0, B_0, A_0
L	H	L	L	H	C_0, B_0, A_1
L	H	L	H	L	C_0, B_1, A_0
L	H	L	H	H	C_0, B_1, A_1
L	H	H	L	L	C_1, B_0, A_0
L	H	H	L	H	C_1, B_0, A_1
L	H	H	H	L	C_1, B_1, A_0
L	H	H	H	H	C_1, B_1, A_1
H	X	X	X	X	None
X	L	X	X	X	None

X = Don't Care.
* When Latch Enable is "Low" channel-select data is latched and switches cannot change state.

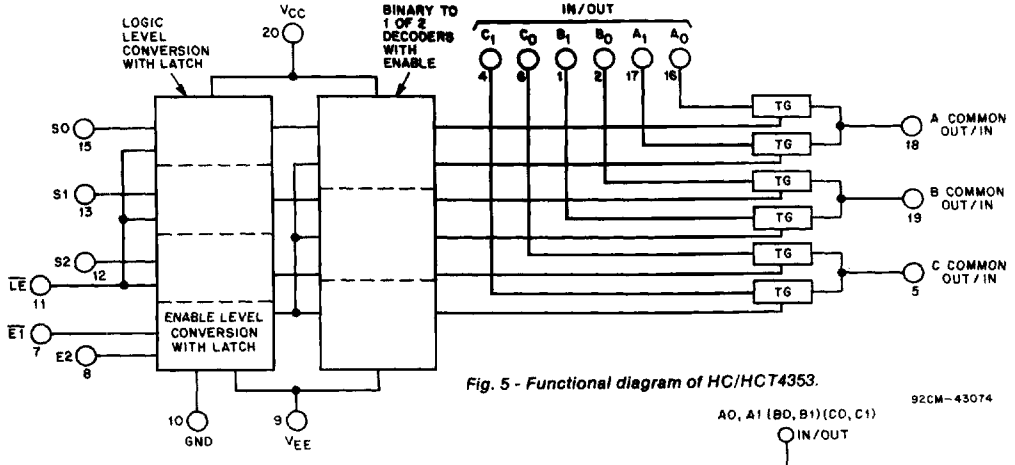


Fig. 5 - Functional diagram of HC/HCT4353.

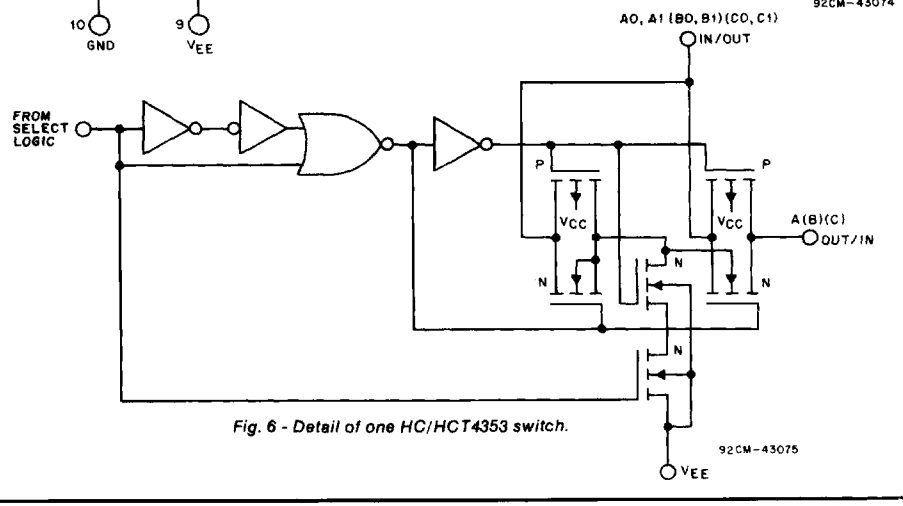


Fig. 6 - Detail of one HC/HCT4353 switch.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

MAXIMUM RATINGS, *Absolute-Maximum Values: (All voltages referenced to Gnd unless otherwise shown)*

DC SUPPLY-VOLTAGE (V_{CC}-V_{EE}) ..... -0.5 to +10.5 V
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to +7 V
DC SUPPLY-VOLTAGE (V_{EE}) ..... +0.5 to -7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_I < V_{EE}$ -0.5 V OR $V_I > V_{CC}$ + 0.5 V) ..... ±20 mA
• DC SWITCH CURRENT (FOR $V_I > V_{EE}$ -0.5 V OR $V_I < V_{CC}$ +0.5 V) ..... +25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
DC V_{EE} CURRENT (I_{EE}) ..... -20 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +100°C (PACKAGE TYPE E) ..... *500 mW*
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

• In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 volt (calculated from R_{ON} values shown in Electrical Characteristics chart). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4351; terminals 3 and 13 on the HC/HCT4352; terminals 4, 14 and 15 on the HC/HCT4353.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}-V_{EE} CD54/74HC Types CD54/74HCT Types See Fig. 7	2	10	V
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{EE}: * CD54/74HC Types CD54/74HCT Types See Fig. 8	0	-6	V
DC Input Control Voltage, V_I	Gnd	V_{CC}	V
Analog Switch I/O Voltage, V_{IS}	V_{EE}	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

RECOMMENDED OPERATING AREA AS A FUNCTION OF SUPPLY VOLTAGES

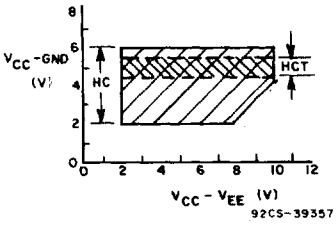


Fig. 7

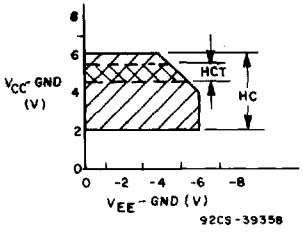


Fig. 8

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC/CD54HC4351, 4352, 4353											CD74HCT/CD54HCT4351, 4352, 4353											UNITS
	TEST CONDITIONS				74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS				74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_S V	V_I V	V_{EE} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_{IS} V	V_I V	V_{EE} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
					Min	Typ	Max	Min	Max	Min	Max					Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}				2	1.5	—	—	1.5	—	1.5	—				4.5 to 5.5	2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—												
				6	4.2	—	—	4.2	—	4.2	—												
Low-Level Input Voltage V_{IL}				2	—	—	0.5	—	0.5	—	0.5				4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35												
				6	—	—	1.8	—	1.8	—	1.8												
"On" Resistance I_O = 1 mA R_{on} (Fig. 20)	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	—	70	160	—	200	—	240			0	4.5	—	70	160	—	200	—	240	Ω
			0	6	—	60	140	—	175	—	210			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	40	120	—	150	—	180			-4.5	4.5	—	40	120	—	150	—	180	
	V_{CC} to V_{EE}		0	4.5	—	90	180	—	225	—	270			0	4.5	—	90	180	—	225	—	270	Ω
			0	6	—	80	160	—	200	—	240			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	45	130	—	162	—	195			-4.5	4.5	—	45	130	—	162	—	195	
Maximum "On" Resistance between any two channels ΔR_{on}			0	4.5	—	10	—	—	—	—	—			0	4.5	—	10	—	—	—	—	—	Ω
			0	6	—	8.5	—	—	—	—	—			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	5	—	—	—	—	—			-4.5	4.5	—	5	—	—	—	—	—	
Switch On/Off Leakage Current I_{IZ} 1&2 Channels (4353) 4 Channels (4352) 8 Channels (4351)	For Switch OFF: When $V_{IS}=V_{CC}$ $V_{OS}=V_{EE}$; When $V_{IS}=V_{EE}$, $V_{OS}=V_{CC}$ For Switch ON: All Applicable Combinations of V_{IS} & V_{OS} Voltage Levels	V_{IL} or V_{IH}	0	6	—	—	±0.1	—	±1	—	±1			0	6	—	—	±0.1	—	±1	—	±1	μA
			-5	5	—	—	±0.1	—	±1	—	±1			-5	5	—	—	±0.1	—	±1	—	±1	
			0	6	—	—	±0.1	—	±1	—	±1			0	6	—	—	±0.1	—	±1	—	±1	
			-5	5	—	—	±0.2	—	±2	—	±2			-5	5	—	—	±0.2	—	±2	—	±2	
			0	6	—	—	±0.2	—	±2	—	±2			0	6	—	—	±0.2	—	±2	—	±2	
			-5	5	—	—	±0.4	—	±4	—	±4			-5	5	—	—	±0.4	—	±4	—	±4	
Control Input Leakage Current I_{IL}	—	V_{CC} or Gnd	0	6	—	—	±0.1	—	±1	—	±1	—	**		5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC} I_O = 0	When $V_{IS}=V_{EE}$, $V_{OS}=V_{CC}$, When $V_{IS}=V_{CC}$, $V_{OS}=V_{EE}$	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	Same as HC	Same as HC	0	5.5	—	—	8	—	80	—	160	μA
			-5	5	—	—	16	—	160	—	320			-4.5	5.5	—	—	16	—	160	—	320	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*													V_{CC}-2.1		4.5 to 5.5	—	100	360	—	450	—	490	μA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

** Any voltage between V_{CC} & Gnd.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

HCT INPUT LOADING TABLE

TYPE	INPUT	UNIT LOADS *
All	$\overline{E1}$, E2, S_n	0.5
(4351, 4352, 4353)	$\overline{LE}$	1.5

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	LIMITS						UNITS
			4351		4352		4353		
			HC	HCT	HC	HCT	HC	HCT	
Turn "On" Time	t_{PZH}	15	27	35	35	40	21	23	ns
$\overline{E1}$, E2, or S_n to V_{OS}	t_{PZL}								
Turn "Off" Time	t_{PHZ}		21	23	21	25	19	21	
$\overline{E1}$, E2, or S_n to V_{OS}	t_{PLZ}								
Power Dissipation Capacitance *	C_{PD}	—	50	52	74	76	38	42	pF

* C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$.
f_o = output frequency.
f_i = input frequency.
C_L = output load capacitance.
C_S = switch capacitance.
V_{CC} = supply voltage.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V_{EE}	V_{CC}	LIMITS												UNITS
			+25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Propagation Delay t_{PLH}	0	2	—	35	—	—	—	45	—	—	—	55	—	—	ns
Switch In to Out t_{PHL}	0	4.5	—	7	—	7	—	9	—	9	—	11	—	11	
4351, 4352, 4353	0	6	—	6	—	—	—	8	—	—	—	9	—	—	
	-4.5	4.5	—	5	—	5	—	7	—	7	—	8	—	8	
Maximum Switch t_{PZH}	0	2	—	300	—	—	—	375	—	—	—	450	—	—	
Turn "On" Delay t_{PZL}	0	4.5	—	60	—	75	—	75	—	94	—	90	—	113	
4351	0	6	—	51	—	—	—	64	—	—	—	77	—	—	
$\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	-4.5	4.5	—	55	—	60	—	69	—	75	—	83	—	90	
4351	0	2	—	300	—	—	—	375	—	—	—	450	—	—	
S_n to V_{OS}	0	4.5	—	60	—	75	—	75	—	94	—	90	—	113	
	0	6	—	51	—	—	—	64	—	—	—	77	—	—	
	-4.5	4.5	—	50	—	60	—	63	—	75	—	75	—	90	
4352	0	2	—	350	—	—	—	440	—	—	—	525	—	—	
$\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	0	4.5	—	70	—	80	—	88	—	100	—	105	—	120	
	0	6	—	60	—	—	—	75	—	—	—	90	—	—	
	-4.5	4.5	—	60	—	65	—	75	—	81	—	90	—	98	
4352	0	2	—	375	—	—	—	470	—	—	—	565	—	—	
S_n to V_{OS}	0	4.5	—	75	—	80	—	94	—	100	—	113	—	120	
	0	6	—	64	—	—	—	80	—	—	—	96	—	—	
	-4.5	4.5	—	55	—	65	—	69	—	81	—	83	—	98	
4353	0	2	—	300	—	—	—	375	—	—	—	450	—	—	
$\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	0	4.5	—	60	—	75	—	75	—	94	—	90	—	113	
	0	6	—	51	—	—	—	64	—	—	—	77	—	—	
	-4.5	4.5	—	55	—	60	—	69	—	75	—	83	—	90	
4353	0	2	—	300	—	—	—	375	—	—	—	450	—	—	
S_n to V_{OS}	0	4.5	—	60	—	75	—	75	—	94	—	90	—	113	
	0	6	—	58	—	—	—	69	—	—	—	77	—	—	
	-4.5	4.5	—	50	—	60	—	63	—	75	—	75	—	90	
Maximum Switch t_{PHZ}	0	2	—	250	—	—	—	315	—	—	—	375	—	—	
Turn "Off" Delay t_{PLZ}	0	4.5	—	50	—	55	—	63	—	69	—	75	—	83	
4351	0	6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{E1}$ to V_{OS}	-4.5	4.5	—	40	—	40	—	50	—	50	—	60	—	60	
4351	0	2	—	250	—	—	—	315	—	—	—	375	—	—	
E2 to V_{OS}	0	4.5	—	50	—	60	—	63	—	75	—	75	—	90	
	0	6	—	43	—	—	—	54	—	—	—	64	—	—	
	-4.5	4.5	—	40	—	50	—	50	—	63	—	60	—	75	
4351	0	2	—	275	—	—	—	345	—	—	—	415	—	—	
$\overline{LE}$ to V_{OS}	0	4.5	—	55	—	60	—	69	—	75	—	83	—	90	
	0	6	—	47	—	—	—	59	—	—	—	71	—	—	
	-4.5	4.5	—	45	—	55	—	56	—	69	—	68	—	83	

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns) (Continued)

CHARACTERISTIC	V_{EE}	V_{CC}	LIMITS												UNITS
			+25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Maximum Switch t_{PHZ}	0	2	—	275	—	—	—	345	—	—	—	415	—	—	ns
Turn "Off" Delay t_{PLZ}	0	4.5	—	55	—	65	—	69	—	81	—	83	—	98	
4351	0	6	—	47	—	—	—	59	—	—	—	71	—	—	
S_n to V_{OS}	-4.5	4.5	—	48	—	55	—	60	—	69	—	71	—	83	
4352	0	2	—	275	—	—	—	345	—	—	—	415	—	—	
$\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	0	4.5	—	55	—	60	—	69	—	75	—	83	—	90	
	0	6	—	47	—	—	—	59	—	—	—	71	—	—	
	-4.5	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
4352	0	2	—	300	—	—	—	375	—	—	—	450	—	—	
S_n to V_{OS}	0	4.5	—	60	—	60	—	75	—	75	—	90	—	90	
	0	6	—	51	—	—	—	64	—	—	—	77	—	—	
	-4.5	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
4353	0	2	—	275	—	—	—	345	—	—	—	415	—	—	
$\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	0	4.5	—	55	—	60	—	69	—	75	—	83	—	90	
	0	6	—	47	—	—	—	59	—	—	—	71	—	—	
	-4.5	4.5	—	45	—	55	—	56	—	69	—	68	—	83	
4353	0	2	—	275	—	—	—	345	—	—	—	415	—	—	
S_n to V_{OS}	0	4.5	—	54	—	65	—	69	—	81	—	83	—	98	
	0	6	—	47	—	—	—	59	—	—	—	71	—	—	
	-4.5	4.5	—	45	—	55	—	56	—	69	—	68	—	83	
Setup Time	0	2	60	—	—	—	75	—	—	—	90	—	—	—	
4351 and 4353	0	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
S_n to $\overline{LE}$	0	6	10	—	—	—	13	—	—	—	15	—	—	—	
	-4.5	4.5	18	—	14	—	23	—	18	—	27	—	21	—	
Hold Time	0	2	5	—	—	—	5	—	—	—	5	—	—	—	
All	0	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
S_n to $\overline{LE}$	0	6	5	—	—	—	5	—	—	—	5	—	—	—	
	-4.5	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
Pulse Width t_W	0	2	100	—	—	—	125	—	—	—	150	—	—	—	
4351 and 4353	0	4.5	20	—	25	—	25	—	31	—	30	—	28	—	
$\overline{LE}$	0	6	17	—	—	—	21	—	—	—	26	—	—	—	
	-4.5	4.5	25	—	25	—	31	—	31	—	38	—	38	—	
4352	0	2	100	—	—	—	125	—	—	—	150	—	—	—	
$\overline{LE}$	0	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
	0	6	17	—	—	—	21	—	—	—	26	—	—	—	
	-4.5	4.5	25	—	25	—	31	—	31	—	38	—	38	—	
Input (Control) C_I Capacitance All	—	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

ANALOG CHANNEL CHARACTERISTICS - TYPICAL VALUES AT T_A = 25°C

CHARACTERISTIC		TEST CONDITIONS	TYPES	LIMITS			UNITS
				V_{EE} (V)	V_{CC} (V)	HC/HCT	
Switch Input Capacitance	C_I		All			5	pF
Common Capacitance	C_{COM}		4351			25	
			4352			12	
			4353			8	
Minimum Switch Frequency	f_{MAX}	See Fig. 9	4351			145	MHz
Response @ -3 dB		Notes 1, 2	4352	-2.25	2.25	165	
Figs. 14, 16, 18			4353			200	
			4351			180	
			4352	-4.5	4.5	185	
			4353			>200	
Crosstalk Between Any Two		See Fig. 10	4351			N/A	dB
Switches		Notes 2, 3	4352	-2.25	2.25	(TBE)	
Note 4			4353			(TBE)	
			4351			N/A	
			4352	-4.5	4.5	(TBE)	
			4353			(TBE)	
Sine-Wave Distortion		See Fig. 11	All	-2.25	2.25	0.035	%
			All	-4.5	4.5	0.018	
$\overline{E}$ or S to Switch		See Fig. 12	4351				mV
Feedthrough Noise		Notes 2, 3	4352	-2.25	2.25	(TBE)	
			4353				
			4351				
			4352	-4.5	4.5	(TBE)	
			4353				
Switch "OFF"		See Fig. 13	4351			-73	dB
Signal Feedthrough		Notes 2, 3	4352	-2.25	2.25	-65	
Figs. 15, 17, 19			4353			-64	
			4351			-75	
			4352	-4.5	4.5	-67	
			4353			-66	

Notes:
1. Adjust input voltage to obtain OdBm @ V_{OS} for f_{in} = 1 MHz.
2. V_{IS} is centered at (V_{CC} - V_{EE})/2.
3. Adjust input for OdBm.
4. Not applicable for HC/HCT4351.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

ANALOG TEST CIRCUITS

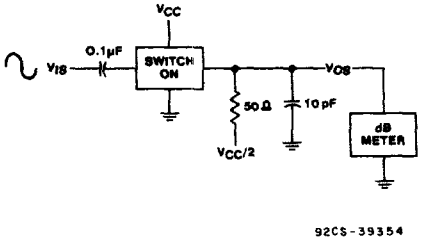


Fig. 9 - Frequency response test circuit.

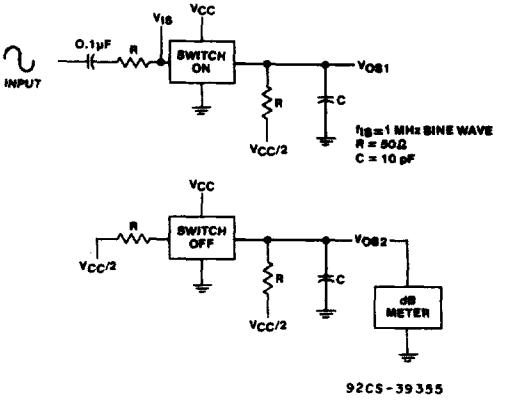


Fig. 10 - Crosstalk between two switches test circuit.

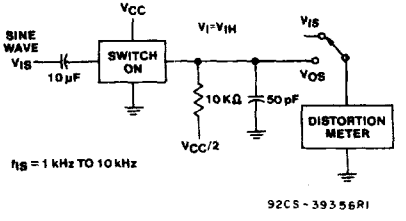


Fig. 11 - Sine wave distortion test circuit.

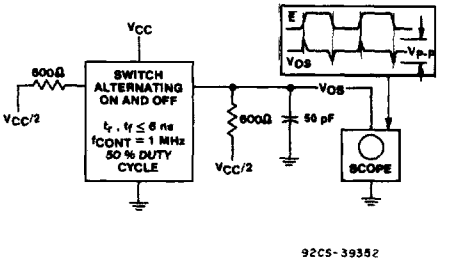


Fig. 12 - Control-to-switch feedthrough noise test circuit.

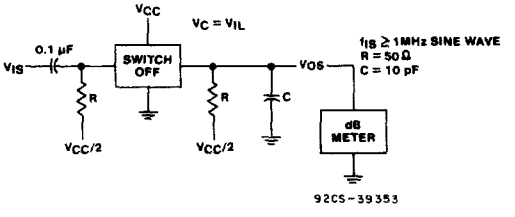


Fig. 13 - Switch off signal feedthrough.

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

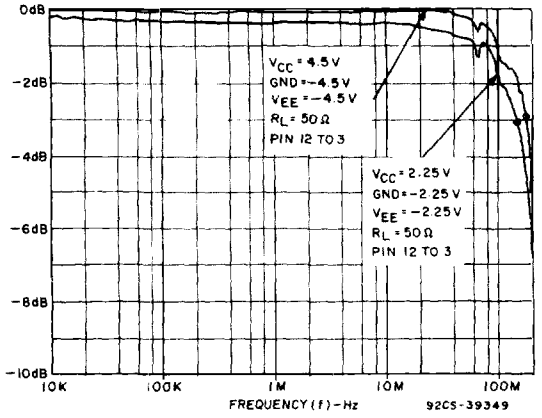


Fig. 14 - Channel on bandwidth (HC/HCT4351).

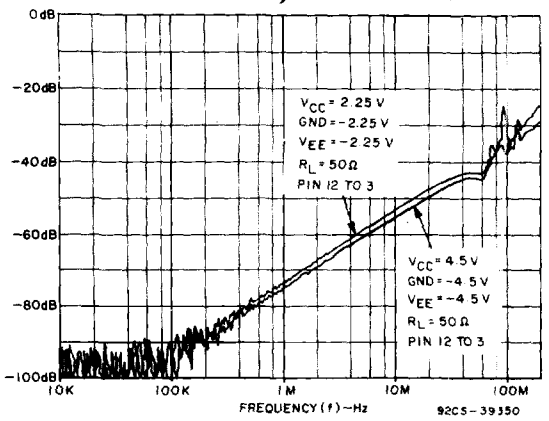


Fig. 15 - Channel off feedthrough (HC/HCT4351).

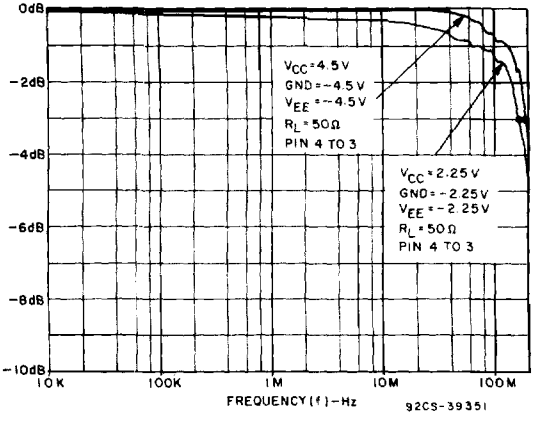


Fig. 16 - Channel on bandwidth (HC/HCT4352).

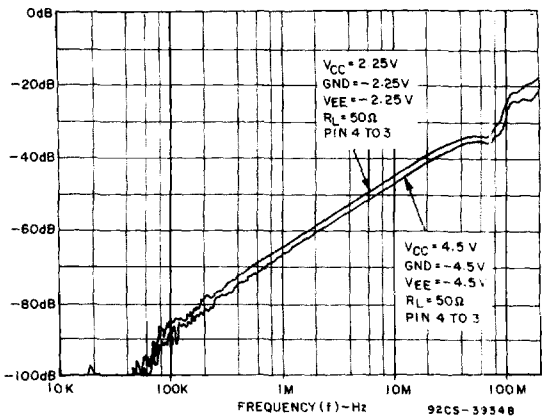


Fig. 17 - Channel off feedthrough (HC/HCT4352).

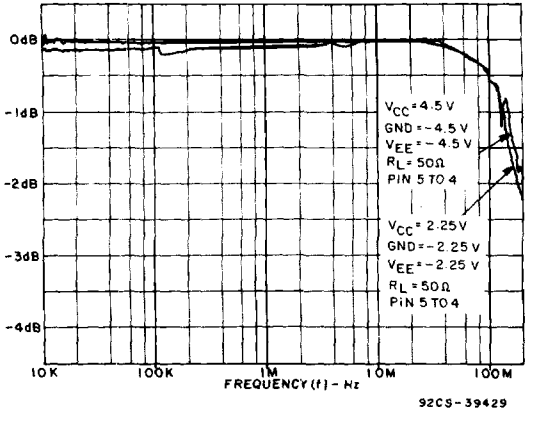


Fig. 18 - Channel on bandwidth (HC/HCT4353).

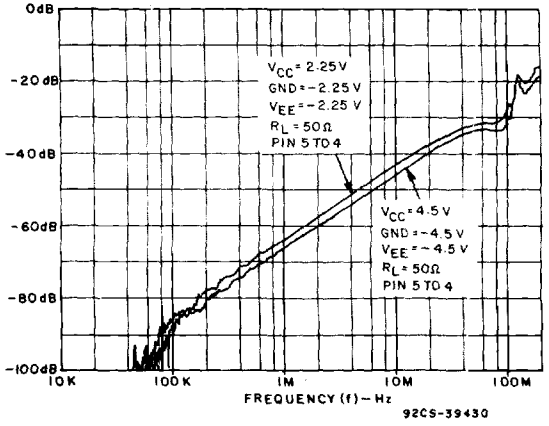


Fig. 19 - Channel off feedthrough (HC/HCT4353).

CD54/74HC4351, CD54/74HCT4351
CD54/74HC4352, CD54/74HCT4352
CD54/74HC4353, CD54/74HCT4353

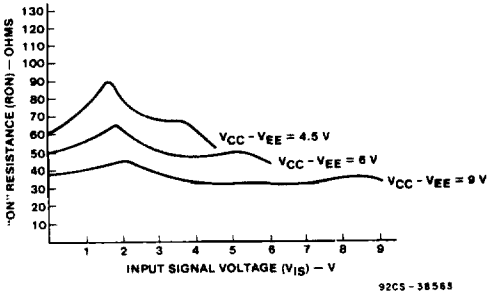
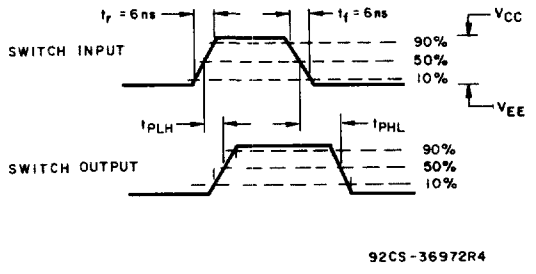
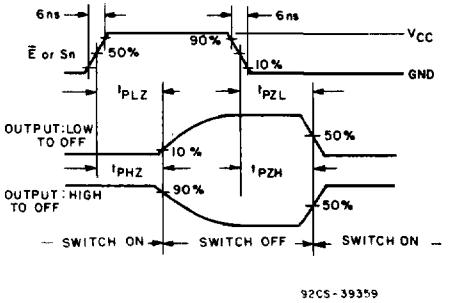


Fig. 20 - Typical ON resistance vs. input signal voltage.





HC4351, HC4352, HC4353

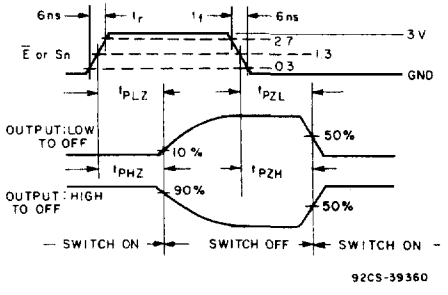


Fig. 21 - Switch propagation delay, turn-on, turn-off times.

HCT4351, HCT4352, HCT4353

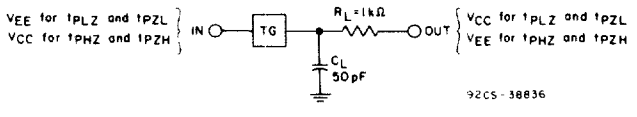


Fig. 22 - Switch on/off propagation delay test circuit.

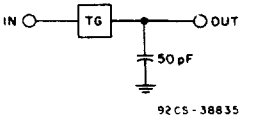


Fig. 23 - Switch In to Switch Out propagation delay test circuit.