

November 2009

FPF1107 / FPF1108 Advance Load Management Switch

Features

- 1.2V to 4V Input Voltage Operating Range
- Typical R_{DS(ON)}:
 - $35m\Omega$ at $V_{IN}=3.3V$
 - $55m\Omega$ at $V_{IN}=1.8V$
 - 85mΩ at V_{IN}=1.2V
- Slew Rate Control with t_R: 130µs
- Output Discharge Function on FPF1108
- Low <1µA Quiescent Current at V_{ON}=V_{IN}
- ESD Protected: Above 4000V HBM, 2000V CDM
- GPIO/CMOS-Compatible Enable Circuitry

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Digital Cameras
- www.DataSheet4U.com
 Advanced Notebook, UMPC, MID
 - Portable Medical Devices
 - GPS and Navigation Equipment

Description

The FPF1107/08 are low R_{DS} P-channel MOSFET load switches of the IntelliMAX $^{\rm TM}$ family. Integrated slew-rate control prevents inrush current from glitch supply rails with capacitive loads common in power applications.

The input voltage range operates from 1.2V to 4V to fulfill today's lowest ultra-portable device supply requirements. Switch control is by a logic input (ON-pin) capable of interfacing directly with low-voltage CMOS control signals and GPIOs in embedded processors.

Ordering Information

Part Number	Part Marking	Switch (Typical) At 1.8V _{IN}	Input Buffer	Output Discharge	ON Pin Activity	t _R	© Eco Status	Package
FPF1107	QC	55mΩ	CMOS	NA	Active HIGH	130µs	Green	4-Ball, Wafer-Level Chip-Scale Package
FPF1108	QD	55mΩ	CMOS	65Ω	Active HIGH	130µs	Green	(WLCSP), 1.0 x 1.0mm, 0.5mm Pitch

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

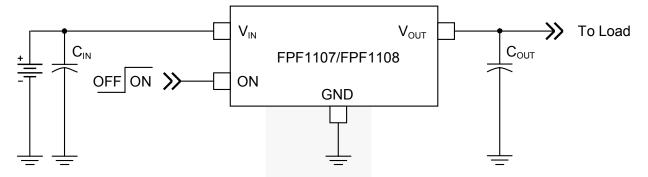


Figure 1. Typical Application

Notes:

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- 1. $C_{IN}=1\mu F$, X5R, 0603, for example Murata GRM185R60J105KE26
- 2. C_{OUT} =1 μ F, X5R, 0805, for example Murata GRM216R61A105KA01

Block Diagram

ON CONTROL LOGIC

ESD protection

FPF1107/8

Output Discharge (Optional)

GND

Figure 2. Block Diagram (Output Discharge for FPF1108 Only)

Pin Configurations



Figure 3. 1 x 1mm WLCSP Bumps Facing Down

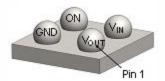


Figure 4. 1 x 1mm WLCSP Bumps Facing Up

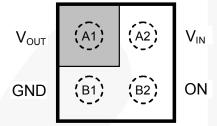


Figure 5. Pin Assignments (Top View)

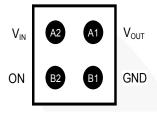


Figure 6. Pin Assignments (Bottom View)

Pin Definitions

Pin#	Name	Description
A1	V _{OUT}	Switch Output
A2	V_{IN}	Supply Input: Input to the Power Switch.
B1	GND	Ground
B2	ON	ON/OFF Control, Active HIGH

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Paramete	Min.	Max.	Unit		
V _{IN}	V _{IN} , V _{OUT} , V _{ON} to GND	-0.3	4.2	V		
I _{SW}	Maximum Continuous Switch Current			1.2	Α	
P_D	Power Dissipation at T _A =25°C			1.0	W	
T _{STG}	Storage Junction Temperature	-65	+150	°C		
T _A	Operating Temperature Range		-40	+85	°C	
0	Thermal Decistance Junation to Ambient	1S2P with 1 Thermal Via		95	°C/W	
Θ_{JA}	Thermal Resistance, Junction-to-Ambient	1S2P without Thermal Via		187		
ESD	Electrostatic Discharge Canability	Human Body Model, JESD22-A114	4		kV	
EGD	Electrostatic Discharge Capability	Charged Device Model, JESD22-C101	2		NV	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.2	4.0	٧
T _A	Ambient Operating Temperature	-40	+85	°C

Electrical Characteristics

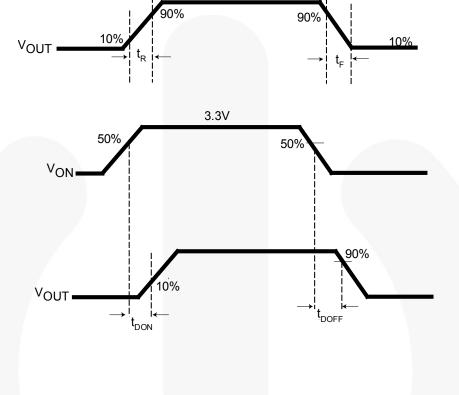
Unless otherwise noted, V_{IN} =1.2 to 4.0V, T_A =-40 to +85°C, typical values are at V_{IN} =3.3V and T_A =25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
Basic Oper	ration					
V _{IN}	Supply Voltage		1.2		4.0	V
I _{Q(OFF)}	Off Supply Current	V _{ON} =GND V _{OUT} =Open, V _{IN} =4V			1	μA
I _{SD(OFF)}	Off Switch Current	V _{ON} =GND V _{OUT} =GND			1	μA
	Quiescent Current	I _{OUT} =0mA, V _{ON} =V _{IN}			1	^
l _Q	Quiescent Current	I _{OUT} =0mA, V _{ON} < V _{IN}			3	μΑ
		V _{IN} =3.3V, I _{OUT} =200mA, T _A =25°C		35	50	mΩ
		V _{IN} =1.8V, I _{OUT} =200mA, T _A =25°C		55	70	
Ron	On Resistance	V _{IN} =1.5V, I _{OUT} =200mA, T _A =25°C		70		
		V _{IN} =1.2V, I _{OUT} =200mA, T _A =25°C		85	150	
		V _{IN} =1.8V, I _{OUT} =200mA, T _A =85°C ⁽³⁾		65	100	ı
R_{PD}	Output Discharge R _{PULL DOWN}	V _{IN} =3.3V, V _{ON} =0V, I _{FORCE} =20mA, T _A =25°C, FPF1108		65	110	Ω
V _{IH}	On Input Logic High Voltage	V _{IN} =1.2V to 4.0V	1.1			V
V _{IL}	On Input Logic Low Voltage	V _{IN} =1.2V to 4.0V			0.35	V
I _{ON}	On Input Leakage	V _{ON} =V _{IN} or GND	-1		1	μA
Dynamic C	haracteristics				'	
t _{DON}	Turn-On Delay ⁽⁴⁾			80		μs
t _R	V _{OUT} Rise Time ⁽⁴⁾	V_{IN} =3.3V, R _L =10 Ω , C _L =0.1 μ F, T _A =25°C, FPF1107/8		130		μs
t _{ON}	Turn-On Time ^(4,6)	14-23 6,111 1107/6		210		μs
t _{DON}	Turn-On Delay ⁽⁴⁾			70	95	μs
t _R	V _{OUT} Rise Time ⁽⁴⁾	V_{IN} =3.3V, R _L =500 Ω , C _L =0.1 μ F, T _A =25°C, FPF1107/8		95	120	μs
ton	Turn-On Time ^(4,6)	14-25 C, 111 1107/6		165	215	μs
FPF1107						
heet4U.com	Turn-Off Delay ⁽⁴⁾		1	2.0	2.5	μs
t _F	V _{OUT} Fall Time ⁽⁴⁾	V_{IN} =3.3V, R _L =10 Ω , C _L =0.1 μ F, - T _A =25°C		2.2		μs
t _{OFF}	Turn-Off ^(4,7)	14-25 C		4.2	, y	μs
t _{DOFF}	Turn-Off Delay ⁽⁴⁾			7.0		μs
t _F	V _{OUT} Fall Time ⁽⁴⁾	V_{IN} =3.3V, R _L =500 Ω , C _L =0.1 μ F, T _A =25°C		110	<i>y</i>	μs
t _{OFF}	Turn-Off ^(4,7)	14-23 0		117		μs
FPF1108 ⁽⁵⁾						
t _{DOFF}	Turn-Off Delay ⁽⁴⁾			2.0	2.5	μs
t _F	V _{OUT} Fall Time ⁽⁴⁾	V _{IN} =3.3V, R _L =10Ω, C _L =0.1μF,		1.9		μs
t _{OFF}	Turn-Off ^(4,7)	_ R _{PD} =65Ω, T _A =25°C		3.9		μs
t _{DOFF}	Turn-Off Delay ⁽⁴⁾			2.5		μs
t _F	V _{OUT} Fall Time ⁽⁴⁾	V _{IN} =3.3V, R _L =500Ω, C _L =0.1μF,		10.6		μs
toff	Turn-Off ^(4,7)	R_{PD} =65 Ω , T_{A} =25°C		13.1		μs

Notes:

- This parameter is guaranteed by design and characterization; not production tested. $t_{\text{DON}}/t_{\text{DOFF}}/t_{\text{R}}/t_{\text{F}}$ are defined in Figure 7. Output discharge path is enabled during off.

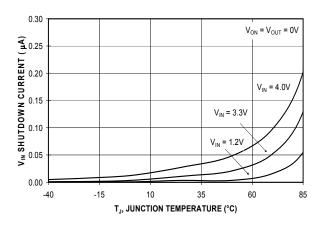
Timing Diagram



Notes:

- 6. $t_{ON}=t_R + t_{DON}$.
- 7. $t_{OFF}=t_F+t_{DOFF}$.

Figure 7. Timing Diagram



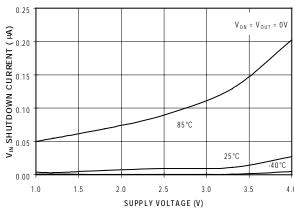
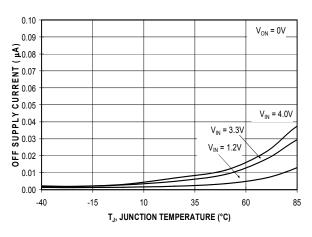
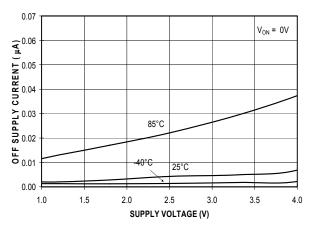


Figure 8. Shutdown Current vs. Temperature

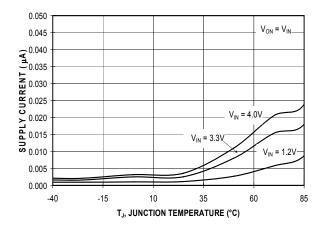
Figure 9. Shutdown Current vs. Supply Voltage





www.DataSheet4Lcom Figure 10. Off Supply Current vs. Temperature (FPF1107, VOUT is Floating)

Figure 11. Off Supply Current vs. Supply Voltage (FPF1107, VOUT is Floating)



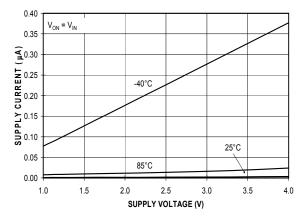


Figure 12. Quiescent Current vs. Temperature $(V_{ON}=V_{IN})$

Figure 13. Quiescent Current vs. Supply Voltage

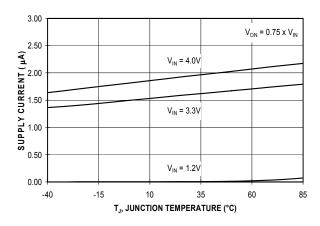


Figure 14. Quiescent Current vs. Temperature (V_{oN}=0.75 x V_{IN})

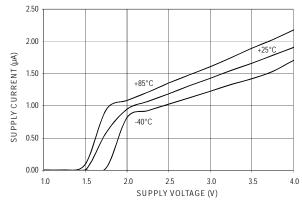


Figure 15. Quiescent Current vs. Supply Voltage at V_{ON} =1.2V

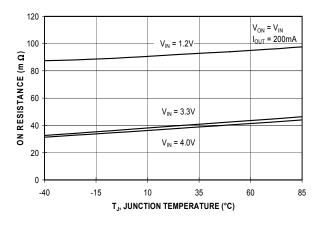


Figure 16. Ron vs. Temperature

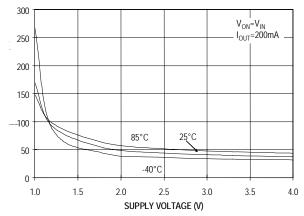


Figure 17. Ron vs. Supply Voltage

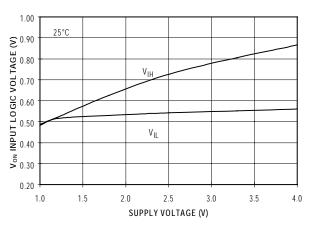


Figure 18. ON-Pin Threshold vs. VIN

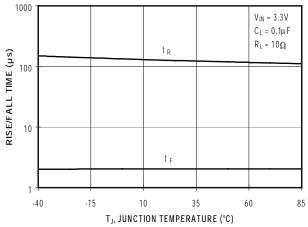
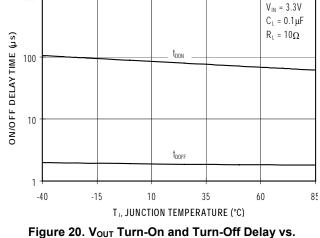


Figure 19. V_{OUT} Rise and Fall Time vs. Temperature at $R_L {=} 10\Omega$



1000

Figure 20. V_{OUT} Turn-On and Turn-Off Delay vs Temperature at R_L =10 Ω

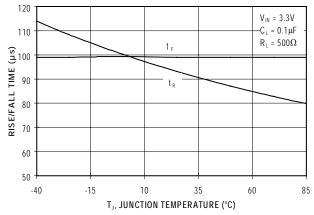


Figure 21. V_{OUT} Rise and Fall Time vs. Temperature at R_I =500Ω

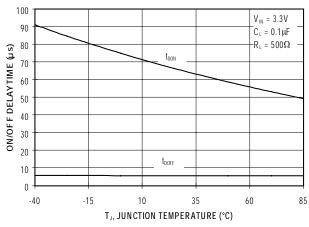


Figure 22. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at $R_1 = 500\Omega$

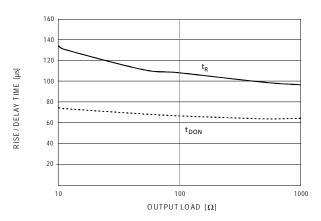


Figure 23. V_{OUT} Turn-On and Turn-Off Delay vs. Output Load at V_{IN} =3.3V

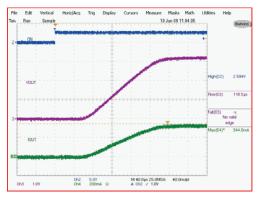


Figure 24. Turn-On Response (V_{IN}=3.3V, C_{IN}=1 μ F, C_{OUT}=0.1 μ F, R_L=10 Ω)

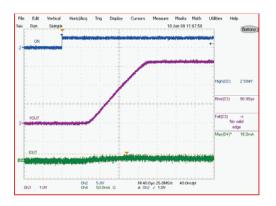


Figure 26. Turn-On Response $(V_{IN}=3.3V, C_{IN}=1\mu F, C_{OUT}=0.1\mu F, R_L=500\Omega)$

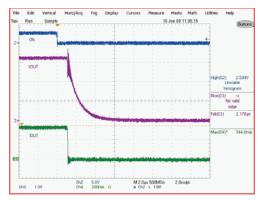


Figure 25. Turn-Off Response (V_{IN}=3.3V, C_{IN}=1 μ F, C_{OUT}=0.1 μ F, R_L=10 Ω)

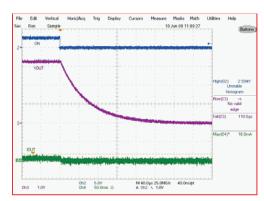


Figure 27. Turn-Off Response (FPF1107 – No Output Pull-Down Resistor) (V_{IN} =3.3V, C_{IN} =1 μ F, C_{OUT} =0.1 μ F, R_L =500 Ω)

Application Information

Input Capacitor

The IntelliMAXTM switch doesn't require input capacitor. To reduce device inrush current effect, a $0.1\mu F$ ceramic capacitor, C_{IN} , is recommended close to the VIN pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

The IntelliMAXTM switch works without an output capacitor. However, if parasitic board inductance forces V_{OUT} below GND when switching off, a $0.1\mu F$ capacitor, C_{OUT} , should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on RC constant of external components as follows:

$$t_{\mathsf{F}} = \mathsf{R}_{\mathsf{L}} \times \mathsf{C}_{\mathsf{L}} \times 2.2 \tag{1}$$

where t_{F} is 90% to 10% fall time, R_{L} is output load and C_{L} is output capacitor.

The same equation works for a device with a pull-down output resistor, then R_L is replaced by a parallel connected pull-down and external output resistor combination, as follows:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \tag{2}$$

where t_F is 90% to 10% fall time, R_L is output load, $R_{PD}{=}65\Omega$ is output pull-down resistor, and C_L is the output capacitor.

Resistive Output Load

If resistive output load is missing, the IntelliMAXTM switch without pull-down output resistor is not discharging output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

Recommended Land Pattern and Layout

For best thermal performance and minimal inductance and parasitic effects, it is recommended to keep input and output traces short and capacitors as close to the device as possible. Below is a recommended layout for this device to achieve optimum performance.

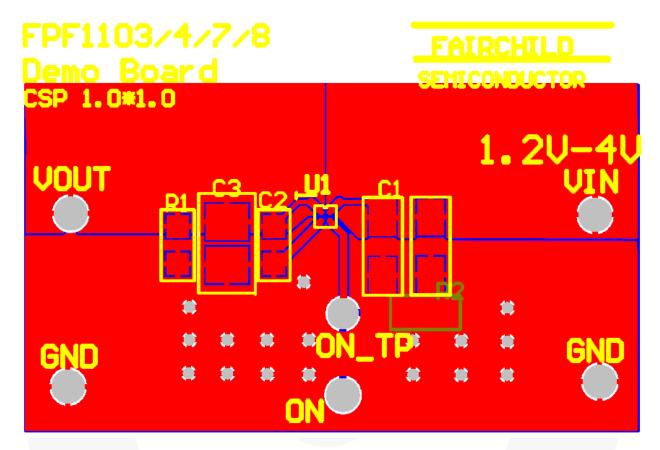
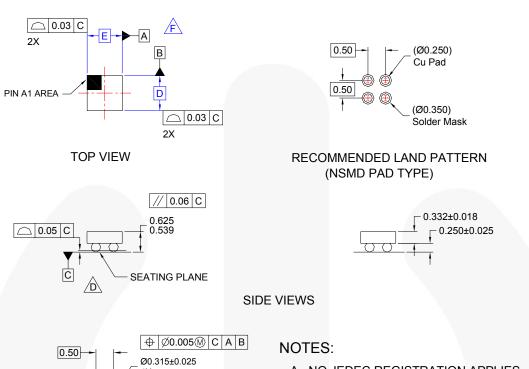


Figure 28. Recommended Land Pattern and Layout

Physical Dimensions



BOTTOM VIEW

0.50

В

(Y)±0.018

 $(X)\pm0.018$

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- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
 - E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILENAME: MKT-UC004ABrev2.

Figure 29. 4 Ball, 1.0 x 1.0mm Wafer Level Chip Scale WLCSP Packaging

Product-Specific Dimensions

Product	D	E	X	Y
FPF1107	960µm ± 30µm	960µm ± 30µm	0.230mm	0.230mm
FPF1108	960um ± 30µm	960um ± 30μm	0.230mm	0.230mm

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Definition of Terms

Datasheet Identification	Product Status	Definition		
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.		
Preliminary	First Production	Data sheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.		
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.		
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.		

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