



GoldStar
GOLDSTAR ELECTRON CO., LTD.

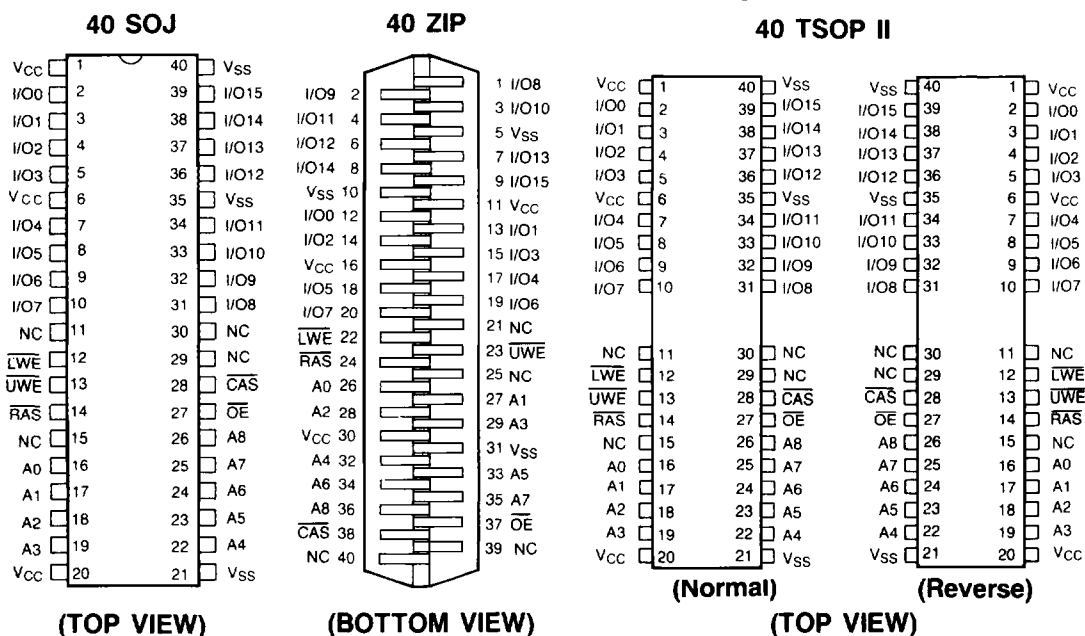
GM71C4270A/AL GM71CS4270A/AL

262,144 WORDS×16BIT
CMOS DYNAMIC RAM

Description

The GM71C4270A/AL is the new generation dynamic RAM organized 262,144×16 Bit. GM71C4270A/AL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4270A/AL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C4270A/AL to be packaged in standard 400 mil 40 pin plastic SOJ, standard 475 mil 40 pin plastic ZIP, and standard 400 mil 40 pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Pin Configuration



Features

- 262,144 Words×16 Bit Organization
- Fast Page Mode Capability
- Single Power Supply (5V ± 10%)
- Fast Access Time & Cycle Time (Unit: ns)

	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}
GM71C4270A/AL-70	70	15	110	40
GM71C4270A/AL-80	80	20	130	45
GM71C4270A/AL-100	100	20	150	50

- Low Power
Active: 825/770/688 mW (MAX)
Standby: 5.5mW (CMOS level: MAX)
1.1mW (L-series)
- RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms
- 512 Refresh Cycles/128ms (L-series)
- Battery Back Up Operation (L-series)
- 2 WE byte Control
- Self-Refresh Operation (GM71CS4270A/AL)

Pin Description

Pin	Function	Pin	Function
A0 ~ A8	Address Input	$\overline{\text{UWE/LWE}}$	Read/Write Enable
A0 ~ A8	Refresh Address Inputs	$\overline{\text{OE}}$	Output Enable
I/O0-I/O15	Data-in/Data-out	V _{CC}	Power (+5V)
$\overline{\text{RAS}}$	Row Address Strobe	V _{SS}	Ground
$\overline{\text{CAS}}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	PKG
GM71C4270AJ/ALJ-70 GM71C4270AJ/ALJ-80 GM71C4270AJ/ALJ-10	70ns 80ns 100ns	400 Mil 40 Pin Plastic SOJ
GM71C4270AZ/ALZ-70 GM71C4270AZ/ALZ-80 GM71C4270AZ/ALZ-10	70ns 80ns 100ns	475 Mil 40 Pin Plastic ZIP
GM71C4270AT/ALT-70 GM71C4270AT/ALT-80 GM71C4270AT/ALT-10	70ns 80ns 100ns	400 Mil 40 Pin Plastic TSOP II (Normal Type)
GM71C4270AR/ALR-70 GM71C4270AR/ALR-80 GM71C4270AR/ALR-10	70ns 80ns 100ns	400 Mil 40 Pin Plastic TSOP II (Reverse Type)
GM71CS4270AZ/ALZ-70 GM71CS4270AZ/ALZ-80 GM71CS4270AZ/ALZ-10	70ns 80ns 100ns	400 Mil 40 Pin Plastic SOJ
GM71CS4270AT/ALT-70 GM71CS4270AT/ALT-80 GM71CS4270AT/ALT-10	70ns 80ns 100ns	475 Mil 40 Pin Plastic ZIP
GM71CS4270AJ/ALJ-70 GM71CS4270AJ/ALJ-80 GM71CS4270AJ/ALJ-10	70ns 80ns 100ns	400 Mil 40 Pin Plastic TSOP II (Normal Type)
GM71CS4270AR/ALR-70 GM71CS4270AR/ALR-80 GM71CS4270AR/ALR-10	70ns 80ns 100ns	400 Mil 40 Pin Plastic TSOP II (Reverse Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	°C
T _{STG}	Storage Temperature (Plastic)	- 55 ~ 125	°C
V _{IN} /V _{OUT}	Voltage on any Pin Relative to V _{SS}	- 1.0 ~ 7.0	V
V _{CC}	Voltage on V _{CC} Relative to V _{SS}	- 1.0 ~ 7.0	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Condition (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	—	6.5	V
V _{IL}	Input Low Voltage (I/O Pin)	- 1.0	—	0.8	V
V _{IL}	Input Low Voltage (Others)	- 2.0	—	0.8	V

Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LWE}}$	$\overline{\text{UWE}}$	$\overline{\text{CAS}}$	$\overline{\text{OE}}$	I/O0-I/O7	I/O8-I/O15	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	H	H	L	L	D _{OUT}	D _{OUT}	Word Read
L	L	H	L	H	D _{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	H	H	L	H	High-Z	High-Z	
H to L	—	—	L	—	High-Z	High-Z	CBR Refresh or Self Refresh

DC Electrical Characteristics: ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC \min}$)	70ns	—	150	mA 1,2
		80ns	—	140	
		100ns	—	125	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} = V_{IH}$, $D_{OUT} = \text{High-Z}$)	—	2	mA	
I_{CC3}	$\overline{RAS}$ -Only Refresh Current Average Power Supply Current ($t_{RC} = t_{RC \min}$)	70ns	—	140	mA 2
		80ns	—	130	
		100ns	—	110	
I_{CC4}	Fast Page Mode Current Average Power Supply Current ($t_{PC} = t_{PC \min}$)	70ns	—	130	mA 1,3
		80ns	—	120	
		100ns	—	110	
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE} \geq V_{CC} - 0.2V$, $D_{OUT} = \text{High-Z}$)	—	1	mA	
		—	200	μA	
I_{CC6}	$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Current ($t_{RC} = t_{RC \min}$)	70ns	—	140	mA 2
		80ns	—	130	
		100ns	—	110	
I_{CC7}	Battery Back Up Current (Standby with CBR Refresh) ($t_{RC} = 250\mu s$, $t_{RAS} \leq 1\mu s$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE} = V_{IH}$, $\overline{CAS} = V_{IL}$, $D_{OUT} = \text{High-Z}$)	—	300	μA	4,5
I_{CC8}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	—	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{CAS} \leq 0.2V$, $D_{OUT} = \text{High-Z}$)	GM71CS4270A	1	mA	6
		GM71CS4270AL	200	μA	
I_{IL1}	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 6.5V$)	-10	10	μA	
I_{OL1}	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 6.5V$)	-10	10	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC} (\max)$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

4. $V_{IH} \geq V_{CC} - 0.2V$, $0 \leq V_{IL} \leq 0.2V$, Address can be changed once or loss while $\overline{RAS} = V_{IL}$.

5. L-Series.

6. Self-refresh series (GM71CS4270A/AL)

7. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	5	pF	1
C_{I2}	Input Capacitance (Clocks)	—	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	—	10	pF	1,2

Note 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable D_{OUT} .

AC Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ C$, Notes 1, 14, 15, 17, 18)

Test Conditions

Input rise and fall times: 5ns

Input timing reference levels: 0.8V, 2.4V

Output load: 2 TTL gate + C_L (100pF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C4270A/AL-70 GM71CS4270A/AL-70		GM71C4270A/AL-80 GM71CS4270A/AL-80		GM71C4270A/AL-10 GM71CS4270A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	150	—	180	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	60	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	22
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	ns	
t_{CRP}	CAS to $\overline{RAS}$ Precharge Time	15	—	15	—	15	—	ns	23
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	20	—	25	—	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	0	—	ns	
t_{DZC}	$\overline{CAS}$ Set-up Time from D_{IN}	0	—	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	8	—	8	—	8	ms	
	Refresh Period (L-Series)	—	128	—	128	—	128	ms	

Read Cycle

Symbol	Parameter	GM71C4270A/AL-70 GM71CS4270A/AL-70		GM71C4270A/AL-80 GM71CS4270A/AL-80		GM71C4270A/AL-10 GM71CS4270A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	—	70	—	80	—	100	ns	2,3
t _{CAC}	Access Time from $\overline{\text{CAS}}$	—	20	—	20	—	25	ns	3,4,13
t _{AA}	Access Time from Address	—	35	—	40	—	45	ns	3,5,13
t _{OAC}	Access Time from $\overline{\text{OE}}$	—	20	—	20	—	25	ns	3,22
t _{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	20
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	—	0	—	0	—	ns	16,19
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	0	—	0	—	0	—	ns	16,19
t _{RA1}	Column Address to $\overline{\text{RAS}}$ Lead Time	35	—	40	—	45	—	ns	
t _{OFF1}	Output Buffer Turn-off Time	0	15	0	15	—	20	ns	6
t _{OFF2}	Output Buffer Turn-off to $\overline{\text{OE}}$	0	15	0	15	0	20	ns	6
t _{CDD}	$\overline{\text{CAS}}$ to $\overline{\text{DIN}}$ Delay Time	15	—	15	—	20	—	ns	

Write Cycle

Symbol	Parameter	GM71C4270A/AL-70 GM71CS4270A/AL-70		GM71C4270A/AL-80 GM71CS4270A/AL-80		GM71C4270A/AL-10 GM71CS4270A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10,19
t _{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	20
t _{WP}	Write Command Pulse Width	10	—	10	—	20	—	ns	21
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	20	—	20	—	25	—	ns	21
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	20	—	20	—	25	—	ns	21
t _{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11,21
t _{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11,21
t _{COD}	$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ Delay Time	—	0	—	0	—	0	ns	22

Read-Modify-Write Cycle

Symbol	Parameter	GM71C4270A/AL-70 GM71CS4270A/AL-70		GM71C4270A/AL-80 GM71CS4270A/AL-80		GM71C4270A/AL-10 GM71CS4270A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RWC}	Read-Modify-Write Cycle Time	180	—	200	—	245	—	ns	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	95	—	105	—	135	—	ns	10,19
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	45	—	45	—	60	—	ns	10,19
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	60	—	65	—	80	—	ns	10,19
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	20	—	20	—	25	—	ns	21

Refresh Cycle

Symbol	Parameter	GM71C4270A/AL-70 GM71CS4270A/AL-70		GM71C4270A/AL-80 GM71CS4270A/AL-80		GM71C4270A/AL-10 GM71CS4270A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	10	—	10	—	10	—	ns	
t _{CPN}	$\overline{\text{CAS}}$ Precharge Time in Normal Mode	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C4270A/AL-70 GM71CS4270A/AL-70		GM71C4270A/AL-80 GM71CS4270A/AL-80		GM71C4270A/AL-10 GM71CS4270A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{PC}	Fast Page Mode Cycle Time	45	—	50	—	55	—	ns	
t _{CP}	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	10	—	10	—	10	—	ns	
t _{RASC}	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	—	40	—	45	—	50	ns	3,13
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	40	—	45	—	50	—	ns	
t _{CPW}	Fast Page Mode Read-Modify-Write Cycle $\overline{\text{CAS}}$ Precharge to $\overline{\text{UWE}}$, $\overline{\text{LWE}}$ Delay Time	65	—	70	—	85	—	ns	21
t _{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95	—	100	—	110	—	ns	

Self-Refresh Mode

Symbol	Parameter	GM71CS4270A/AL-70		GM71CS4270A/AL-80		GM71CS4270A/AL-10		Note
		Min	Max	Min	Max	Min	Max	
t _{RAS}	RAS Pulse Width (Self Refresh)	100	—	100	—	100	—	
t _{RPS}	RAS Precharge Time (Self-Refresh)	130	—	150	—	180	—	
t _{CHS}	CAS Hold Time (Self-Refresh)	-50	—	-50	—	-50	—	

Notes:

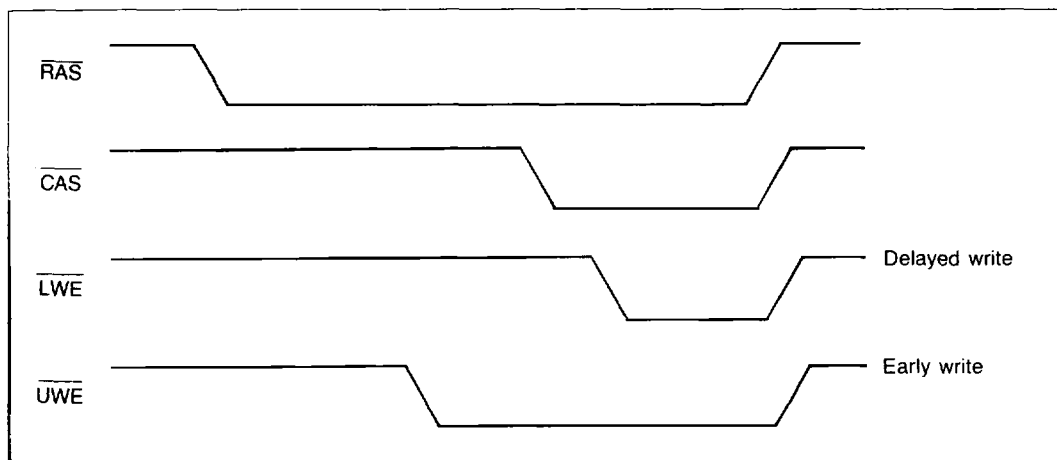
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{TRWD}, t_{TCWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{TRWD} \geq t_{TRWD}(\text{min})$, $t_{TCWD} \geq t_{TCWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RAS} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. After power up pause for 100 μ s, then DRAM initialization requires a minimum of eight $\overline{\text{RAS}}$ -only refresh or eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles. If the user will implement $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ timing in their system, then the eight initialization cycles MUST be $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycles.
15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
16. Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
17. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.
18. A word of data can be written only when $\overline{\text{LWE}}$ and $\overline{\text{UWE}}$ go low at the same time. This implies that early write cycles cannot be combined with delayed write cycles in the same cycles because all data is latched at the fall of the first $\overline{\text{WE}}$. In other words, staggering the $\overline{\text{WE}}$ signals in one cycles is not permitted.
19. t_{TRCH}, t_{TRRH}, t_{WCS}, t_{TRWD}, t_{TCWD} and t_{AWD} are determined by the earlier falling edge of $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$.
20. t_{WCH} and t_{TRCS} are determined by the later rising edge of $\overline{\text{UWE}}$ or $\overline{\text{LWE}}$.
21. t_{WP}, t_{RWL}, t_{CWL}, t_{OEHL}, t_{DS}, t_{DH} and t_{CPW} should be satisfied by both $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$.

22. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH}(\min)/V_{IL}(\max)$ level.
23. t_{CRP} is planned to be improved to match the standard DRAM specifications.
24. If you use distributed CBR refresh mode with $15.6\mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6\mu s$ immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with $15.6\mu s$ interval should be executed within 8ms immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

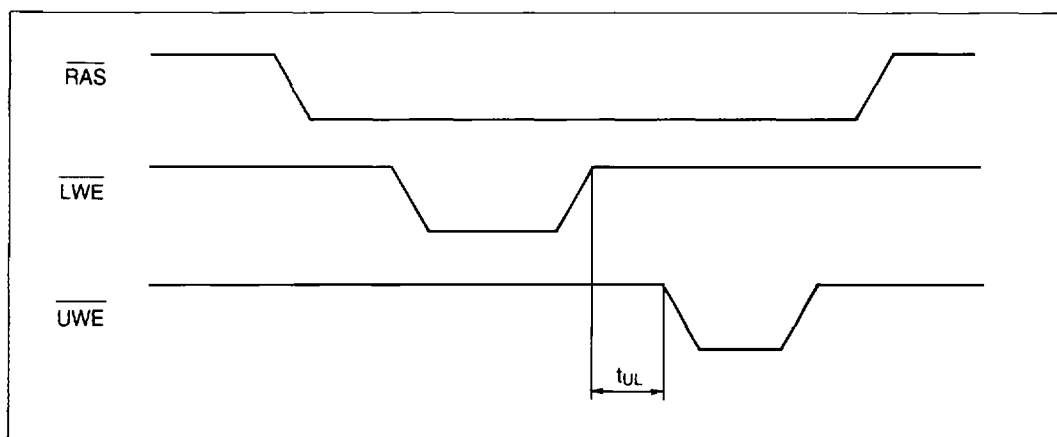
Notes concerning $\overline{2WE}$ control

Please do not separate the $\overline{UWE}/\overline{LWE}$ operation timing intentionally. However skew between $\overline{UWE}/\overline{LWE}$ are allowed under the following conditions.

- 1) Each of the $\overline{UWE}/\overline{LWE}$ should satisfy the timing specifications individually.
- 2) Different operation mode for upper/lower byte is not allowed; such as following.



- 3) Closely separated upper/lower byte control is not allowed. Unless the condition ($t_{CP} \leq t_{UL}$) is satisfied.



TIMING WAVEFORMS

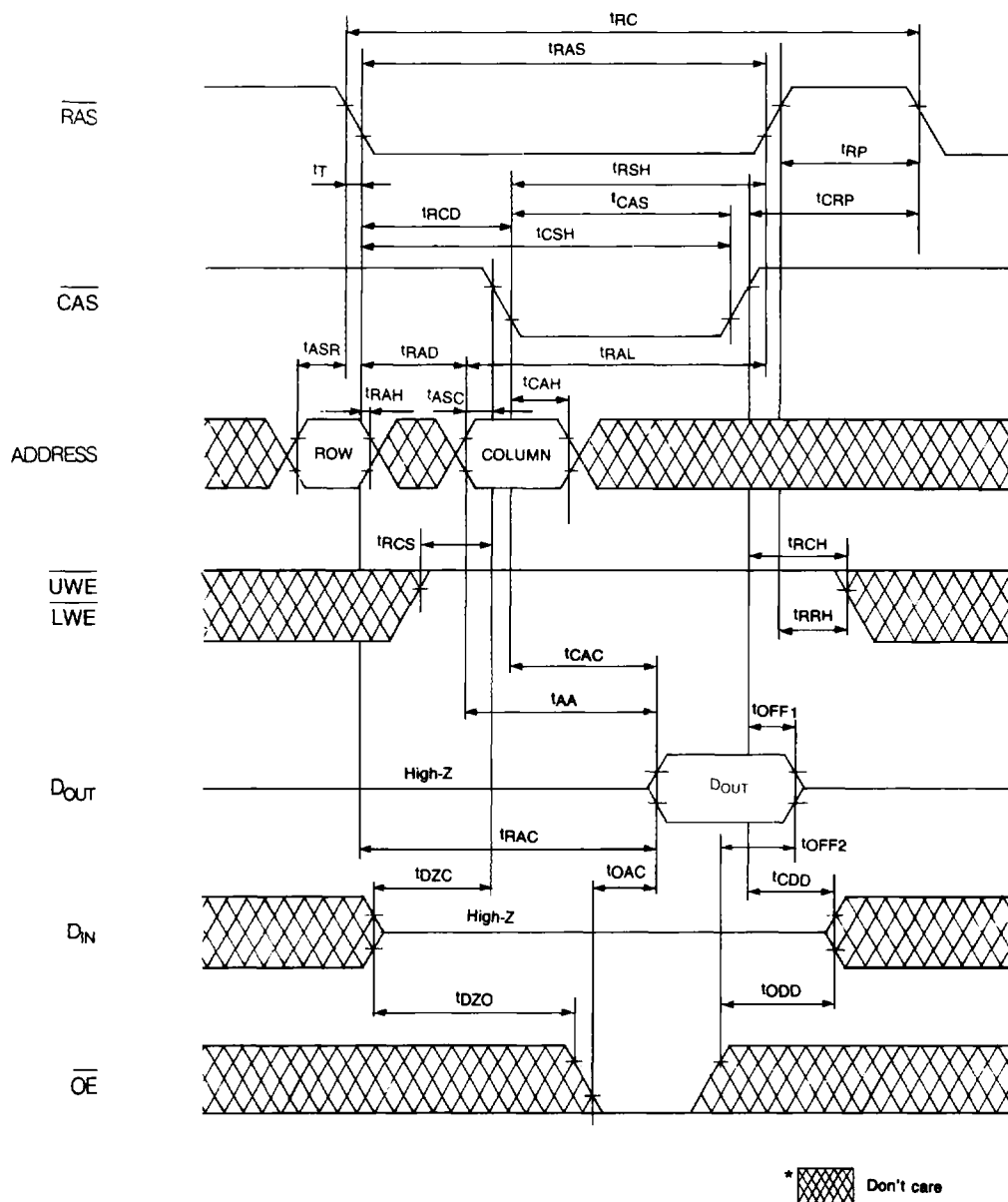


FIGURE 1. READ CYCLE

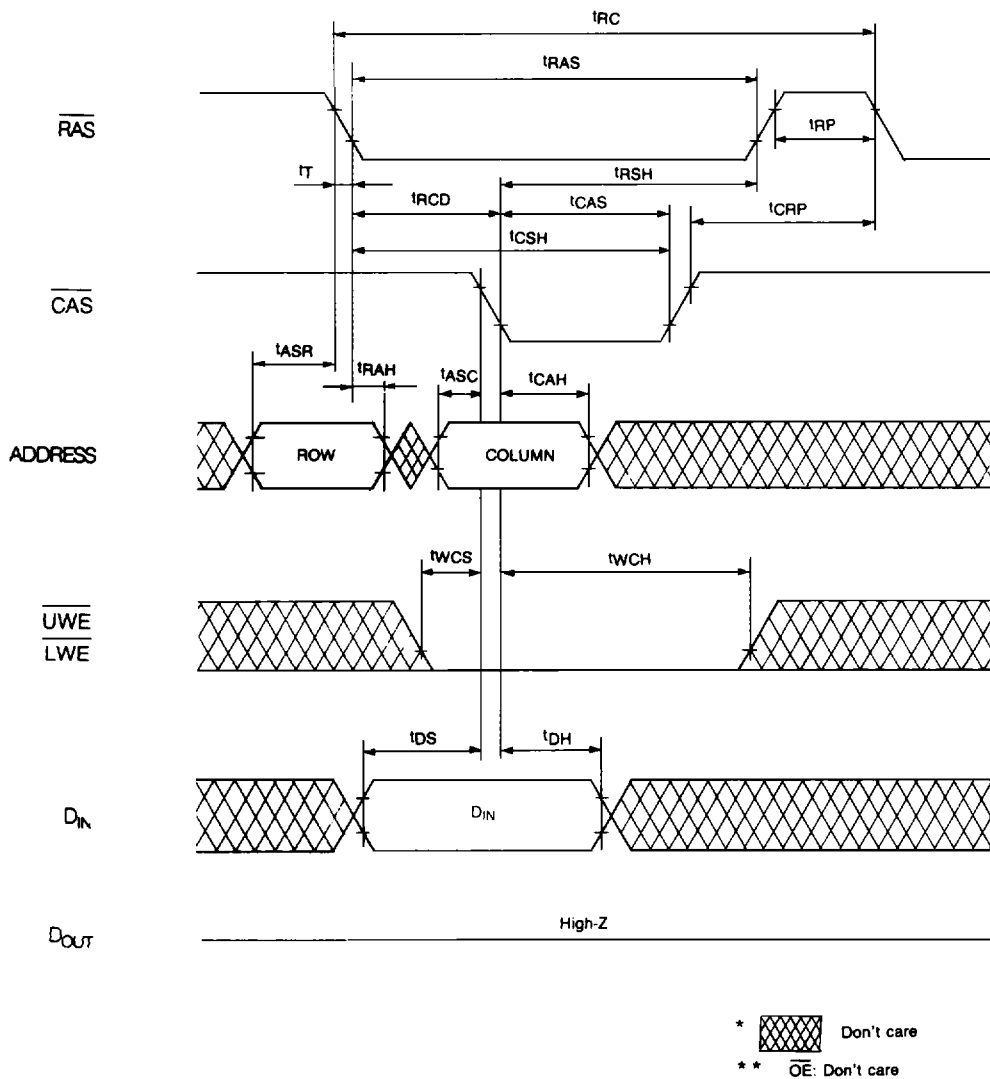


FIGURE 2. EARLY WRITE CYCLE

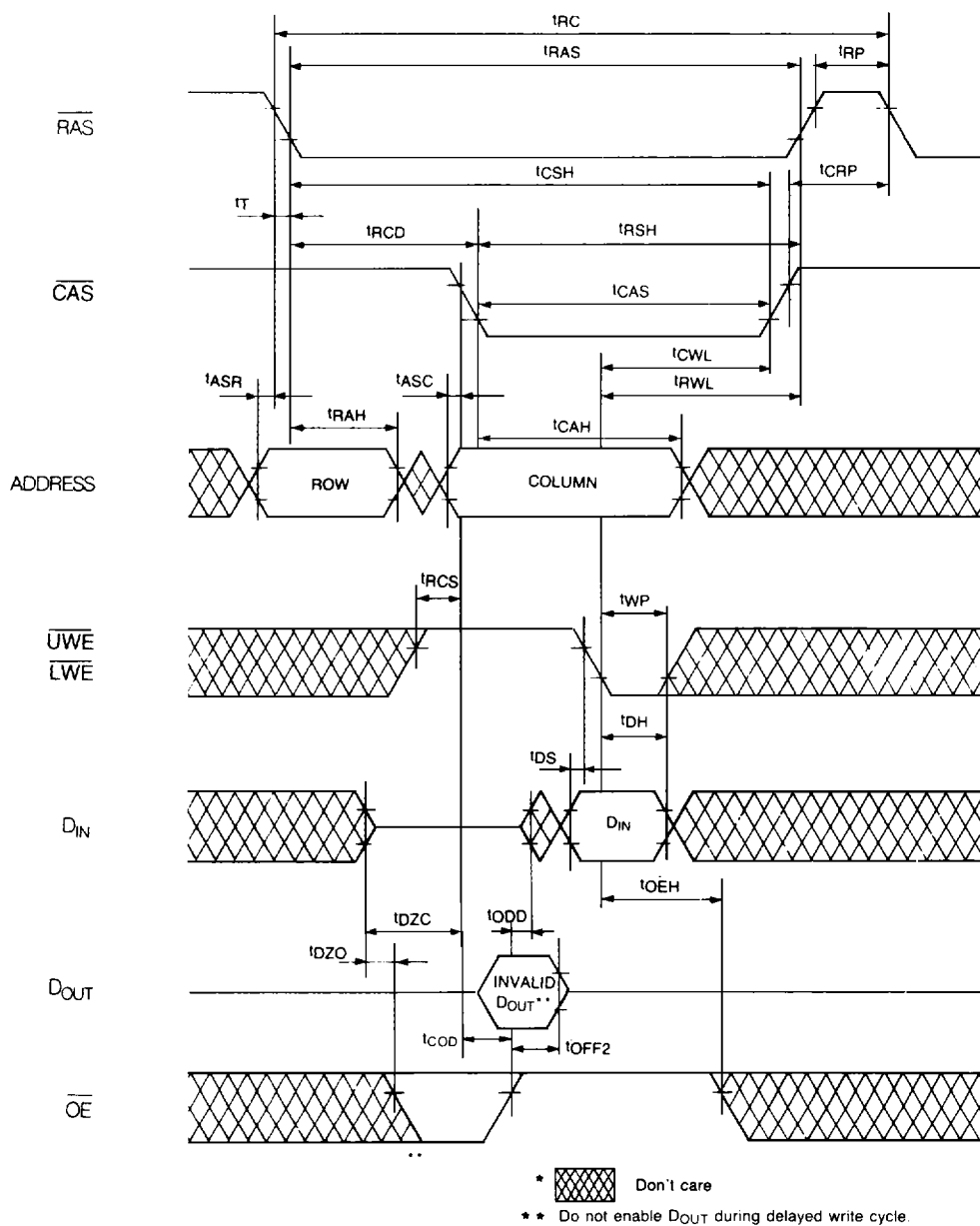


FIGURE 3. DELAYED WRITE CYCLE



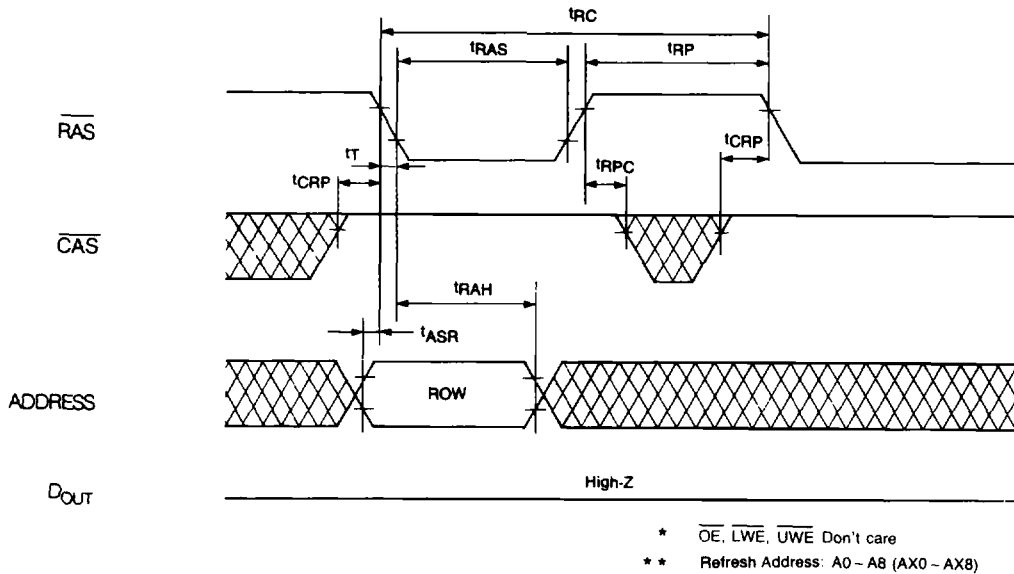


FIGURE 5. $\overline{\text{RAS}}$ -ONLY REFRESH CYCLE

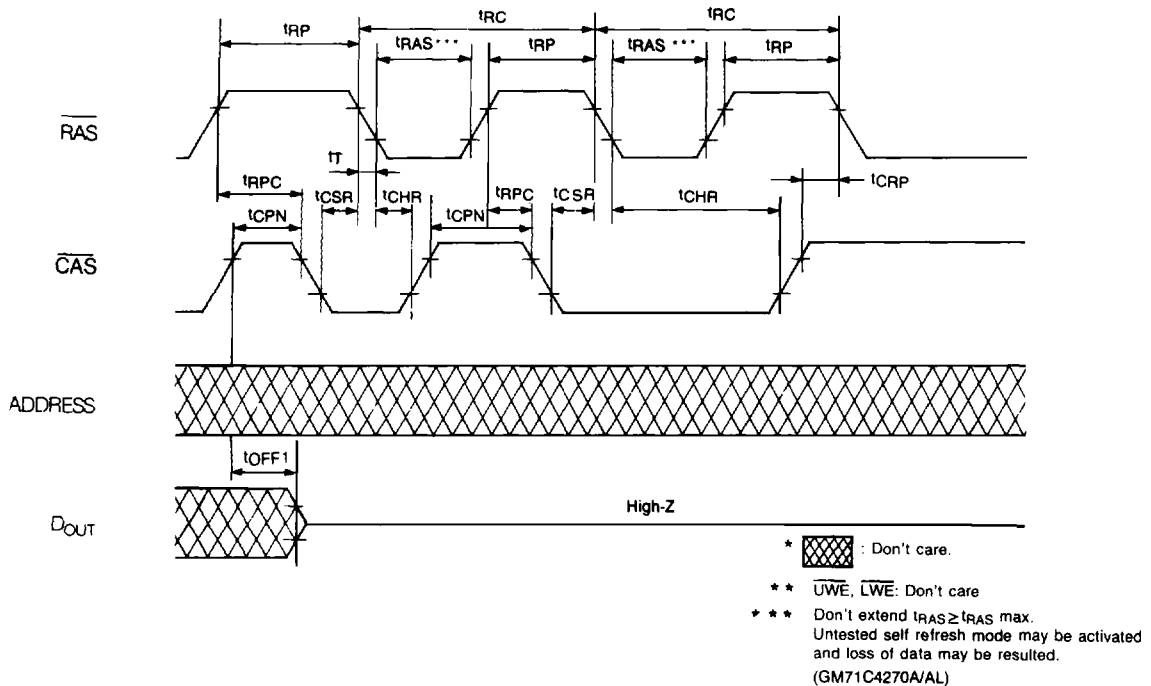


FIGURE 6. CAS-BEFORE-RAS REFRESH CYCLE

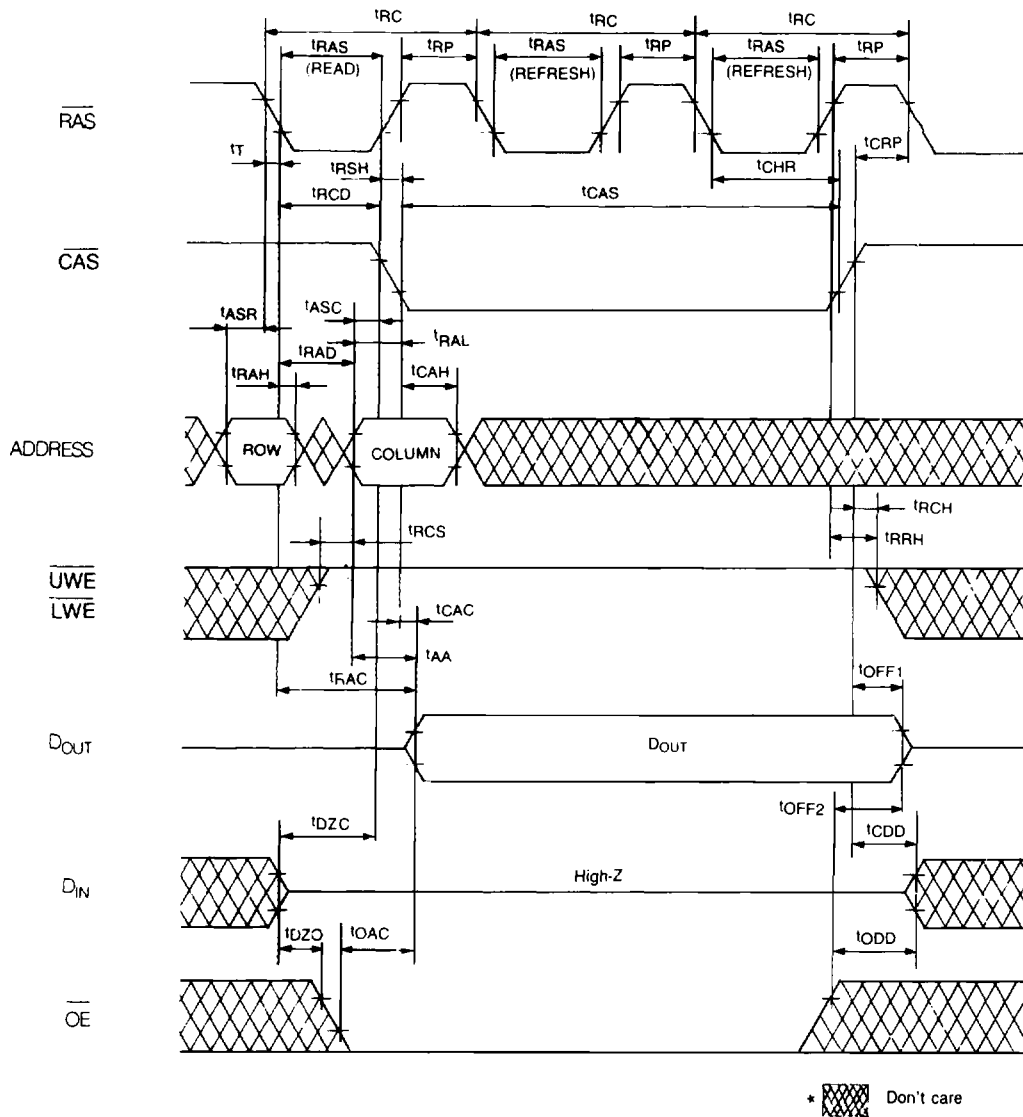


FIGURE 7. HIDDEN REFRESH CYCLE



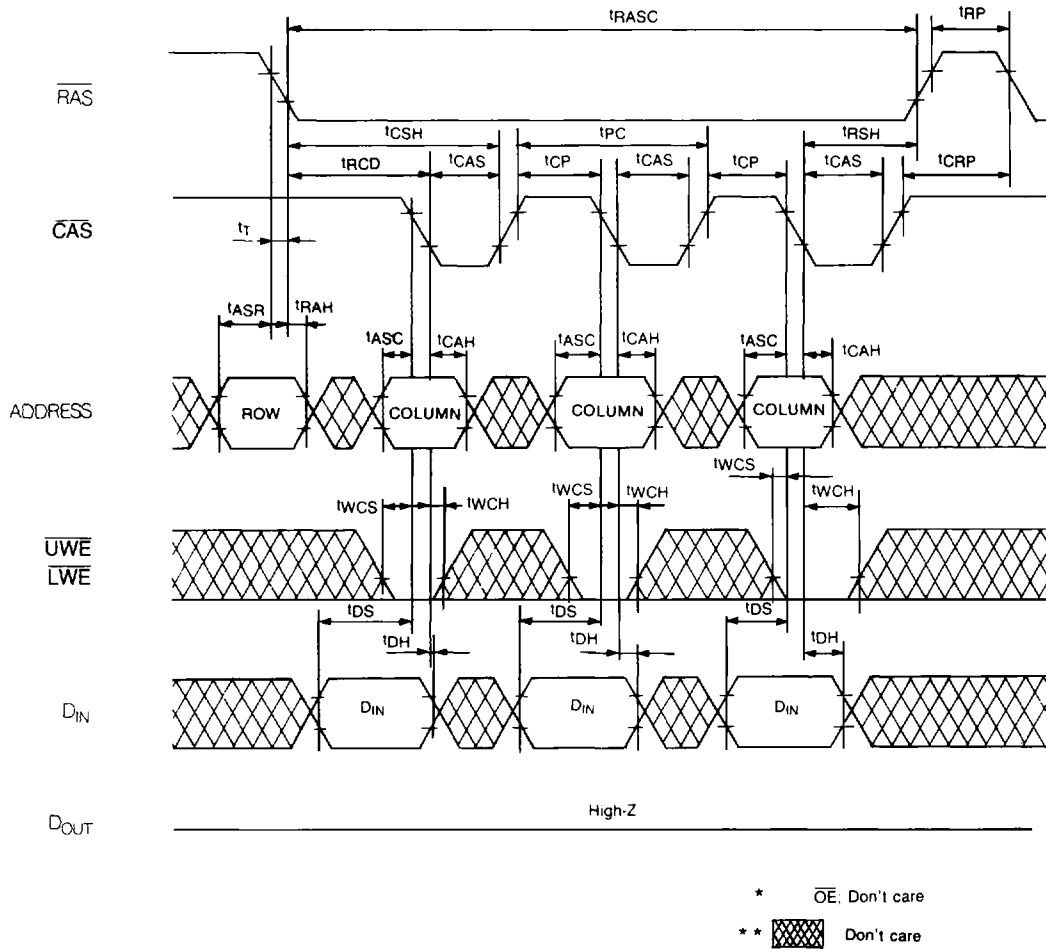


FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

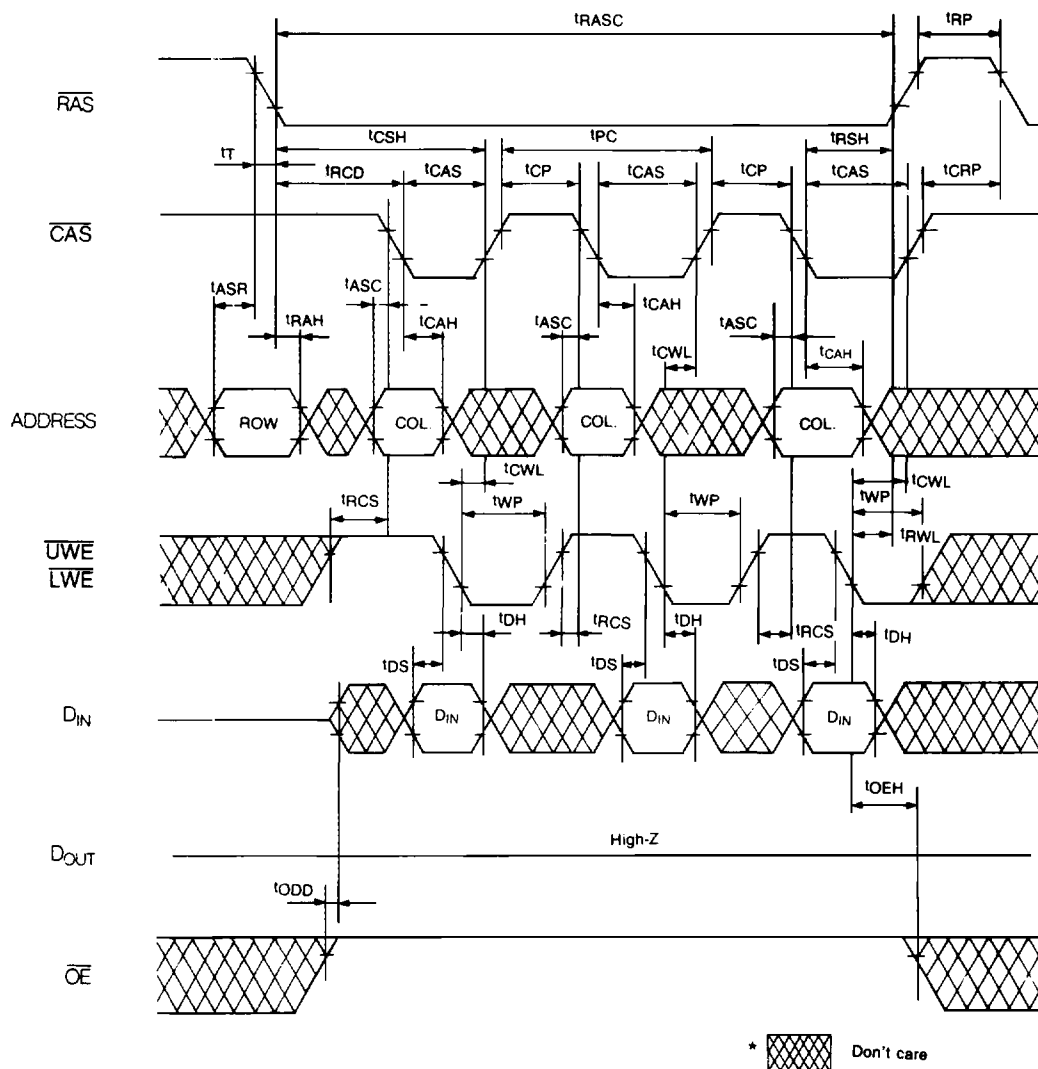


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

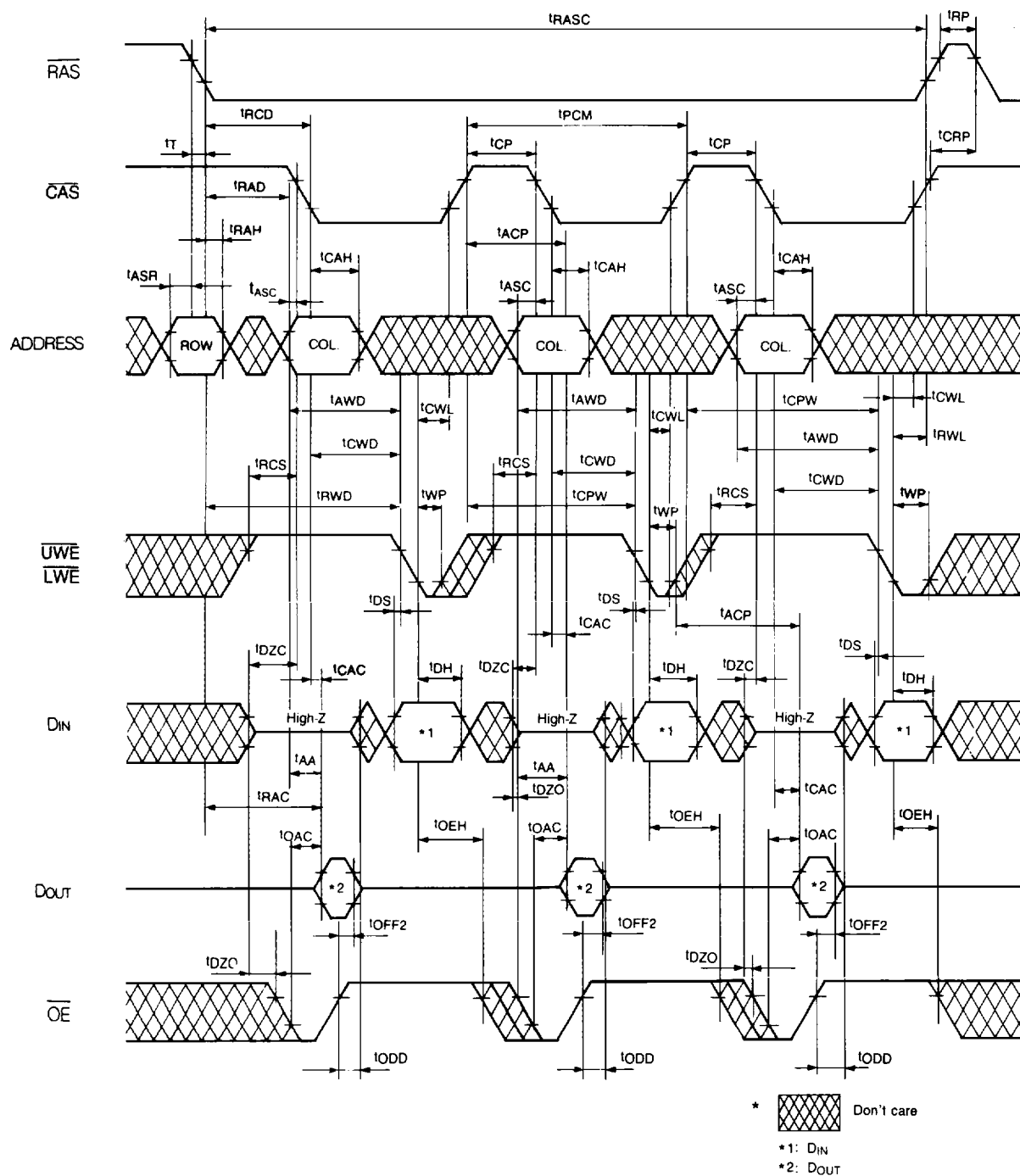
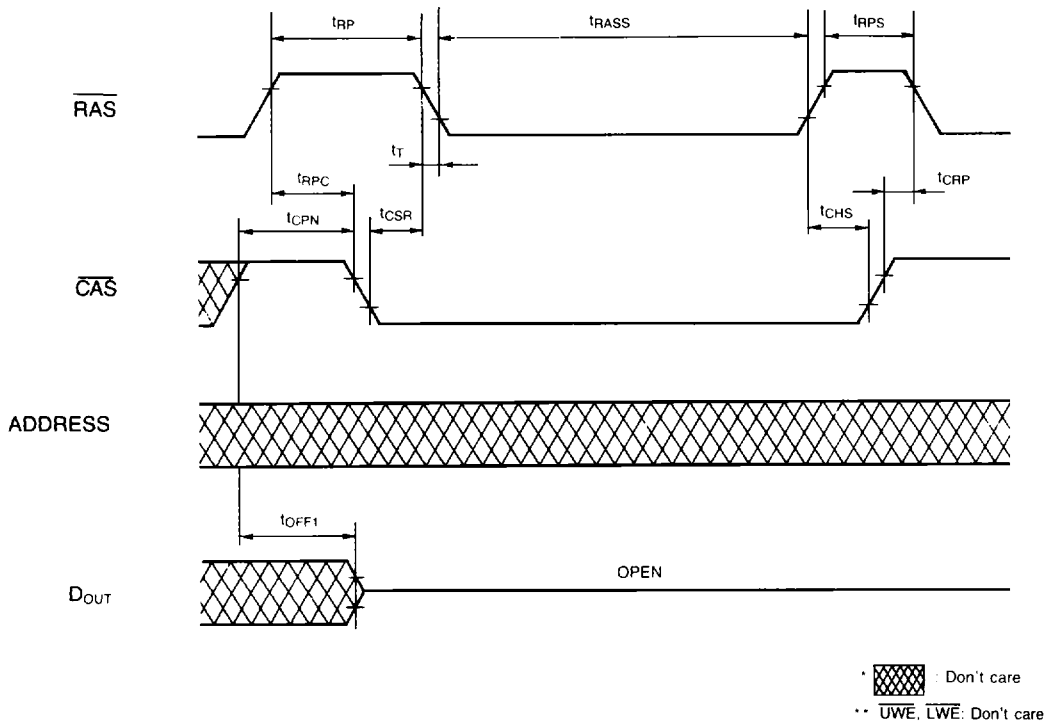


FIGURE 11. FAST PAGE MODE READ-MODIFY-WRITE CYCLE



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

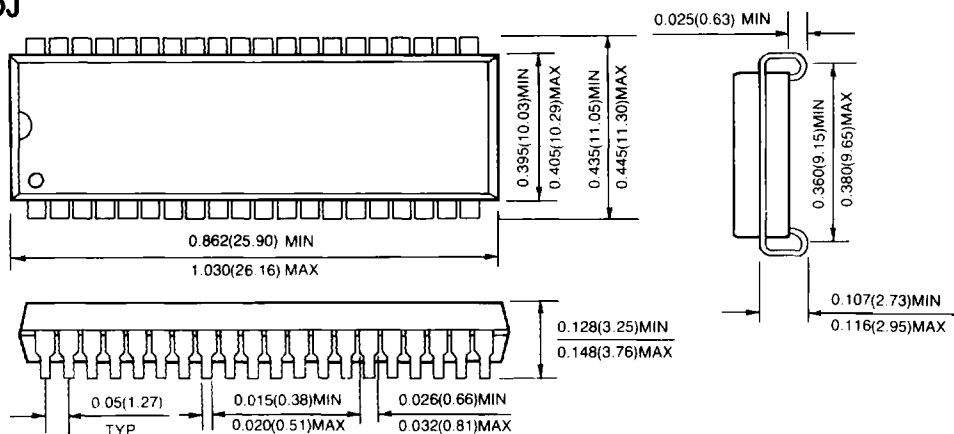
1. Please do not use t_{RASS} timing, $10\mu\text{s} \leq t_{\text{RASS}} \leq 100\mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} \geq 100\mu\text{s}$, the $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .
2. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with $15.6\mu\text{s}$ interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6\mu\text{s}$ interval in normal read/write cycle, CBR refresh should be executed within $15.6\mu\text{s}$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

FIGURE 12. SELF REFRESH CYCLE

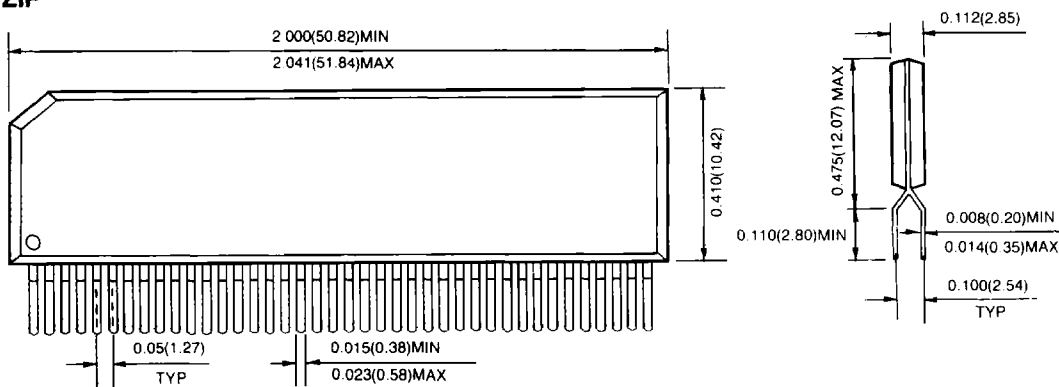
Package Dimensions

unit: inches (mm)

SOJ



ZIP



TSOP

