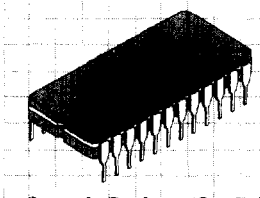
MB8416A-12, MB8416A-12L, MB8416A-15, MB8416A-15L

CMOS 16,384-Bit Static Random Access Memory

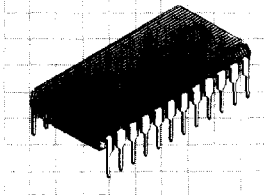
Description

The Fujitsu MB8416A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

The MB8416A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.



Ceramic Package(Cerdip)
DIP-24C-C03

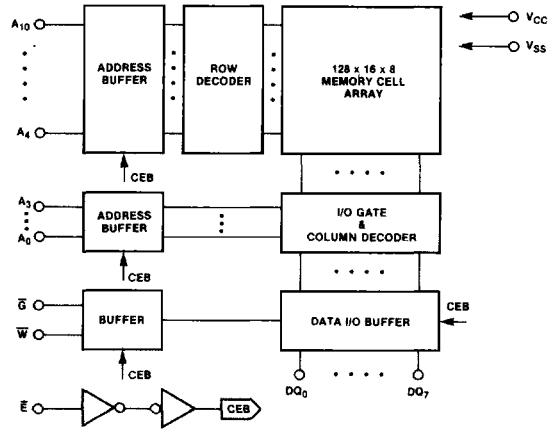


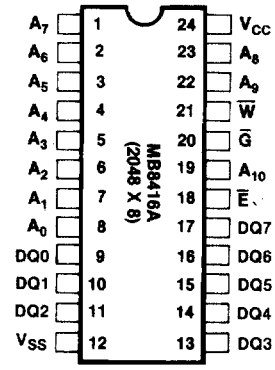
Plastic Package
DIP-24P-M01

Features

- Organization: 2048 words x 8-bits
- Fast Access Time:
  120 ns max. (MB8416A-12/12L)
  150 ns max. (MB8416A-15/15L)
- Completely static operation: No clocks required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply
- Low power standby:
  5.5 mW max. (MB8416A-12/15)
  275μW max. (MB8416A-12L/15L)
- Data retention: 2.0V min.
- Jedec Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)
- Also Jedec Standard 32 pad LCC package.
- Pin compatible with HM6116, TC5517 and μPD446
- Output Enable ($\overline{G}$) pin for precise data bus control

MB8416A Block Diagram and Pin Assignment





Truth Table

$\overline{E}_B$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

R6

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Storage Temperature	Cerdip / Plastic	T_{stg}	−65 to +150 / −40 to +125	°C
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5 to V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

K2

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to GND)

R4

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Ambient Temperature	T_A	0	—	70	°C

DC Characteristics

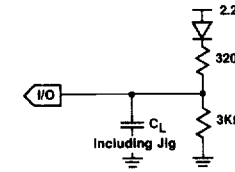
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	MB8416A-12/15 Min	MB8416A-12/15 Max	MB8416A-12L/15L Min	MB8416A-12L/15L Max	Unit
Standby Supply Current 1	$\overline{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2V$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E} = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E} = V_{IH}$ or $\overline{G} = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

Note: All voltages are referenced to GND.

AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load:	$C_L = 5_{pF}$ for TEHQZ, TGHQZ and TWLQZ $C_L = 100$ pF for all others.



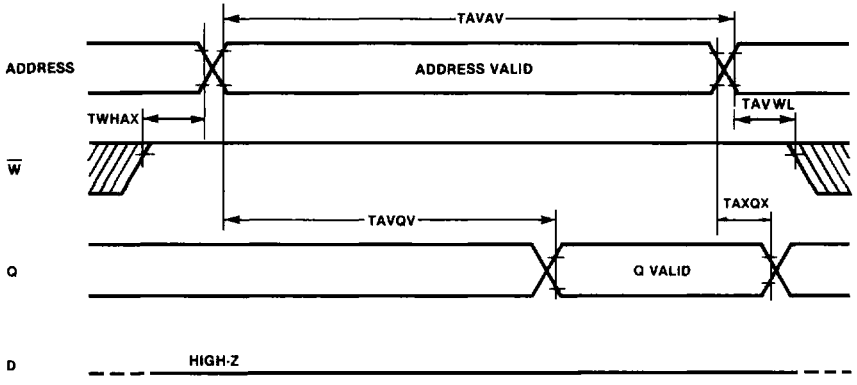
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

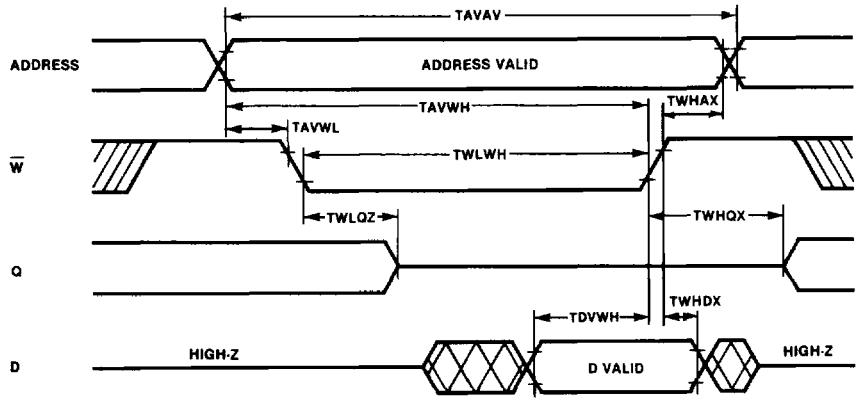
Parameter	Symbol	MB8416A-12/12L Min	MB8416A-12/12L Max	MB8416A-15/15L Min	MB8416A-15/15L Max	Unit
Read Cycle Time	TAVAV	120	—	150	—	ns
Write Cycle Time	TAVAV	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{G}$	TGLQX	10	—	10	—	ns
Output High Z from $\overline{G}$	TGHQZ	—	40	—	50	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Output Enable to Output Valid	TGLQV	—	50	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	0	—	ns
Write Set Up Time	TWLEL	0	—	0	—	ns
Write Hold Time	TEHWH	0	—	0	—	ns
Address Valid to End of Write	TAVWH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH	100	—	120	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Write Recovery Time	TWHAX, TEHAX	5	—	5	—	ns
Data Set Up Time	TDVEH, TDVWH	35	—	40	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	0	—	ns

Mode 1 — $\overline{W}$ Controlled
($\overline{E}$ = Low, $\overline{G}$ = Low)

Read Cycle Timing Diagram

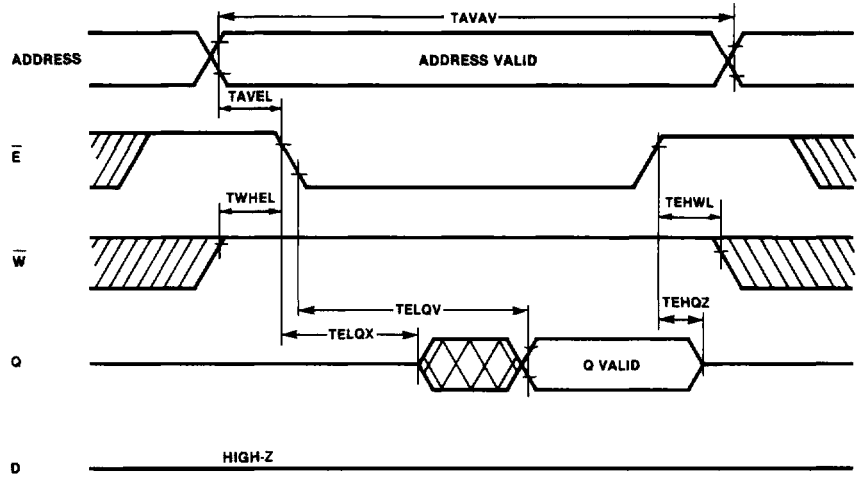


Write Cycle Timing Diagram

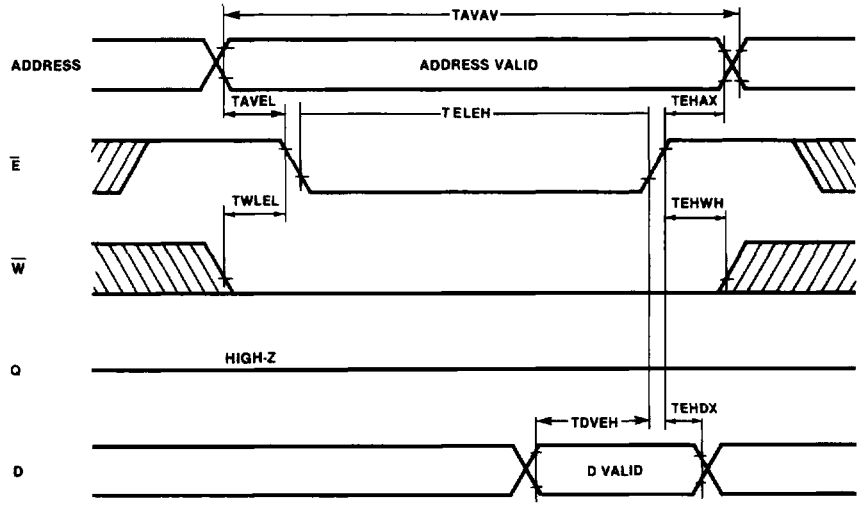


Mode 2 — $\overline{E}$ Controlled
($\overline{G}$ = Low)

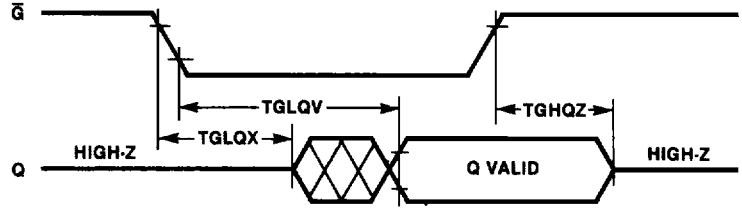
Read Cycle Timing Diagram



Write Cycle Timing Diagram



Mode 3 — $\overline{G}$ Controlled
($\overline{E}$ = Low, $\overline{W}$ = High, Address Valid)

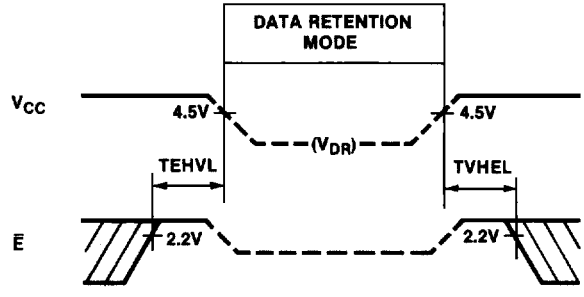


Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8416A-12/15 Min	MB8416A-12/15 Max	MB8416A-12L/15L Min	MB8416A-12L/15L Max	Unit	Test Condition
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	40	—	40	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

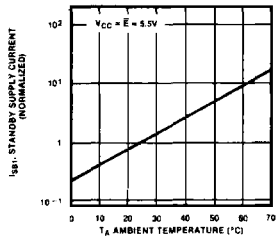
Note 1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V. $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR} = 3.0V$, $\overline{E} = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.
Note 3. $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.

Data Retention Timing Diagram

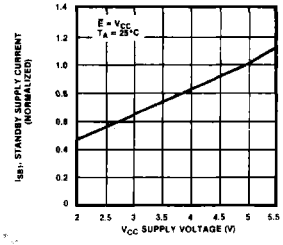


Typical Characteristics Curves

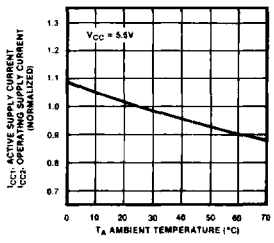
Standby Supply Current vs. Ambient Temp



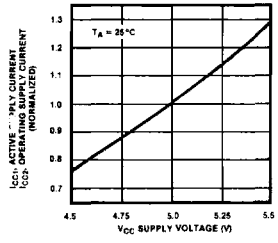
Standby Supply Current vs. Supply Voltage



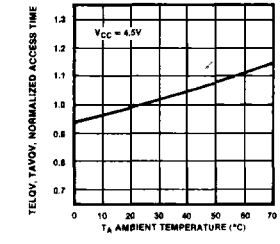
Supply Current (Active/Operating) vs. Ambient Temp



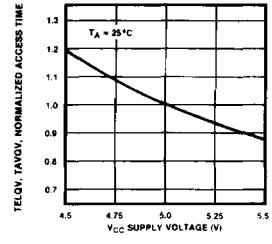
Supply Current (Active/Operating) vs. Supply Voltage



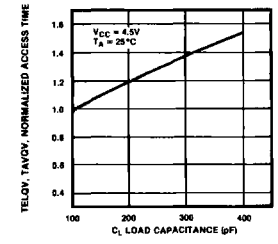
Access Times vs. Ambient Temp



Access Times vs. Supply Voltage



Access Times vs. Load Capacitance



Supply Current vs. Frequency