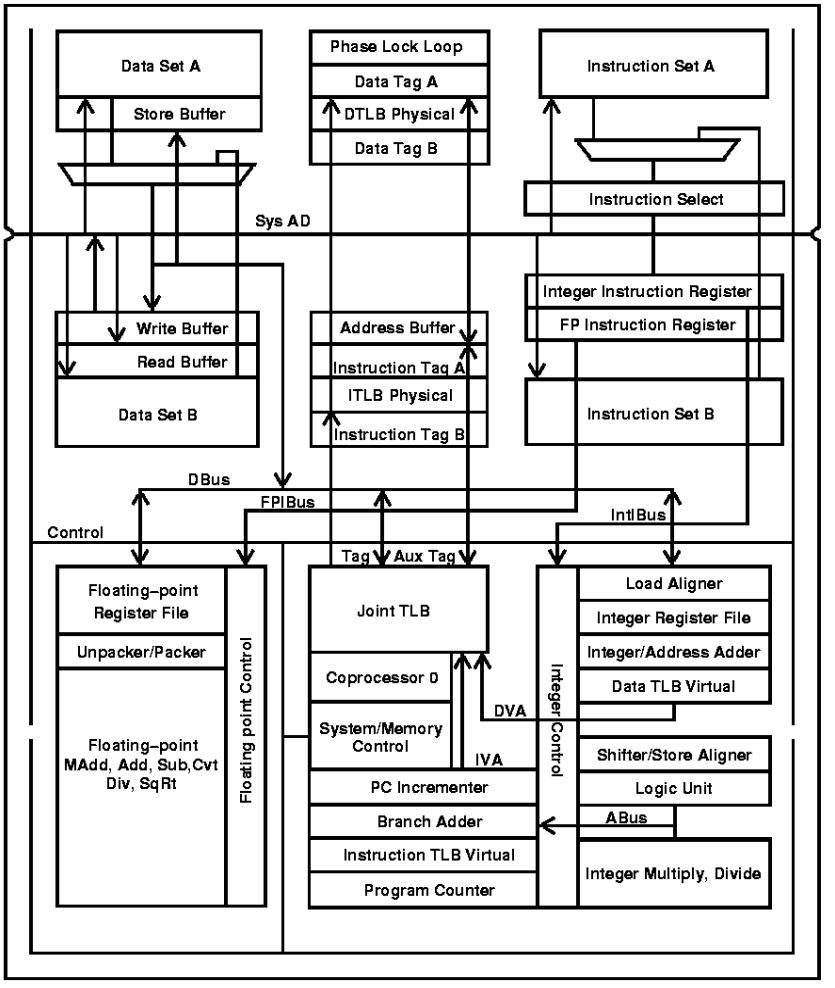
ACT5260
64–Bit Superscaler Microprocessor

Features

- Full militarized QED RM5260 microprocessor
- Dual Issue superscalar QED RISCMark™ microprocessor – can issue one integer and one floating–point instruction per cycle
  - 100, 133 and 150MHz operating frequency
- High performance system interface compatible with R4600, R4700 and R5000
  - 64–bit multiplexed system address/data bus for optimum price/performance
  - High performance write protocols maximize uncached write bandwidth
  - Operates at input system clock multipliers of 2 through 8
  - 5V tolerant I/O's
  - IEEE 1149.1 JTAG boundary scan
- Integrated on–chip caches
  - 16KB instruction – 2 way set associative
  - 16KB data – 2 way set associative
  - Virtually indexed, physically tagged
  - Write–back and write–through on per page basis
  - Pipeline restart on first double for data cache misses
- Integrated memory management unit
  - Fully associative joint TLB (shared by I and D translations)
  - 48 dual entries map 96 pages
  - Variable page size (4KB to 16MB in 4x increments)
- High–performance floating point unit
  - Single cycle repeat rate for common single precision operations and some double precision operations
  - Two cycle repeat rate for double precision multiply and double precision combined multiply–add operations
  - Single cycle repeat rate for single precision combined multiply–add operation
- MIPS IV instruction set
  - Floating point multiply–add instruction increases performance in signal processing and graphics applications
  - Conditional moves to reduce branch frequency
  - Index address modes (register + register)
- Embedded application enhancements
  - Specialized DSP integer Multiply–Accumulate instruction and 3 operand multiply instruction
  - I and D cache locking by set
  - Optional dedicated exception vector for interrupts
- Fully static CMOS design with power down logic
  - Standby reduced power mode with WAIT instruction
  - 5 Watts typical at 3.3V, less than TBD mwatts in Standby
- Embedded supply de–coupling capacitors and PII filter components
- 208–lead CQFP, cavity–up package
- 179–pin PGA package (*Future Product*)

BLOCK DIAGRAM



Preliminary

DESCRIPTION:

The ACT5260 is a highly integrated superscalar microprocessor that implements a superset of the MIPS IV Instruction Set Architecture(ISA). It has a high performance 64–bit integer unit, a high throughput, fully pipelined 64–bit floating point unit, an operating system friendly memory management unit with a 48–entry fully associative TLB, a 16 KByte 2–way set associative instruction cache, a 16 KByte 2–way set associative data cache, and a high–performance 64–bit system interface. The ACT5260 can issue both an integer and a floating point instruction in the same cycle.

The ACT5260 is ideally suited for high–end embedded control applications such as internetworking, high performance image manipulation, high speed printing, and 3–D visualization.

HARDWARE OVERVIEW

The ACT5260 offers a high–level of integration targeted at high–performance embedded applications. Some of the key elements of the ACT5260 are briefly described below.

Superscalar Dispatch

The ACT5260 has an efficient asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating–point computation instruction simultaneously. With respect to superscalar issue, integer instructions include alu, branch, load/store, and floating–point load/store, while floating–point computation instructions include floating–point add, subtract, combined multiply–add, converts, etc. In combination with its high throughput fully pipelined floating–point execution unit, the superscalar capability of the ACT5260 provides unparalleled price/performance in computationally intensive embedded applications.

CPU Registers

Like all MIPS ISA processors, the ACT5260 CPU has a simple, clean user visible state consisting of 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits.

Pipeline

For integer operations, loads, stores, and other non–floating–point operations, the ACT5260 uses the simple 5–stage pipeline also found in the circuits R4600, R4700, and R5000. In addition to this standard pipeline, the ACT5260 uses an extended seven stage pipeline for floating–point operations. Like the R5000, the ACT5260 does virtual to physical translation in parallel with cache access.

Integer Unit

Like the R5000, the ACT5260 implements the MIPS IV Instruction Set Architecture, and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I–III instruction sets. Additionally, the ACT5260 includes two implementation specific instructions not found in the baseline MIPS IV ISA but that are useful in the embedded market place. Described in detail in the QED RM5260 datasheet, these instructions are integer multiply–accumulate and 3–operand integer multiply.

The ACT5260 integer unit includes thirty–two general purpose 64–bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/divide unit. Additional register resources include: the HI/LO result registers for the two–operand integer multiply/ divide operations, and the program counter(PC).

Register File

The ACT5260 has thirty–two general purpose registers with register location 0 hard wired to zero. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

ALU

The ACT5260 ALU consists of the integer adder/ subtractor, the logic unit, and the shifter. The adder performs address calculations in addition to arithmetic operations, the logic unit performs all logical and zero shift data moves, and the shifter performs shifts and store alignment operations. Each of these units is optimized to perform all operations in a single processor cycle

For additional Detail Information regarding the operation of the Quantum Effect Design (QED) RISCMark™ RM5260™, 64–Bit Superscalar Microprocessor see the latest QED datasheet.

Absolute Maximum Ratings[1]

Symbol	Rating	Range	Units
V_{TERM}	Terminal Voltage with respect to GND	−0.5[2] to 4.6	V
Tc	Operating Temperature	−55 to +125	°C
T_{BIAS}	Case Temperature under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	°C
I_{IN}	DC Input Current	20[3]	mA
I_{OUT}	DC Output Current	50	mA

Notes:
1. Stresses above those listed under "AbsoluteMaximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. V_{IN} minimum = −2.0V for pulse width less than 15nS. V_{IN} maximum should not exceed +5.5 Volts.
3. When V_{IN} < 0V or V_{IN} > Vcc.
4. No more than one output should be shorted at one time. Duration of the short should not exceed more than 30 second.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+3.135	+3.465	V
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	−0.5	$0.2V_{CC}$	V
T_C	Operating Temperature Case (Commercial)	−55	+125	°C

DC Characteristics

(Vcc = 3.3V ±5%; Tc =−55°C to +125°C)

Parameter	Sym	Conditions	100 / 133 / 150MHz		Units
			Min	Max	
Output Low Voltage	V_{OL1}	I_{OL} = 20 µA		0.1	V
Output High Voltage	V_{OH1}	I_{OL} = 20 µA	Vcc − 0.1		V
Output Low Voltage	V_{OL2}	I_{OL} = 4 mA		0.4	V
Output High Voltage	V_{OH2}	I_{OL} = 4 mA	2.4		V
Input High Voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}		−0.5	$0.2V_{CC}$	V
Input Current	I_{IN1}	V_{IN} = 0V	−20	+20	µA
Input Current	I_{IN2}	V_{IN} = V_{CC}	−20	+20	µA
Input Current	I_{IN3}	V_{IN} = 5.5V	−250	+250	µA
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF

Power Consumption

Parameter	Symbol	Conditions	100MHz, 3.3V		133MHz, 3.3V		150MHz, 3.3V		Units
			Typ[5]	Max	Typ[5]	Max	Typ[5]	Max	
Active Operating Supply Current	I_{CC1}	C_L = 0pF, 150/75MHz, No SysAD activity	TBD	TBD	TBD	TBD	TBD	TBD	mA
	I_{CC2}	C_L = 50pF, 150/75MHz, R4000 write protocol without FPU operation	1000	1750	1000	1750	1150	1950	mA
	I_{CC3}	C_L = 50pF, 150/75MHz, write re–issue or pipelined writes	1100	2000	1100	2000	1250	2250	mA
Standby Current	I_{SB1}	C_L = 0pF, 150/75MHz		TBD		TBD		TBD	mA
	I_{SB1}	C_L = 50pF, 150/75MHz		TBD		TBD		TBD	mA

Notes:
5. Typical integer instruction mix and cache miss rates.

AC Characteristics
(V_{CC} = 3.3V ±5%; Tc = –55°C to +125°C)

Capacitive Load Deration

Symbol	Parameter	100 / 133 / 150MHz		Units
		Minimum	Maximum	
C_{LD}	Load Derate		2	ns/25pF

Clock Parameters

Parameter	Symbol	Test Conditions	100/133/150MHz		Units
			Min	Max	
SysClock High	t_{SCHigh}	Transition ≤ 5ns	4		ns
SysClock Low	t_{SCLow}	Transition ≤ 5ns	4		ns
SysClock Frequency[6]			33	75	MHz
SysClock Period	t_{SCP}			30	ns
Clock Jitter for SysClock	$t_{JitterIn}$			±250	ps
SysClock Rise Time	t_{SCRise}			5	ns
SysClock Fall Time	t_{SCFall}			5	ns
ModeClock Period	$t_{ModeCKP}$			$256*t_{SCP}$	ns
JTAG Clock Period	$t_{JTAGCKP}$			$4*t_{SCP}$	ns

Notes:
6. Operation of the ACT5260 is only guaranteed with the Phase Loop enabled.

System Interface Parameters[7]

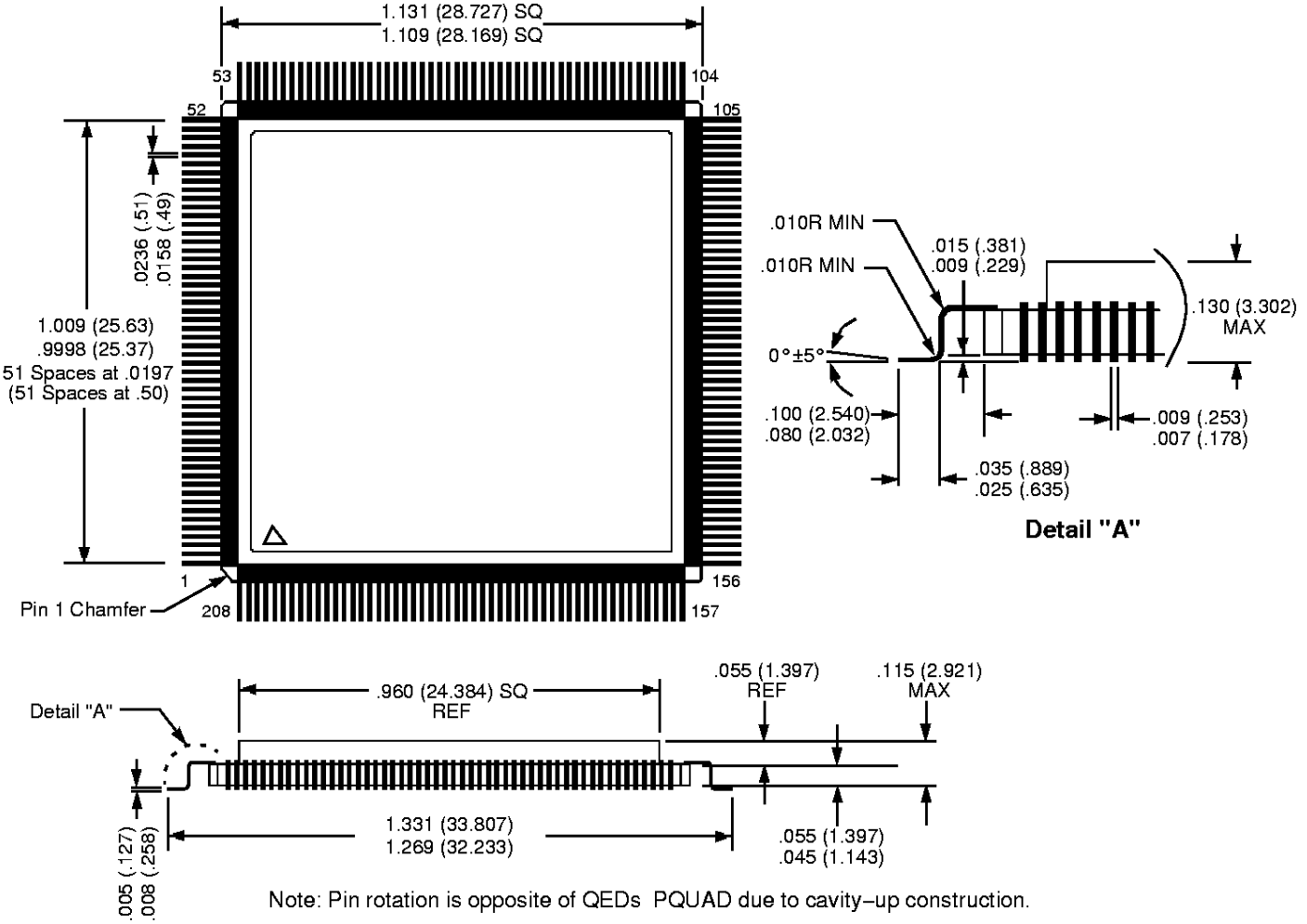
Parameter	Symbol	Test Conditions	100MHz		133MHz		150MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output[8]	t_{DO}	$mode_{14...13}$ = 10 (fastest)	TBD	TBD	TBD	TBD	TBD	TBD	ns
		$mode_{14...13}$ = 11	TBD	TBD	TBD	TBD	TBD	TBD	ns
		$mode_{14...13}$ = 00	1.0	8.0	1.0	8.0	1.0	8.0	ns
		$mode_{14...13}$ = 01 (slowest)	TBD	TBD	TBD	TBD	TBD	TBD	ns
Data Setup	t_{DS}	t_{RISE} = 5ns	4.0		4.0		4.0		ns
Data Hold	t_{DH}	t_{FALL}= 5ns	0		0		0		ns

Notes:
7. Timmings are are measured from from 1.5V of the clock to 1.5V of the signal.
8. Capacitive load for all output timing is 50pF.

Boot Time Interface Parameters

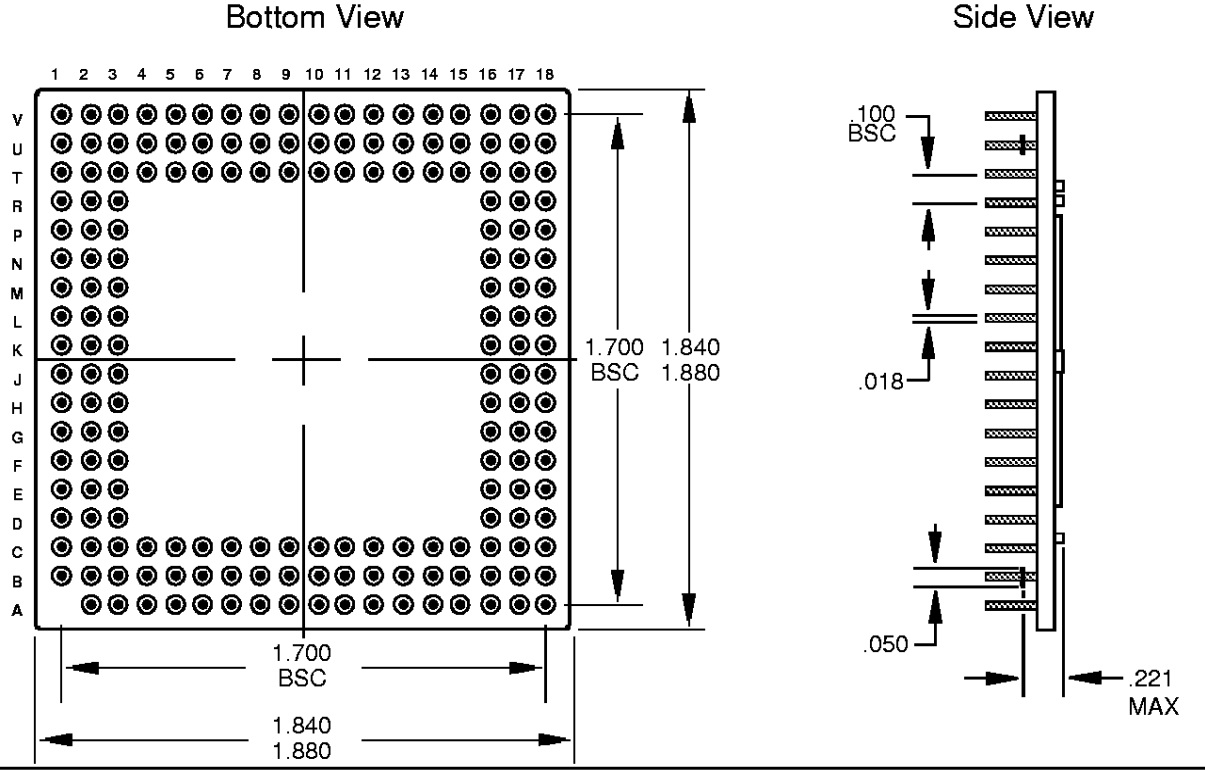
Parameter	Symbol	Test Conditions	100/133/150MHz		Units
			Min	Max	
Mode Data Setup	t_{DS}		4		SysClock cycles
Mode Data Hold	t_{DH}		0		SysClock cycles

Package Information – "F17" – CQFP 208 Leads



Note: Pin rotation is opposite of QEDs PQUAD due to cavity–up construction.

Future Package – "P10" – PGA 179 Pins



ACT5260 Microprocessor CQFP Pinouts – "F17"

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	Vcc	53	NC	105	Vcc	157	NC
2	NC	54	NC	106	NMI*	158	NC
3	NC	55	NC	107	ExtRqst*	159	NC
4	Vcc	56	Vcc	108	Reset*	160	NC
5	Vss	57	Vss	109	ColdReset*	161	Vcc
6	SysAD4	58	ModeIn	110	VccOK	162	Vss
7	SysAD36	59	RdRdy*	111	BigEndian	163	SysAD28
8	SysAD5	60	WrRdy*	112	Vcc	164	SysAD60
9	SysAD37	61	ValidIn*	113	Vss	165	SysAD29
10	Vcc†	62	ValidOut*	114	SysAD16	166	SysAD61
11	Vss	63	Release*	115	SysAD48	167	Vcc†
12	SysAD6	64	VccP	116	Vcc†	168	Vss
13	SysAD38	65	VssP	117	Vss	169	SysAD30
14	Vcc	66	SysClock	118	SysAD17	170	SysAD62
15	Vss	67	Vcc†	119	SysAD49	171	Vcc
16	SysAD7	68	Vss	120	SysAD18	172	Vss
17	SysAD39	69	Vcc	121	SysAD50	173	SysAD31
18	SysAD8	70	Vss	122	Vcc	174	SysAD63
19	SysAD40	71	Vcc†	123	Vss	175	SysADC2
20	Vcc†	72	Vss	124	SysAD19	176	SysADC6
21	Vss	73	SysCmd0	125	SysAD51	177	Vcc†
22	SysAD9	74	SysCmd1	126	Vcc†	178	Vss
23	SysAD41	75	SysCmd2	127	Vss	179	SysADC3
24	Vcc	76	SysCmd3	128	SysAD20	180	SysADC7
25	Vss	77	Vcc	129	SysAD52	181	Vcc
26	SysAD10	78	Vss	130	SysAD21	182	Vss
27	SysAD42	79	SysCmd4	131	SysAD53	183	SysADC0
28	SysAD11	80	SysCmd5	132	Vcc	184	SysADC4
29	SysAD43	81	Vcc	133	Vss	185	Vcc†
30	Vcc†	82	Vss	134	SysAD22	186	Vss
31	Vss	83	SysCmd6	135	SysAD54	187	SysADC1
32	SysAD12	84	SysCmd7	136	Vcc†	188	SysADC5
33	SysAD44	85	SysCmd8	137	Vss	189	SysAD0
34	Vcc	86	SysCmdP	138	SysAD23	190	SysAD32
35	Vss	87	Vcc†	139	SysAD55	191	Vcc
36	SysAD13	88	Vss	140	SysAD24	192	Vss
37	SysAD45	89	Vcc†	141	SysAD56	193	SysAD1
38	SysAD14	90	Vss	142	Vcc	194	SysAD33
39	SysAD46	91	Vcc	143	Vss	195	Vcc†
40	Vcc†	92	Vss	144	SysAD25	196	Vss
41	Vss	93	Int0*	145	SysAD57	197	SysAD2
42	SysAD15	94	Int1*	146	Vcc†	198	SysAD34
43	SysAD47	95	Int2*	147	Vss	199	SysAD3
44	Vcc	96	Int3*	148	SysAD26	200	SysAD35
45	Vss	97	Int4*	149	SysAD58	201	Vcc
46	ModeClock	98	Int5*	150	SysAD27	202	Vss
47	JTDO	99	Vcc	151	SysAD59	203	NC
48	JTDI	100	Vss	152	Vcc	204	NC
49	JTCK	101	NC	153	Vss	205	NC
50	JTMS	102	NC	154	NC	206	NC
51	Vcc	103	NC	155	NC	207	Vcc
52	Vss	104	NC	156	Vss	208	Vss

† These Vcc pins may be 2.5V in future higher performance devices

ACT5260 Microprocessor Future PGA Pinouts – "P10"

Signal	PGA	Signal	PGA	Signal	PGA
INT0	N2	SYSAD45	B17	VCC	A13
INT1	L3	SYSAD46	E17	VCC	A16
INT2	K3	SYSAD47	F17	VCC	B18
INT3	J3	SYSAD48	L2	VCC	C1
INT4	H3	SYSAD49	M3	VCC	D18
INT5	F2	SYSAD5	C4	VCC	F1
NC	T13	SYSAD50	N3	VCC	G18
GND	U12	SYSAD51	R2	VCC	H1
JTCK	H17	SYSAD52	T3	VCC	J18
JTDI	G16	SYSAD53	U3	VCC	K1
JTDO	F16	SYSAD54	T6	VCCP	K17
JTMS	E16	SYSAD55	T7	VCC	L18
MODECLK	B4	SYSAD56	T10	VCC	M1
MODEIN	U4	SYSAD57	T11	VCC	N18
SYSCLK	J17	SYSAD58	U13	VCC	R1
NC	P17	SYSAD59	V15	VCC	T18
NC	T17	SYSAD6	B5	VCC	U1
NC	R16	SYSAD60	T15	VCC	V3
NC	J16	SYSAD61	U17	VCC	V6
NC	P16	SYSAD62	N16	VCC	V8
SYSAD0	J2	SYSAD63	N17	VCC	V10
SYSAD1	G2	SYSAD7	B6	VCC	V12
SYSAD10	C12	SYSAD8	B9	VCC	V14
SYSAD11	B14	SYSAD9	B11	VCC	V17
SYSAD12	B15	SYSADC0	C8	VCC	T9
SYSAD13	C16	SYSADC1	G17	GND	A3
SYSAD14	D17	SYSADC2	T8	GND	A6
SYSAD15	E18	SYSADC3	L16	GND	A8
SYSAD16	K2	SYSADC4	B8	GND	A10
SYSAD17	M2	SYSADC5	H16	GND	A12
SYSAD18	P1	SYSADC6	U8	GND	A14
SYSAD19	P3	SYSADC7	L17	GND	A17
SYSAD2	E1	SYSCMD0	E2	GND	A18
SYSAD20	T2	SYSCMD1	D3	GND	B1
SYSAD21	T4	SYSCMD2	B2	GND	C18
SYSAD22	U5	SYSCMD3	A5	GND	D1
SYSAD23	U6	SYSCMD4	B7	GND	F18
SYSAD24	U9	SYSCMD5	C9	GND	G1
SYSAD25	U11	SYSCMD6	B10	GND	H18
SYSAD26	T12	SYSCMD7	B12	GND	J1
SYSAD27	U14	SYSCMD8	C13	VSSP	K16
SYSAD28	U15	SYSCMDP	C14	GND	K18
SYSAD29	T16	NC	C17	GND	L1
SYSAD3	E3	NC	D16	GND	M18
SYSAD30	R17	VCCOK	M17	GND	N1
SYSAD31	M16	CLDRST	T14	GND	P18
SYSAD32	H2	EXTRQST	U2	GND	R18
SYSAD33	G3	NC	B16	GND	T1
SYSAD34	F3	NMI	U7	GND	U18
SYSAD35	D2	RDRDY	T5	GND	V1
SYSAD36	C3	RELEASE	V5	GND	V2
SYSAD37	B3	RESET	U16	GND	V4
SYSAD38	C6	VALIDOUT	R3	GND	V7
SYSAD39	C7	VALIDIN	P2	GND	V9
SYSAD4	C2	WRRDY	C5	GND	V11
SYSAD40	C10	VCC	A2	GND	V13
SYSAD41	C11	VCC	A4	GND	V16
SYSAD42	B13	NC	A7	GND	V18
SYSAD43	A15	VCC	A9	–	–
SYSAD44	C15	VCC	A11	NC	U10

AEROFLEX
CIRCUIT TECHNOLOGY

Sample Ordering Information

Part Number	Screening	Speed (MHz)	Package
ACT–5260PC–100F17C	Commercial Temperature	100	208 Lead CQFP
ACT–5260PC–133F17T	Military Temperature	133	208 Lead CQFP
ACT–5260PC–150F17M	Military Screening	150	208 Lead CQFP

Part Number Breakdown

ACT– 5260 PC – 100 F17 M

Aeroflex Circuit Technology

Base Processor Type

Cache Style

PC = Primary Cache

Maximum Pipeline Freq.

100 = 100MHz
133 = 133MHz
150 = 150MHz
200 = 200MHZ (Future option)

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, –40°C to +85°C
T = Military Temp, –55°C to +125°C
M = Military Temp, –55°C to +125°C, Screened*
Q = MIL–PRF–38534 Compliant/SMD if applicable

Package Type & Size

Surface Mount Package

F18 = 1.120" SQ 208 Lead CQFP

Thru–Hole Package

P10 = 1.86"SQ PGA 179 pins with shoulder

* **Screened to the individual test methods of MIL–STD–883**

Specifications subject to change without notice.

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