Features

- **16 Mbit SRAM Multi Chip Module**
- **Allows 32-, 16- or 8-bit access configuration**
- **Operating Voltage: 3.3V $\pm$ 0.3V**
- **Access Time:**
  - **AT68166FT (5V Tolerant)**
    - **25 ns**
    - **20 ns (preliminary information)**
  - **AT68166F**
    - **20 ns**
    - **18 ns (preliminary information)**
- **Very Low Power Consumption**
  - **AT68166FT (5V Tolerant)**
    - **Active: 540 mW per byte (Max) @ 25 ns - 450 mW per byte (Max) @ 50ns**
    - **Standby: 15 mW (Typ)**
  - **AT68166F**
    - **Active: 620 mW per byte (Max) @ 20 ns - 450 mW per byte (Max) @ 50ns**
    - **Standby: 15 mW (Typ)**
- **Military Temperature Range: -55 to +125°C**
- **TTL-Compatible Inputs and Outputs**
- **Asynchronous**
- **Die manufactured on Atmel 0.25 µm Radiation Hardened Process**
- **No Single Event Latch Up below LET Threshold of 80 MeV/mg/cm^2**
- **Tested up to a Total Dose of 300 krads (Si) according to MIL-STD-883 Method 1019**
- **ESD Better than 4000V for the AT68166F**
- **ESD Better than 2000V for the AT68166FT**
- **Quality Grades:**
  - **QML-Q or V with SMD 5962-06229**
  - **ESCC**
- **950 Mils Wide MQFPT 68 Package**
- **Mass : 8.5 grams**

Description

The AT68166F/FT is a 16 Mbit Radiation Hardened hermetic Multi Chip Module (MCM), made of very low-power CMOS asynchronous static RAM which can be organized as 1 bank of 512K x 32, 2 banks of 512Kx16, or 4 banks of 512Kx8. It is built with 4 dice of the AT60142F/FT SRAM keeping all their basic characteristics: power consumption, stand by current, data retention, Multiple Bit Upset (MBU) immunity, etc.

This MCM takes full benefit of Atmel expertise in hermetic ceramic package assembly. The small size of the AT60142F/FT die allows for assembling it in a 68 pins quad flat pack which results into a package footprint compatible with products from other sources. Furthermore, all dice being assembled on the same package side makes power dissipation through the PCB much easier and more efficient.

This MCM brings the solution to applications where fast computing is as mandatory as low power consumption and higher integration density, saving 75% of the PCB area used when using the individually packaged 4 Mbit SRAM.

AT68166F and AT68166FT power supply is 3.3V. AT68166FT is 5V tolerant while AT68166F is not.

The AT68166F/FT are processed according to the test methods of the latest revision of the MIL-PRF-38535 or the ESCC 9000.

Rad Hard 16 MegaBit SRAM Multi Chip Module

AT68166F
AT68166FT

7531F–AERO–04/07

Block Diagram

Figure 1. AT68166F/FT Block Diagram

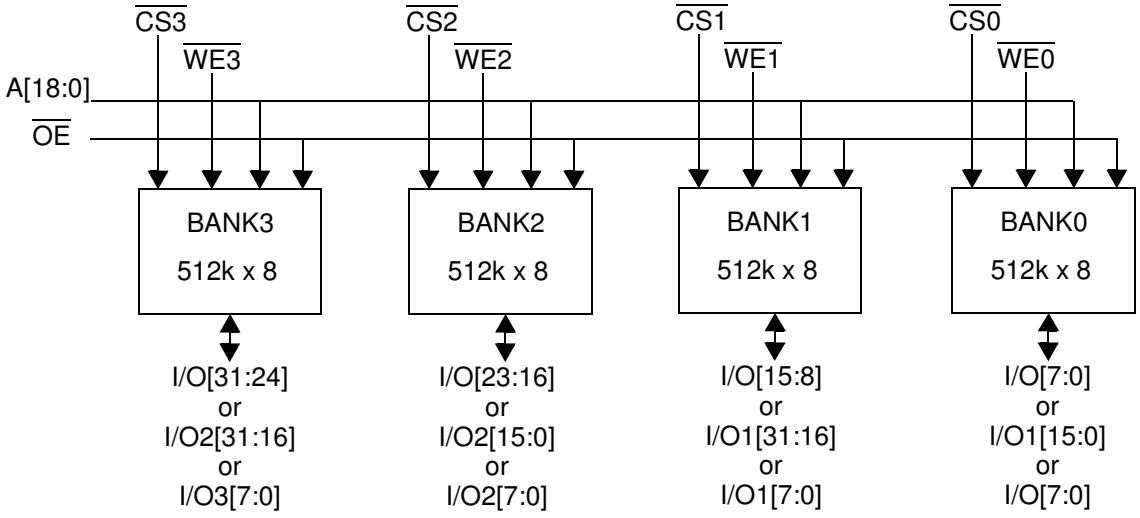
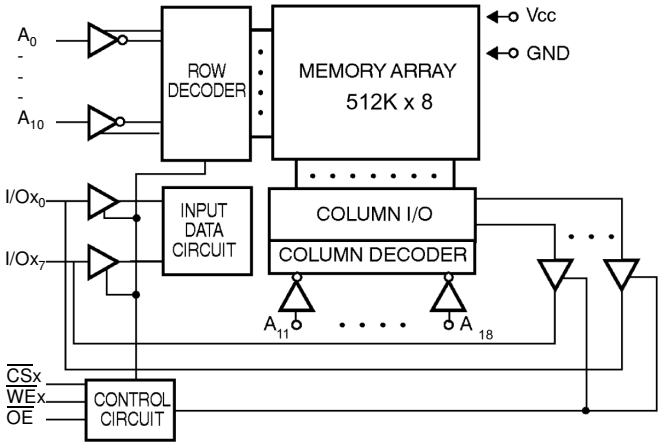


Figure 2. 512K x 8 Banks Block Diagram (AT60142F/FT)



Packages

AT68166 is packed in MQFP68.

	Access Times		
	25 ns	**20 ns**	**18 ns**
AT68166FT	YM	YS	-
AT68166F	-	YM	YS

The pin assignment depends on the access time. There are 2 versions:

- YM package where 3 pins are not connected.
- YS package where the 3 above pins are connected to GND or V_{CC}.

Pin Configuration

Table 1. AT68166F/FT pin assignement in YM package

Lead	Signal	Lead	Signal	Lead	Signal	Lead	Signal
1	I/O0[0]	18	VCC	35	I/O3[7]	52	VCC
2	I/O0[1]	19	A11	36	I/O3[6]	53	A10
3	I/O0[2]	20	A12	37	I/O3[5]	54	A9
4	I/O0[3]	21	A13	38	I/O3[4]	55	A8
5	I/O0[4]	22	A14	39	I/O3[3]	56	A7
6	I/O0[5]	23	A15	40	I/O3[2]	57	A6
7	I/O0[6]	24	A16	41	I/O3[1]	58	$\overline{WE0}$
8	I/O0[7]	25	$\overline{CS0}$	42	I/O3[0]	59	$\overline{CS3}$
9	GND	26	$\overline{OE}$	43	GND	60	GND
10	I/O1[0]	27	$\overline{CS1}$	44	I/O2[7]	61	$\overline{CS2}$
11	I/O1[1]	28	A17	45	I/O2[6]	62	A5
12	I/O1[2]	29	$\overline{WE1}$	46	I/O2[5]	63	A4
13	I/O1[3]	30	$\overline{WE2}$	47	I/O2[4]	64	A3
14	I/O1[4]	31	$\overline{WE3}$	48	I/O2[3]	65	A2
15	I/O1[5]	32	A18	49	I/O2[2]	66	A1
16	I/O1[6]	33	NC(2)	50	I/O2[1]	67	A0
17	I/O1[7]	34	NC(1)	51	I/O2[0]	68	NC(1)

Notes: 1. In YS package leads 34 and 68 are connected to V_{CC}.
2. In YS package lead 33 is connected in GND.

Figure 3. AT68166F/FT pin assignment in YM package

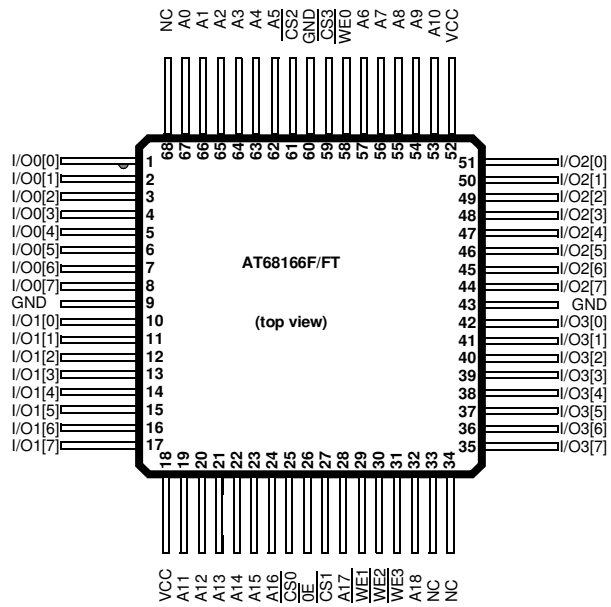
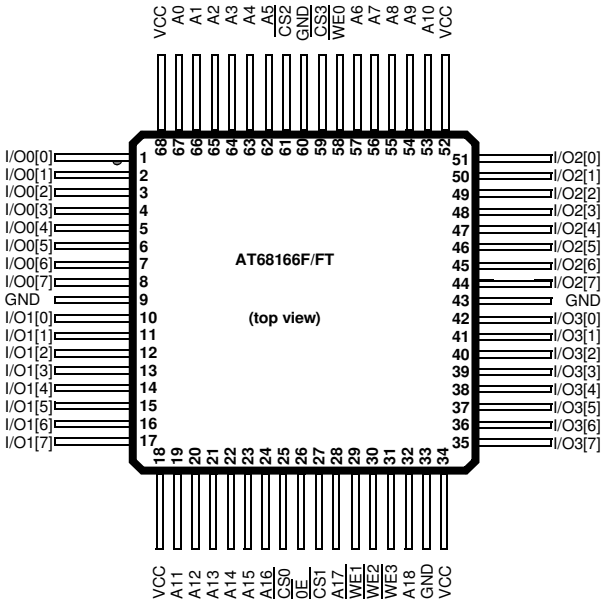


Figure 4. AT68166F/FT pin assignment in YS package



Pin Description

Table 2. Pin Names

Name	Description
A0 - A18	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CS0}$ - $\overline{CS3}$	Chip Select
$\overline{WE0}$ - $\overline{WE3}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
GND[1]	Ground

Note: 1. The package lid is connected to GND

Table 3. Truth Table[1]

$\overline{CSx}$	$\overline{WEx}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	Z	Standby
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	Z	Output Disable

Note: 1. L=low, H=high, X= H or H, Z=high impedance.

Electrical Characteristics

Absolute Maximum Ratings*

Supply Voltage to GND Potential:	-0.5V + 4.6V
DC Input Voltage:	GND -0.5V to 4.6V[1]
DC Output Voltage High Z State:	GND -0.5V to 4.6V[1]
Storage Temperature:	-65°C to + 150°C
Output Current Into Outputs (Low):	20 mA
Electro Statics Discharge Voltage[2]:	> 4000V (MIL STD 883D Method 3015.3)

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. 7V for FT version.
2. For AT68166F. It is better than 2000V for AT68166FT.

Military Operating Range

Operating Voltage	Operating Temperature
3.3 $\pm$ 0.3V	-55°C to + 125°C

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
Vcc	Supply voltage	3	3.3	3.6	V
GND	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	V_{CC} + 0.3[1]	V

Note: 1. FT version: 5.5V in DC, 5.8V in transient conditions.

Capacitance

Parameter	Description	Min	Typ	Max	Unit
C_{in}[1] (OE and Ax)	Input capacitance	–	–	48	pF
C_{in}[1] (CSx and WEx)	Input capacitance	–	–	12	pF
C_{io}[1]	I/O capacitance	–	–	12	pF

Note: 1. Guaranteed but not tested.

DC Parameters

Parameter	Description	Minimum	Typical	Maximum	Unit
$IIX^{(1)}$	Input leakage current	-1	–	1	µA
$IOZ^{(1)}$	Output leakage current	-1	–	1	µA
$IIH^{(2)}$ at 5.5V	Input Leakage Current ($\overline{OE}$ & Axx)	–	–	10	µA
	Input Leakage Current ($\overline{WE}$ & $\overline{CS}$)	–	–	5	µA
$IOZH^{(2)}$ at 5.5V	Output Leakage Current	–	–	5	µA
$VOL^{(3)}$	Output low voltage	–	–	0.4	V
$VOH^{(4)}$	Output high voltage	2.4	–	–	V

Notes: 1. $GND < V_{IN} < V_{CC}$, $GND < V_{OUT} < V_{CC}$ Output Disabled.
2. FT version only: $V_{IN} = 5.5V$, $V_{OUT} = 5.5V$, Output Disabled.
3. V_{CC} min. I_{OL} = 8 mA (F version) - I_{OL} = 6 mA (FT version)
4. 4. V_{CC} min. I_{OH} = -4 mA

Consumption for AT68166FT

Symbol	Description	TAVAV/TAVAW Test Condition	AT68166FT-25	AT68166FT-20 (preliminary)	Unit	Value
$I_{CCSB}^{(1)}$	Standby Supply Current	–	10	10	mA	max
$I_{CCSB1}^{(2)}$	Standby Supply Current	–	8	8	mA	max
$I_{CCOP}^{(3)}$ Read per byte	Dynamic Operating Current	20 ns 25 ns 50 ns 1 µs	– 150 85 15	170 150 85 15	mA	max
$I_{CCOP}^{(4)}$ Write per byte	Dynamic Operating Current	20 ns 25 ns 50 ns 1 µs	– 150 125 110	150 150 125 110	mA	max

Notes: 1. All $\overline{CSx} \geq V_{IH}$
2. All $\overline{CSx} \geq V_{CC}$ - 0.3V
3. $F = 1/_{TAVAV}$, I_{out} = 0 mA, $\overline{WEx} = \overline{OE} = V_{IH}$, $V_{IN} = GND/V_{CC}$, V_{CC} max.
4. $F = 1/_{TAVAW}$, I_{out} = 0 mA, $\overline{WEx} = V_{IL}$, $\overline{OE} = V_{IH}$, $V_{IN} = GND/V_{CC}$, V_{CC} max.

Consumption for AT68166F

Symbol	Description	TAVAV/TAVAW Test Condition	AT68166F-20	AT68166F-18 (preliminary)	Unit	Value
I_{CCSB}(1)	Standby Supply Current	–	10	10	mA	max
I_{CCSB1}(2)	Standby Supply Current	–	8	8	mA	max
I_{CCOP}(3) Read per byte	Dynamic Operating Current	18 ns 20 ns 50 ns 1 µs	– 170 85 15	180 170 85 15	mA	max
I_{CCOP}(4) Write per byte	Dynamic Operating Current	18 ns 20 ns 50 ns 1 µs	– 150 125 110	155 150 125 110	mA	max

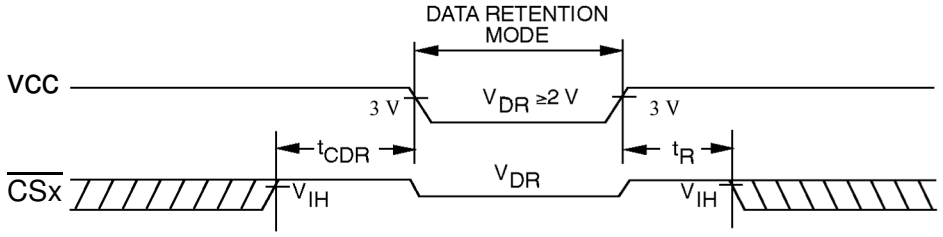
Notes:
1. All $\overline{CSx} \geq V_{IH}$
2. All $\overline{CSx} \geq V_{CC}$ - 0.3V
3. $F = 1/_{TAVAV}$, I_{out} = 0 mA, $\overline{WEx} = \overline{OE} = V_{IH}$, $V_{IN} = GND/V_{CC}$, V_{CC} max.
4. $F = 1/_{TAVAW}$, I_{out} = 0 mA, $\overline{WE}x = V_{IL}$, $\overline{OE} = V_{IH}$, $V_{IN} = GND/V_{CC}$, V_{CC} max.

Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. During data retention chip select $\overline{CSx}$ must be held high within V_{CC} to V_{CC} -0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions $\overline{CSx}$ and $\overline{OE}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}.
4. The RAM can begin operation > t_R ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 5. Data Retention Timing



Data Retention Characteristics

Parameter	Description	Min	Typ T_A = 25°C	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
t_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	t_{AVAV} (1)	–	–	ns
I_{CCDR} (2)	Data retention current	–	3	6	mA

1. T_{AVAV} = Read cycle time.
2. All $\overline{CSx}$ = V_{CC}, V_{IN} = GND/V_{CC}.

AC Characteristics

Temperature Range:..... -55 +125°C

Supply Voltage: ..... 3.3 $\pm$0.3V

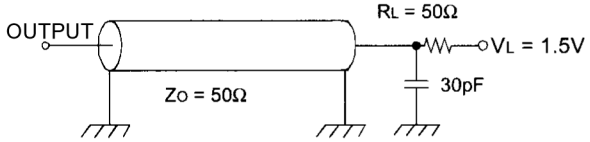
Input Pulse Levels: ..... GND to 3.0V

Input Rise and Fall Times:..... 3ns (10 - 90%)

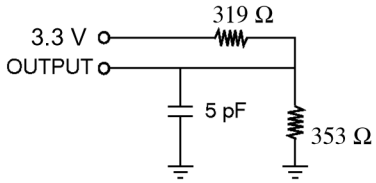
Input and Output Timing Reference Levels: 1.5V

Output Loading I_{OL}/I_{OH}:..... See Figure 3

Figure 6. AC Test Loads Waveforms



General



Specific (TWLQZ, TWHQX, TELQX, TEHQZ TGLQX, TGHQZ)

Write Cycle

Table 4. Write cycle timings for AT68166FT[2]

Symbol	Parameter	AT68166FT-25		AT68166FT-20 (preliminary)		Unit
		min	max	min	max	
TAVAW	Write cycle time	20	-	20	-	ns
TAVWL	Address set-up time	2	-	2	-	ns
TAVWH	Address valid to end of write	14	-	14	-	ns
TDVWH	Data set-up time	9	-	9	-	ns
TELWH	$\overline{CS}$ low to write end	12	-	12	-	ns
TWLQZ	Write low to high Z[1]	-	10	-	10	ns
TWLWH	Write pulse width	12	-	12	-	ns
TWHAX	Address hold from end of write	0	-	0	-	ns
TWHDX	Data hold time	2	-	2	-	ns
TWHQX	Write high to low Z[1]	5	-	5	-	ns

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 10.)
2. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.

Write Cycle

Table 5. Write cycle timings for AT68166F[2]

Symbol	Parameter	AT68166F-20		AT68166F-18 (preliminary)		Unit
		min	max	min	max	
TAVAW	Write cycle time	20	-	18	-	ns
TAVWL	Address set-up time	2	-	0	-	ns
TAVWH	Address valid to end of write	14	-	10	-	ns
TDVWH	Data set-up time	9	-	8	-	ns
TELWH	$\overline{CS}$ low to write end	12	-	12	-	ns
TWLQZ	Write low to high Z[1]	-	10	-	8	ns
TWLWH	Write pulse width	12	-	10	-	ns
TWHAX	Address hold from end of write	0	-	0	-	ns
TWHDX	Data hold time	2	-	0	-	ns
TWHQX	Write high to low Z[1]	5	-	3	-	ns

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 10.)
2. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.

Figure 7. Write Cycle 1. $\overline{WE}$ Controlled, $\overline{OE}$ High During Write

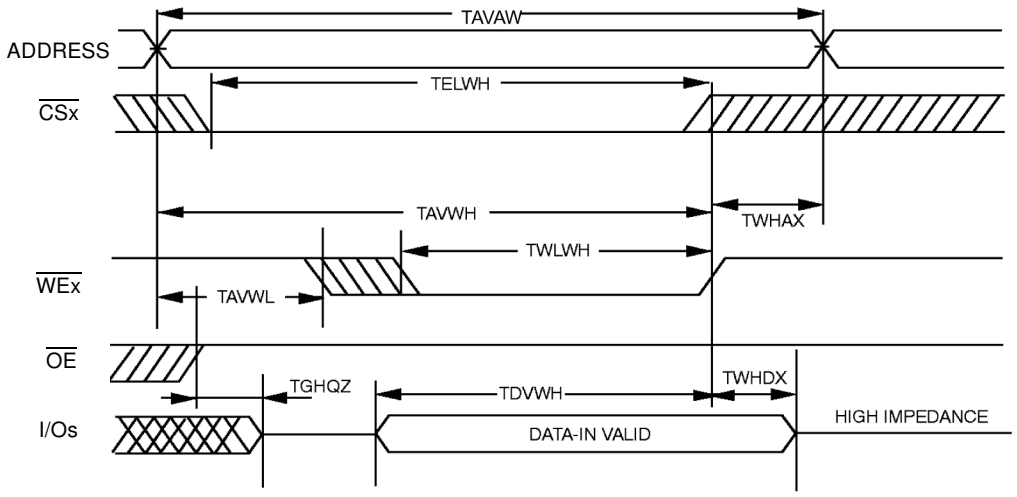


Figure 8. Write Cycle 2. $\overline{WE}$ Controlled, $\overline{OE}$ Low

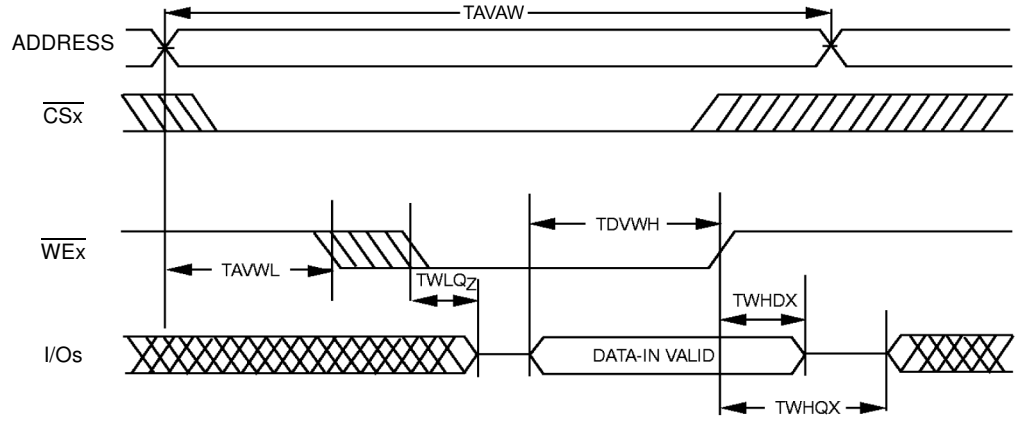
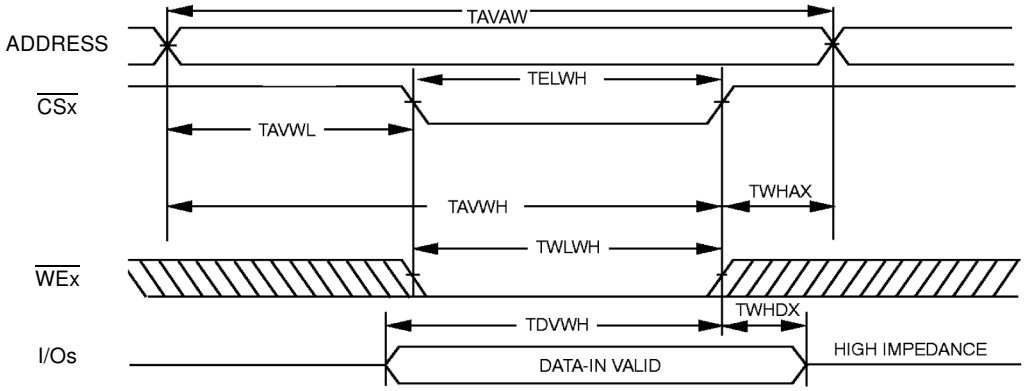


Figure 9. Write Cycle 3. $\overline{CS}$ Controlled[1]



The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{WE}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$= V_{IH}.

Read Cycle

Table 6. Read cycle timings for AT68166FT[2]

Symbol	Parameter	AT68166FT-25		AT68166FT-20 (preliminary)		Unit
		min	max	min	max	
TAVAV	Read cycle time	25	-	20	-	ns
TAVQV	Address access time	-	25	-	20	ns
TAVQX	Address valid to low Z	5	-	5	-	ns
TELQV	Chip-select access time	-	25	-	20	ns
TELQX	$\overline{CS}$ low to low Z[1]	5	-	5	-	ns
TEHQZ	$\overline{CS}$ high to high Z[1]	-	10	-	9	ns
TGLQV	Output Enable access time	-	12	-	11	ns
TGLQX	$\overline{OE}$ low to low Z[1]	2	-	2	-	ns
TGHQZ	$\overline{OE}$ high to high Z [1]	-	10	-	9	ns

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 10.)
2. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.

Table 7. Read cycle timings for AT168166F[2]

Symbol	Parameter	AT68166F-20		AT68166F-18 (preliminary)		Unit
		min	max	min	max	
TAVAV	Read cycle time	20	-	18	-	ns
TAVQV	Address access time	-	20	-	18	ns
TAVQX	Address valid to low Z	5	-	5	-	ns
TELQV	Chip-select access time	-	20	-	18	ns
TELQX	$\overline{CS}$ low to low Z[1]	5	-	5	-	ns
TEHQZ	$\overline{CS}$ high to high Z[1]	-	9	-	7	ns
TGLQV	Output Enable access time	-	11	-	9	ns
TGLQX	$\overline{OE}$ low to low Z[1]	2	-	2	-	ns
TGHQZ	$\overline{OE}$ high to high Z [1]	-	9	-	7	ns

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See “AC Test Loads Waveforms” on page 10.)

Timings figures applicable for 8-bit, 16-bit and 32-bit mode

Figure 10. Read Cycle nb 1: Address Controlled ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

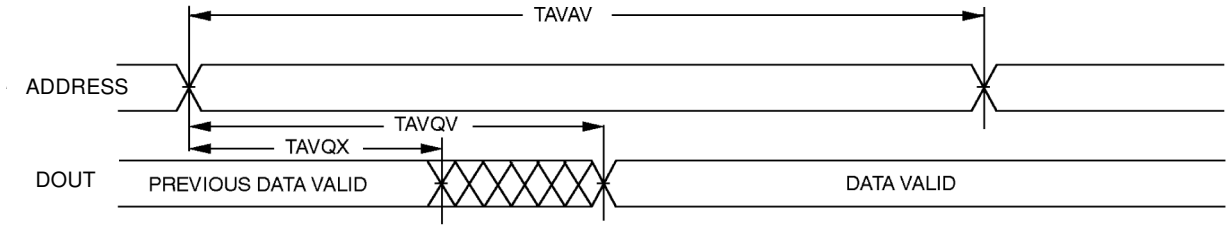
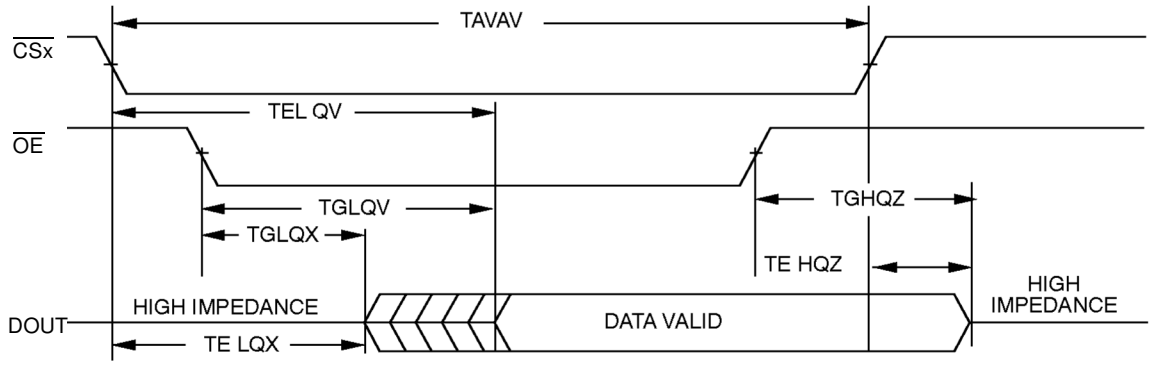


Figure 11. Read Cycle nb 2: Chip Select Controlled ($\overline{WE}$ = V_{IH})



Typical Applications

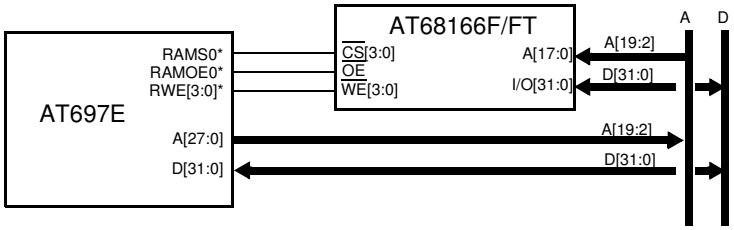
This section presents some standard implementations of the AT68166F/FT in application.

32-bit mode application

When used on a 32-bit (word) application, the module shall be connected as follow :

- The 32 lines of data are connected to distinct data lines
- The four $\overline{CSx}$ are connected together and linked to a single host $\overline{CS}$ output
- Each one of the four $\overline{WE}$x is connected to a dedicated $\overline{WE}$ line on the host to allow byte, half word and word format write.

Figure 12. 32-bit typical application (1 SRAM bank)

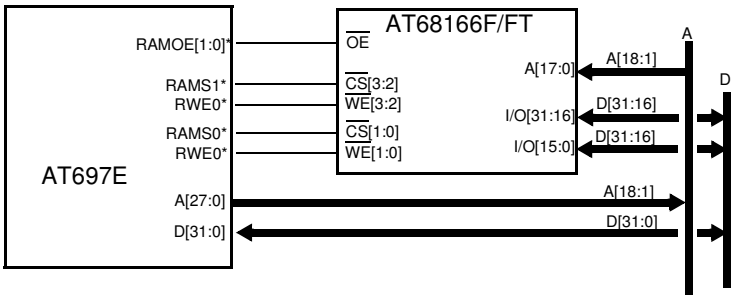


16-bit mode application

When used on a 16-bit (half word) application, the module can be connected as presented in the following figure. This allows use of a single AT68166F/FT part for two SRAM memory banks.

All input controls of the AT68166F/FT not used in the application shall be pulled-up.

Figure 13. 16-bit typical application (two SRAM banks)

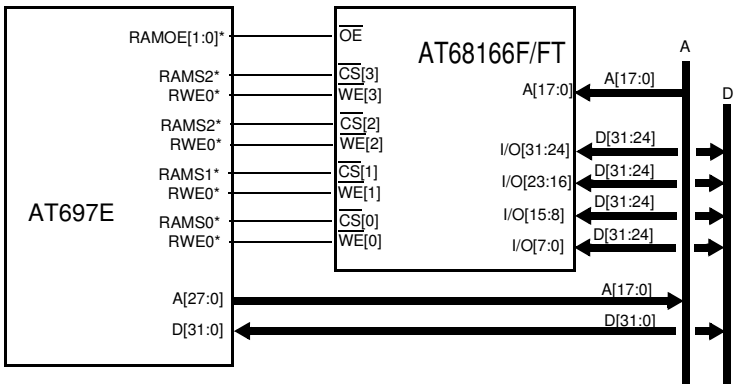


8-bit mode application

When used on a 8-bit (byte) application, the module can be connected as presented in the following figure. This allows use of a single AT68166F/FT part for up to four SRAM memory banks.

All input controls of the AT68166F/FT not used in the application shall be pulled-up.

Figure 14. 8-bit typical application (two SRAM banks)



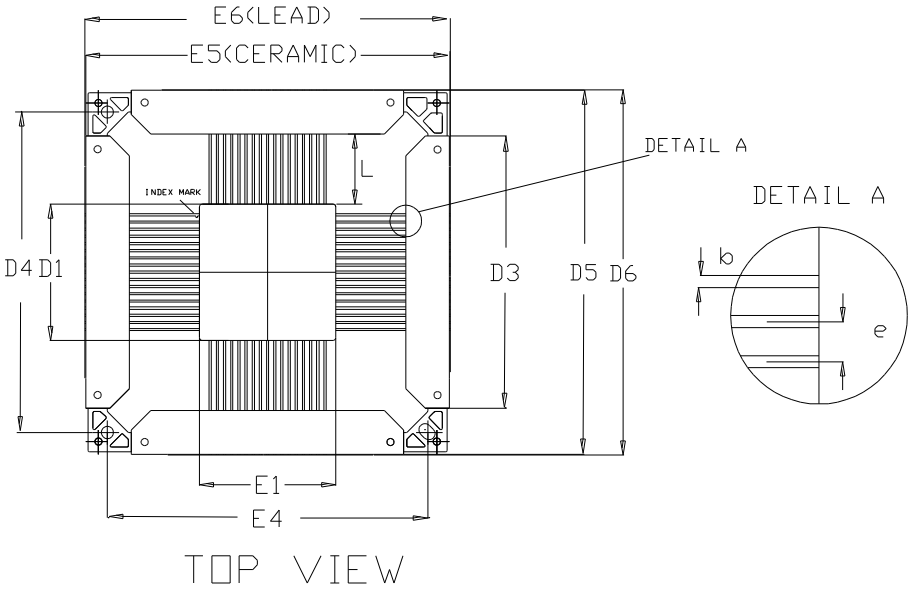
Ordering Information

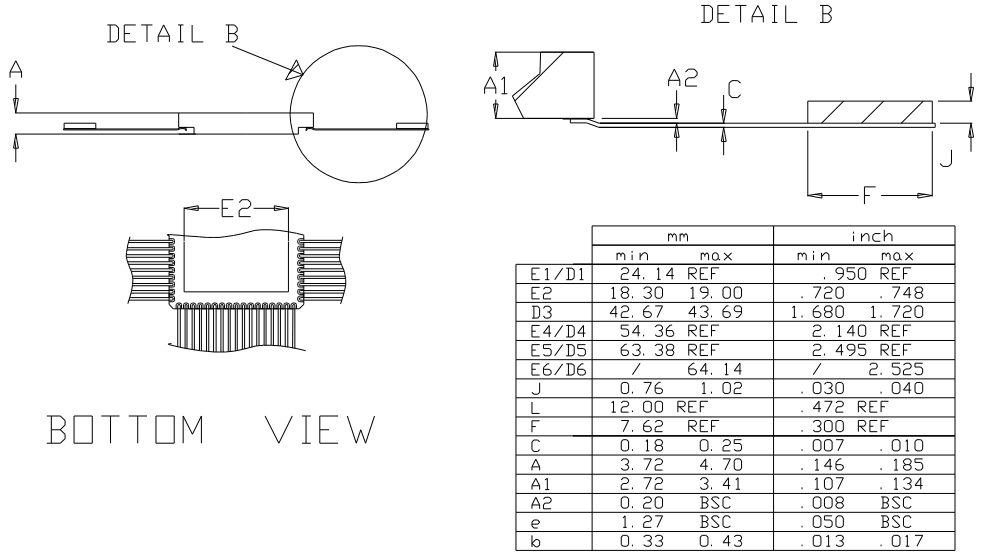
Part Number	Temperature Range	Speed	Package	Flow
AT68166FT				
AT68166FT-YM25-E	25°C	25 ns/5V tol.	MQFPT68	Engineering Samples
5962-0622901QXC	-55° to +125°C	25 ns/5V tol.	MQFPT68	QML Q
5962-0622901VXC	-55° to +125°C	25 ns/5V tol.	MQFPT68	QML V
5962R0622901VXC	-55° to +125°C	25 ns/5V tol.	MQFPT68	QML V RHA
AT68166FT-YM25ESCC	-55° to +125°C	25 ns/5V tol.	MQFPT68	ESCC
AT68166FT-YS20-E(1)	25°C	20 ns/5V tol.	MQFPT68	Engineering Samples
AT68166F				
AT68166F-YM20-E	25°C	20 ns/3.3V	MQFPT68	Engineering Samples
5962-0622902QXC	-55° to +125°C	20 ns/3.3V	MQFPT68	QML Q
5962-0622902VXC	-55° to +125°C	20 ns/3.3V	MQFPT68	QML V
5962R0622902VXC	-55° to +125°C	20 ns/3.3V	MQFPT68	QML V RHA
AT68166F-YM20ESCC	-55° to +125°C	20 ns/3.3V	MQFPT68	ESCC
AT68166F-YS18-E(1)	25°C	18 ns/3.3V	MQFPT68	Engineering Samples

Note: 1. Please contact your local sales office.

Package Drawings

68-lead Quad Flat Pack (950 Mils) with non conductive tie bar





	mm		inch	
	min	max	min	max
E1/D1	24.14 REF		.950 REF	
E2	18.30	19.00	.720	.748
D3	42.67	43.69	1.680	1.720
E4/D4	54.36 REF		2.140 REF	
E5/D5	63.38 REF		2.495 REF	
E6/D6	/	64.14	/	2.525
J	0.76	1.02	.030	.040
L	12.00 REF		.472 REF	
F	7.62 REF		.300 REF	
C	0.18	0.25	.007	.010
A	3.72	4.70	.146	.185
A1	2.72	3.41	.107	.134
A2	0.20 BSC		.008 BSC	
e	1.27 BSC		.050 BSC	
b	0.33	0.43	.013	.017

Note: Lid is connected to Ground.

Note: YM and YS package drawings are identical.

Document Revision History

Changes from 7531C to 7531D

1. Update of access time parameters.

Changes from 7531D to 7531E

1. Added YS package.

Changes from 7531D to 7531E

1. Updated ordering information.

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