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PRELIMINARY

# FM27C010L
# 1,048,576-Bit (128Kx8) Low Power Fast EPROM

## General Description

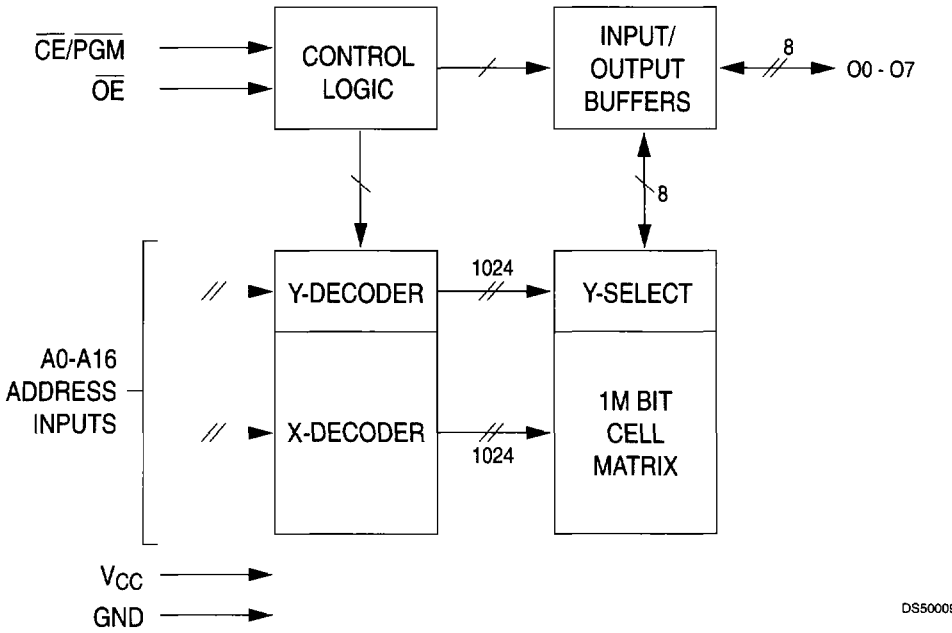
The FM27C010 is a low-power 1Mbit, 5V-only one-time-programmable (OTP) read-only memory (EPROM), organized into 128K words with 8 bits per word. Any byte can be accessed in less than 45ns, eliminating the need for WAIT states in high-performance microprocessor systems. The FM27C010 has separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls which eliminate bus contention issues.

The FM27C010 is one member of a fast EPROM family which range in densities from 256Kb to 1Mb.

## Features

- Fast Read Access Time: -45 and -55ns
- Single 5V Power Supply
- Low Standby Current: 1μA (Typical)
- Programming Voltage +12.75V
- Typical programming time 50μs
- Low Power CMOS Operation
- 30mA Operation (Max.)
- CMOS-and TTL-Compatible I/O
- High-Reliability CMOS Technology
- Latch-Up Immunity to 100mA from -1V to $V_{CC}$ + 1V
- Two-Line Control ($\overline{OE}$ & $\overline{CE}$)
- Standard Product Identification Code
- JEDEC Standard Pinout
  - 32-pin PDIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)
- Commercial and Industrial Temperature Ranges

## Block Diagram




DS500094-1

## Connection Diagrams

| 27C080 | 27C040 | 27C020 | 27C512 | 27C256 |
|---|---|---|---|---|
| $A_{19}$ | XX/$V_{PP}$ | XX/$V_{PP}$ | | |
| $A_{16}$ | $A_{16}$ | $A_{16}$ | | |
| $A_{15}$ | $A_{15}$ | $A_{15}$ | $A_{15}$ | $A_{15}$ |
| $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ |
| $A_7$ | $A_7$ | $A_7$ | $A_7$ | $A_7$ |
| $A_6$ | $A_6$ | $A_6$ | $A_6$ | $A_6$ |
| $A_5$ | $A_5$ | $A_5$ | $A_5$ | $A_5$ |
| $A_4$ | $A_4$ | $A_4$ | $A_4$ | $A_4$ |
| $A_3$ | $A_3$ | $A_3$ | $A_3$ | $A_3$ |
| $A_2$ | $A_2$ | $A_2$ | $A_2$ | $A_2$ |
| $A_1$ | $A_1$ | $A_1$ | $A_1$ | $A_1$ |
| $A_0$ | $A_0$ | $A_0$ | $A_0$ | $A_0$ |
| $O_0$ | $O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $O_1$ | $O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| GND | GND | GND | GND | GND |

DIP
FM27C010-L

| | | | |
|---|---|---|---|
| XX/$V_{PP}$ | 1 | 32 | $V_{CC}$ |
| $A_{16}$ | 2 | 31 | XX/$\overline{PGM}$ |
| $A_{15}$ | 3 | 30 | NC |
| $A_{12}$ | 4 | 29 | $A_{14}$ |
| $A_7$ | 5 | 28 | $A_{13}$ |
| $A_6$ | 6 | 27 | $A_8$ |
| $A_5$ | 7 | 26 | $A_9$ |
| $A_4$ | 8 | 25 | $A_{11}$ |
| $A_3$ | 9 | 24 | $\overline{OE}$ |
| $A_2$ | 10 | 23 | $A_{10}$ |
| $A_1$ | 11 | 22 | $\overline{CE}$ |
| $A_0$ | 12 | 21 | $O_7$ |
| $O_0$ | 13 | 20 | $O_6$ |
| $O_1$ | 14 | 19 | $O_5$ |
| $O_2$ | 15 | 18 | $O_4$ |
| GND | 16 | 17 | $O_3$ |

| 27C256 | 27C512 | 27C020 | 27C040 | 27C080 |
|---|---|---|---|---|
| | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| | | XX/$\overline{PGM}$ | $A_{18}$ | $A_{18}$ |
| $V_{CC}$ | $V_{CC}$ | $A_{17}$ | $A_{17}$ | $A_{17}$ |
| $A_{14}$ | $A_{14}$ | $A_{14}$ | $A_{14}$ | $A_{14}$ |
| $A_{13}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ |
| $A_8$ | $A_8$ | $A_8$ | $A_8$ | $A_8$ |
| $A_9$ | $A_9$ | $A_9$ | $A_9$ | $A_9$ |
| $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ |
| OE | OE/$V_{PP}$ | OE | OE | OE/$V_{PP}$ |
| $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ |
| CE/PGM | CE/PGM | CE | CE/PGM | CE/PGM |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ | $O_3$ |

DS500094-2

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the FM27C010 pins.

## Commercial Temperature Range (0°C to +70°C) $V_{CC}$ = 5V ± 10%

| Parameter/Order Number | Access Time (ns) |
|---|---|
| FM27C010 N, T, V 45 L | 45 |
| FM27C010 N, T, V 55 L | 55 |

## Industrial Temperature Range (-40°C to +85°C) $V_{CC}$ = 5V ± 10%

| Parameter/Order Number | Access Time (ns) |
|---|---|
| FM27C010 NE, TE, VE 45 L | 45 |
| FM27C010 NE, TE, VE 55 L | 55 |

Note 1: All versions are guaranteed to function for slower speeds.

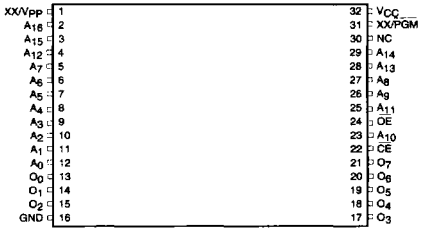
Package Types:
- N = Plastic DIP Package
- T = TSOP Package
- V = PLCC Package

All packages conform to the JEDEC standard

## Pin Names

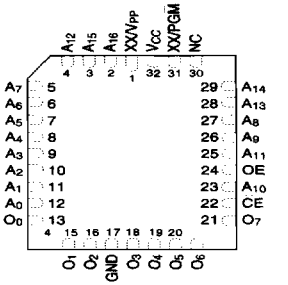
| Pin Name | Function |
|---|---|
| $A_0$-$A_{16}$ | Addresses |
| $O_0$-$O_7$ | Outputs |
| $\overline{PGM}$ | Program |
| $\overline{OE}$ | Output Enable |
| NC | No Connect |
| $\overline{CE}$ | Chip Enable |

### TSOP Pin Configuration




DS500094-5

### PLCC Pin Configuration




DS500094-4

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Storage Temperature | -65°C to +125°C |
| All Input Voltage except A9 with Respect to Ground | -0.6V to +7V |
| $V_{PP}$ and A9 with Respect to Ground | -0.6V to +13.5V |
| $V_{CC}$ Supply Voltage with Respect to Ground | -0.6V to +7V |
| ESD Protection (MIL St. 883, Method 3015.2) | >2000V |
| All Output Voltages with Respect to Ground | -0.6V to $V_{CC}$ + 0.5V |

## Operating Range

| Range | Temperature ($T_C$) | $V_{CC}$ | Tolerance |
|---|---|---|---|
| Commercial | 0°C to +70°C | +5V | ±10% |
| Industrial | -40°C to +85°C | +5V | ±10% |

## Read Operation

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -0.4mA | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.45 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 to $V_{CC}$ | -5 | 5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0 to $V_{CC}$ | -10 | 10 | µA |
| $I_{CC3}$ | $V_{CC}$ Power-Down Current | $\overline{CE}$ = $V_{CC}$ ± 0.3V | | 10 | µA |
| $I_{CC2}$ | $V_{CC}$ Standby Current | $\overline{CE}$ = $V_{IH}$ | | 1 | mA |
| $I_{CC1}$ | $V_{CC}$ Active Current | $\overline{CE}$ = $V_{IL}$, f = 5MHz, $I_{OUT}$ = 0mA | | 30 | mA |
| $I_{PP}$ | $V_{PP}$ Supply Current Read | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $V_{PP}$ = $V_{CC}$ | | 100 | µA |

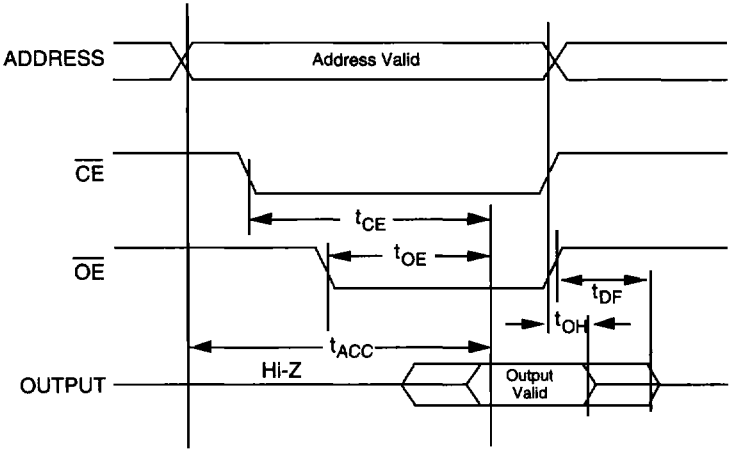
## AC Electrical Characteristics

| Symbol | Parameter | -45 | | -55 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | | 45 | | 55 | ns |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | | 45 | | 55 | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay | | 25 | | 25 | ns |
| $t_{DF}$ | $\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first | | 20 | | 20 | ns |
| $t_{OH}$ | Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First | 0 | | 0 | | ns |

## Capacitance $T_A = 25°C$, f = 1MHz

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance Except $\overline{OE}/V_{PP}$ | $V_{IN} = 0V$ | 8 | 12 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | 8 | 12 | pF |
| $V_{PP}$ | $\overline{OE}/V_{PP}$ Input Capacitance | $V_{IN} = 0V$ | 18 | 25 | pF |

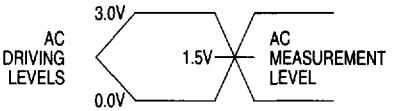
## AC Waveforms for Read Operation




DS500094-6

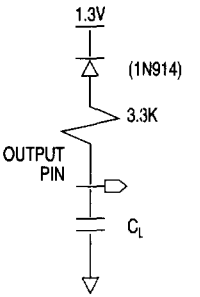
## Output Test Waveforms and Measurements

**45 and 55 Devices**




$t_R$, $t_F$ < 5 ns (10% to 90%)

**Output Test Load**




**Note:** $C_L$ = 30pF including jig capacitance

DS500094-7

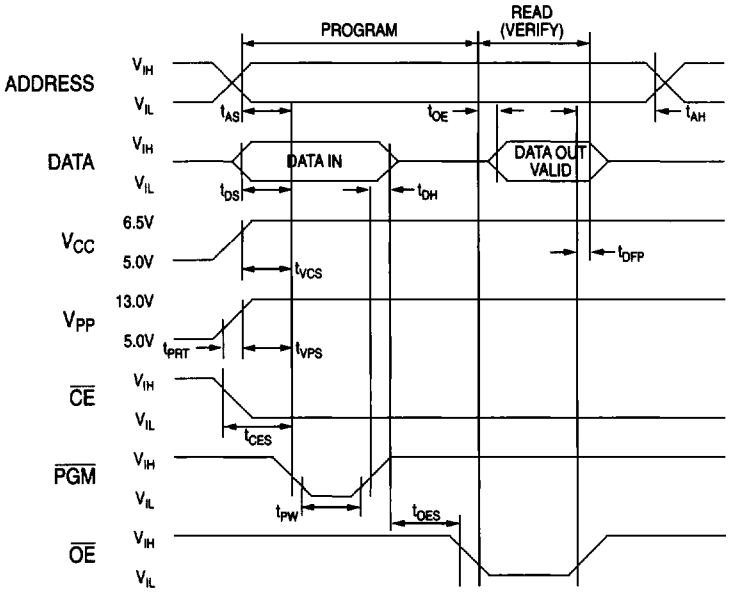
## DC Programming Characteristics

| Sumbol | Parameter | Test Conditions | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | 5.0 | µA |
| $V_{IL}$ | Input Low Level | | -0.5 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.4 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current | | | 40 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current | $\overline{CE} = \overline{PGM} = V_{IL}$ | | 10 | mA |
| $V_{ID}$ | A9 Product ID Voltage | | 11.5 | 12.5 | V |
| $V_{PP}$ | Programming Supply Voltage | | 12.5 | 13.0 | V |
| $V_{CC}$ | Power Supply Voltage | | 6.25 | 6.75 | V |

## Switching Programming Characteristics ($T_A$ = +25° ± 5°C)

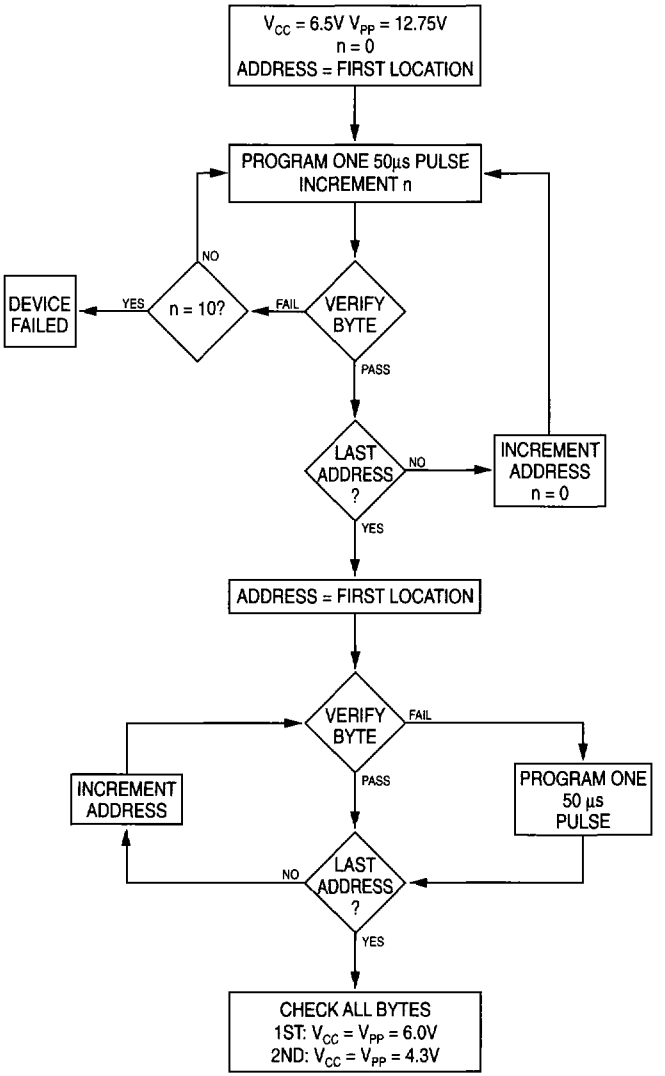
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AS}$ | Address Setup Time | 1 | | µs |
| $t_{OES}$ | $\overline{OE}/V_{PP}$ Setup Time | 1 | | µs |
| $t_{DS}$ | Data Setup Time | 1 | | µs |
| $t_{AH}$ | Address Hold Time | 0 | | µs |
| $t_{DH}$ | Data Hold Time | 1 | | µs |
| $t_{DFP}$ | Output Enable to Output Float Delay | 0 | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | 1 | | µs |
| $t_{PW}$ | $\overline{PGM}$ Program Pulse Width | 20 | 105 | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | 1 | | µs |
| $t_{CES}$ | $\overline{CE}$ Setup Time | 1 | | µs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | 150 | ns |

## Programming Waveforms




DS500094-8

## Turbo Programming Algorithm Flow Chart




DS500094-9

**Figure 1**

**Note:** National Semiconductor NM27C010 Fast Programming Algorithm may also be used.

## Functional Description

### Device Operation

The modes of operation of the EPROM are listed in Table 1. The power supplies required are $V_{CC}$ and $\overline{OE}/V_{PP}$. The $\overline{OE}/V_{PP}$ power supply must be at 12.75 during the three programming modes, and must be at 5V in the other three modes. The $V_{CC}$ power must be at 6.5V during the three programming modes, and at 5V in the other three modes.

### Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs $t_{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### Standby Mode

The FM27C010 has CMOS standby mode which reduces the maximum $V_{CC}$ current to 1µA (typical). It is placed in CMOS standby when $\overline{CE}$ is at $V_{CC} \pm 0.3V$. The FM27C010 also has a TTL standby mode which reduces the maximum $V_{CC}$ current to 1.0 mA. It is placed in TTL standby when $\overline{CE}$ is at $V_{IH}$. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

### Two-Line Output Control Function

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selection function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### Programming

Caution: Exceeding 13.5V on pin 22 ($\overline{OE}/V_{PP}$) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ power supply is at 12.75V. it is required that at least a 0.1µf capacitor be placed across $V_{CC}$ to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address locaiton to be programmed.

The EPROM is programmed with the Turbo Programming Algorithm shown in Figure 1. Each Address is programmed with a series of 50µs pulses until it verifies good, up to a maximum of 10 pulses. Most memory cells will program with a single 50µs pulse. The Turbo Programming Algorithm will be available in early Quarter 1, 1998. Until this program is installed the EPROM may be programmed using National Semiconductor NM27C010 Fast Programming Algorithm.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled EPROM.

### Program Inhibit Mode

Programming of multiple FM27C010 in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for CE, all like inputs of the parallel FM27C010 may be common. A TTL low-level program pulse appled to a FM27C010 CE input with $\overline{OE}/V_{PP} = 12.75 \pm 0.25V$ will program that FM27C010. A high-level CE input inhibits the other FM27C010 from being programmed.

### Program Verify Mode

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at $V_{IL}$. Data should be verified at $t_{DV}$ after the falling edge of $\overline{CE}$.

## System Consideration

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and $V_{SS}$ to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7µF bulk electrolytic capacitor should be used between $V_{CC}$ and $V_{SS}$ for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## Mode Selection

The modes of operation of the FM27C010 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $V_{PP}$ and A9 for device signature.

## Functional Description (Continued)

**Table 1. Mode Selection**

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | A0 | A1 | A9 | $V_{PP}$ | Output |
|---|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | X (Note 2) | X | X | X | $V_{CC}$ | $D_{OUT}$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | X | X | X | X | $V_{CC}$ | High Z |
| Standby (TTL) | $V_{IH}$ | X | X | X | X | X | $V_{CC}$ | High Z |
| Standby (CMOS) | $V_{CC} \pm 0.3V$ | X | X | X | X | X | $V_{CC}$ | High Z |
| Program (Note 4) | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | X | $V_{PP}$ | $D_{IN}$ |
| Program Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | X | $V_{PP}$ | $D_{OUT}$ |
| Program Inhibit | $V_{IH}$ | X | X | X | X | X | $V_{PP}$ | High Z |
| Manufacturer Code (Note 3) | $V_{IL}$ | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | VH (Note 1) | $V_{CC}$ | |
| Device Code (Note 3) | $V_{IL}$ | X | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | VH (Note 1) | $V_{CC}$ | |

Note 1: VH = 12.0V ± 0.5V.

Note 2: X = Either $V_{IH}$ or $V_{IL}$.

Note 3: For Manufacturer Code and Device Code, A1 = $V_{IH}$
When A1 = $V_{IL}$, both codes will read 7F.

Note 4: See DC Programming Characteristics for $V_{PP}$ voltage during programming.

**Table 2. Manufacturer's Identification Code**

| Pins / Code | A0 | A1 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1C |
| Device Type | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Continuation | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F |
| | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F |

## Ordering Information

FM27C010 N E 45 L

**Low Standby Current**

**Speed**
45 = 45ns
55 = 55ns

**Temperature Range**
(Blank) = Commercial (0°C to +70°C)
E = Industrial (-40°C to +85°C)

**Package**
N = 32 Plastic DIP
V = 32 Plastic PLCC
T = 32 Plastic TSOP

**Base Part Number**
FM = Fairchild Memory device
27 = EPROM
C = CMOS
010 = 128K x 8

DS500094-10