

32K x 68-bit Entry NETWORK SEARCH ENGINE

Figure 1. 272-ball PBGA Package

DATA BRIEFING

FEATURES SUMMARY

- 32K DATA ENTRIES IN 68-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO FOUR (4) QUADRANTS (Data entry width in each octant is configurable as 34, 68, 136, or 272 bits.)
- UP TO 83 MILLION SUSTAINED SEARCHES PER SECOND IN 68-BIT and 136-BIT CONFIGURATIONS
- UP TO 41.5 MILLION SEARCHES PER SECOND IN 34-BIT and 272-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 248K TO 1984K DEPENDING ON THE WIDTH OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE: V_{DD} (Operating Supply Voltage) = 1.8V V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 272 PBGA, 27mm x 27mm

272-ball PBGA

27mm x 27mm

December 2001 1/6

DESCRIPTION

Overview

ST Microelectronics, Inc.'s M7020R Search Engine incorporates patent-pending Associative Processing Technology™ (APT) and is designed to be a high-performance, pipelined, synchronous, 32K-entry network database search engine. The M7020R database entry size can be 68 bits, 136 bits, or 272 bits. In the 68-bit entry mode, the size of the database is 32K entries. In the 136-bit mode, the size of the database is 16K entries, and in the 272-bit mode, the size of the database is 8K entries. The M7020R is configurable to support multiple databases with different entry sizes. The 34-bit entry table can be implemented using the Global Mask Registers (GMRs) building-database size of 64K entries with a single device.

Performance

The Search Engine can sustain 83 million transactions per second when the database is programmed or configured as 68 or 136 bits. When the database is programmed to have an entry size

of 34 or 272 bits, the Search Engine will perform at 41.5 million transactions per second. STM's M7020R can be used to accelerate network protocols such as Longest-prefix Match (CIDR), ARP, MPLS, and other Layer 2, 3, and 4 protocols.

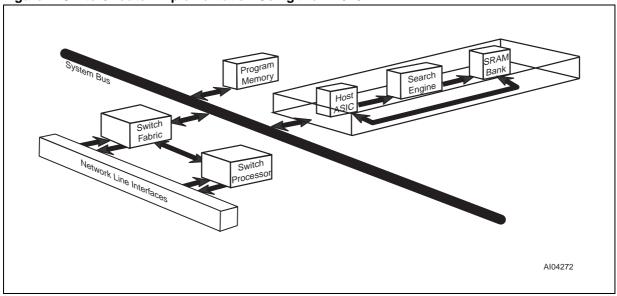
Applications

This high-speed, high-capacity Search Engine can be deployed in a variety of networking and communications applications. The performance and features of the M7020R make it attractive in applications such as Enterprise LAN switches and routers and broadband switching and/or routing equipment supporting multiple data rates at OC–48 and beyond. The Search Engine is designed to be scalable in order to support network database sizes to 1984K entries specifically for environments that require large network policy databases. Figure 4, page 5 shows the block diagram for the M7020R device.

Table 1. Product Range

Part Number	Operating Supply Voltage	Operating I/O Voltage	Speed	Temperature Range
M7020R-083ZA1	1.8V	2.5 or 3.3V	83MHz	Commercial
M7020R-066ZA1	1.8V	2.5 or 3.3V	66MHz	Commercial
M7020R-050ZA1	1.8V	2.5 or 3.3V	50MHz	Commercial

Figure 2. Switch/Router Implementation Using the M7020R



2/6

Table 2. Signal Names

Symbol	Type ⁽¹⁾	Description							
Clocks and Reset									
CLK2X	1	Master Clock							
PHS_L	I	Phase							
TEST	I	Test Input							
RST_L	- 1	Reset							
C	ommand	and DQ Bus							
CMD[8:0]	I	Command Bus							
CMDV	- 1	Command Valid							
DQ[67:0]	I/O	Address/Data Bus							
ACK ⁽⁴⁾	Т	READ Acknowledge							
EOT ⁽⁴⁾	Т	End of Transfer							
SSF	Т	SEARCH Successful Flag							
SSV	Т	SEARCH Successful Flag Valid							
SRAM Interface									
SADR[21:0]	Т	SRAM Address							
CE_L	Т	SRAM Chip Enable							
WE_L	Т	SRAM Write Enable							
OE_L	Т	SRAM Output Enable							
ALE_L	Т	Address Latch Enable							

	Cascade	Interface					
LHI[6:0]	I	Local Hit In					
LHO[1:0]	0	Local Hit Out					
BHI[2:0]	I	Block Hit In					
BHO[2:0]	0	Block Hit Out					
FULI[6:0]	I	Full In					
FULO[1:0]	0	Full Out					
FULL	0	Full Flag					
	Device Ide	entification					
ID[4:0] I Device Identification							
	Sup	plies					
V_{DD}	n/a	Chip Core Supply (1.8V)					
V_{DDQ}	n/a	Chip I/O Supply (2.5 or 3.3V)					
	Test Ac	cess Port					
TDI I Test Access Port's Test Data In							
тск	I	Test Access Port's Test Clock					
TDO	Т	Test Access Port's Test Data Out					
TMS	I	Test Access Port's Test Mode Select					
TRST_L	I	Test Access Port's Reset					

Note: 1. Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate
2. "CLK" is an internal clock signal. Any reference to "CLK Cycles" means one cycle of CLK.
3. ACK and EOT Signals require a weak, external pull-down resistor of 47 KΩ or 100 KΩ.

Figure 3. Connections

NC	GND	EOT	NC	NC	V_{DD}	FULI5	FULI4	FULI1	вноо	V_{DD}	BHI0	LHI6	NC	V_{DD}	ID2	ID0	TDO	NC	NC
NC	NC	ACK	FULL	NC	FULO1	NC	FULI6	FULI2	вно1	BHI2	V_{DDQ}	LHI5	LHI3	LHI2	ID3	TMS	TDI	V _{DD}	N
DQ64	NC	NC	V _{DDQ}	V _{DD}	V_{DDQ}	NC	NC	V_{DDQ}	вно2	V _{DD}	LHO1	LHI4	V_{DDQ}	LHI0	ID1	TCK	NC	NC	DQ
DQ62	NC	V _{DD}	GND	RSTL	NC	FULO0	GND	FULI3	FULI0	BHI1	LHO0	GND	LHI1	ID4	T RST_L	GND	DQ63	DQ61	DQ
DQ60	V_{DDQ}	NC	DQ66		ТОР											DQ67	DQ59	NC	DQ
V_{DD}	NC	DQ56	DQ58									V _{DDQ}	DQ55	DQ49	٧٢				
DQ50	V_{DDQ}	DQ52	DQ54													DQ47	V_{DDQ}	DQ51	۷ _D
NC	DQ46	DQ48	GND													GND	NC	DQ45	DQ
DQ40	DQ42	V_{DDQ}	DQ44					GND	GND	GND	GND					DQ41	DQ39	V _{DD}	DG
V_{DD}	NC	DQ36	DQ38	LEFT				GND	GND	GND	GND			R	IGHT	V_{DDQ}	DQ35	DQ33	DG
V _{DDQ}	DQ34	DQ32	DQ30					GND	GND	GND	GND				10111	V_{DDQ}	NC	DQ29	٧
NC	DQ28	V_{DDQ}	DQ26					GND	GND	GND	GND					NC	DQ23	DQ25	DC
DQ24	V _{DD}	DQ20	GND													GND	DQ19	V _{DDQ}	DC
DQ22	DQ16	DQ14	V_{DDQ}												V_{DDQ}	NC	DQ15	DQ	
V_{DD}	DQ18	V_{DDQ}	DQ6													DQ9	DQ11	DQ13	٧
NC	DQ12	DQ8	DQ0					воттом							DQ1	DQ5	DQ7	N	
DQ10	NC	V_{DDQ}	GND	NC	CMD4	CMD2	GND	WE_L	CLK2X	V_{DD}	SADR 15	GND	V_{DDQ}	SADR 5	V _{DDQ}	GND	NC	NC	٧ _D
DQ2	DQ4	V _{DD}	SSF	CMD6	CMD3	CMD0	AE_L	OE_L	SADR 21	SADR 18	SADR 16	SADR 12	SADR 9	SADR 7	SADR 6	NC	SADR 0	V _{DD}	DO
NC	NC	NC	SSV	CMD5	CMD1	CMDV	V _{DDQ}	PHS_L	V_{DDQ}	SADR 19	V_{DDQ}	NC	SADR 10	SADR 11	NC	SADR 4	SADR 3	NC	N
NC	NC	CMD8	CMD7	V _{DDQ}	V _{DD}	NC	CE_L	NC	V _{DD}	SADR 20	SADR 17	SADR 14	SADR 13	V_{DD}	SADR 8	V _{DDQ}	SADR 2	SADR 1	N

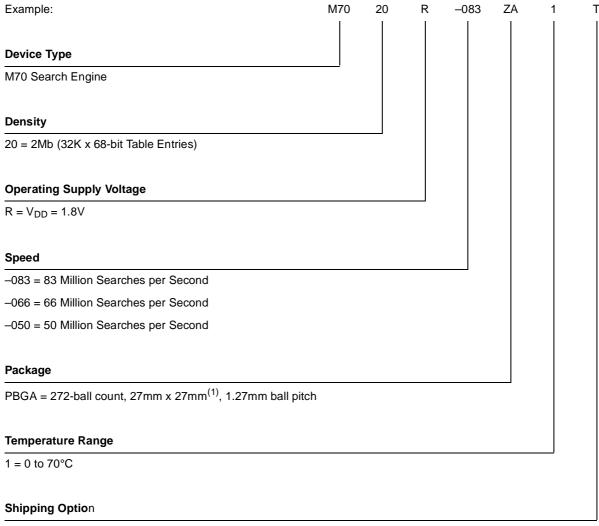
4/6

PHS_L -Comparand Registers[15:0] Global Mask Registers [7:0] CLK2X -RST_L → Information and Command Register **Burst Read Register** Burst Write Register Next Free Address Register Search Successful Index Registers [7:0] Compare/PIO Data (All registers are 68-bit-wide) TAP TAP Controller DQ [67:0] Compare/PIO Data Configurable as SADR [21:0] 64K x 34 32K x 68 CMD [8:0] · 16K x 136 OE_L Command Address Decode Pipeline CMDV -Priority Encode Decode 8K x 272 Match Logic and and PIO Access Data Array ACK ◀ SRAM WE_L Control EOT ◀ Configurable as 64K x 34 CE_L 32K x 68 16K x 136 ALE_L ID [4:0] 8K x 272 Mask Array FULL [6:0] -Full Logic LHI [6:0] -**FULL** LHO [1:0] BHI [2:0] -Arbitration BHO [2:0] Logic SSF FULO [1:0] SSV AI04271

Figure 4. M7020R Block Diagram

PART NUMBERING





Tape & Reel Packing = T

Note: 1. Where "Z" is the symbol for BGA packages and "A" denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

6/6