Contents

CMOS 2K/4K-bit SERIAL E^{2}PROM — S-29255A/29355A

The S-29255A (2K-bit) and S-29355A (4K-bit) are E^{2}PROMs characterized by a wide operating voltage range and low power consumption. The organization is 128-word×16-bit and 256-word×16-bit, respectively. They are easily interfaced with a serial port because the instruction is composed of eight-bit units. Also, through the RESET pin, erroneous writing at power on/off can be avoided.

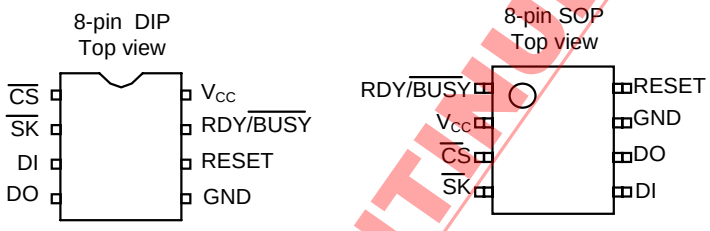
■ Features

- S-29255A : 2K-bit, instruction code conforming to M6M80021
  S-29355A : 4K-bit, instruction code conforming to M6M80041
- Low power consumption Operating: 2.0 mA max.
  Standby: 1.0 µA max.
- Wide operating voltage range Write: 2.7 to 6.5 V
  Read: 1.8 to 6.5 V
- Easy interface with serial port
- Memory protection by RESET pin
- Rewritings: 10^5 times/word
- Data retention: 10 years
- Operating temperature: -40 °C to+85 °C
- Package: 8-pin DIP/SOP, bare chip

■ Package

- 8-pin DIP (PKG drawing code : DP008-A)
- 8-pin SOP (PKG drawing code : FE008-A)

■ Pin Assignment



$\overline{CS}$	Chip select
$\overline{SK}$	Serial clock
DI	Serial data input
DO	Serial data output
V_{CC}	Power supply voltage
GND	Ground
RDY/$\overline{BUSY}$	Ready output/Busy output
RESET	Reset input L : Stable Status H : Reset write circuit (Memory protection)

Figure 1

■ Block Diagram

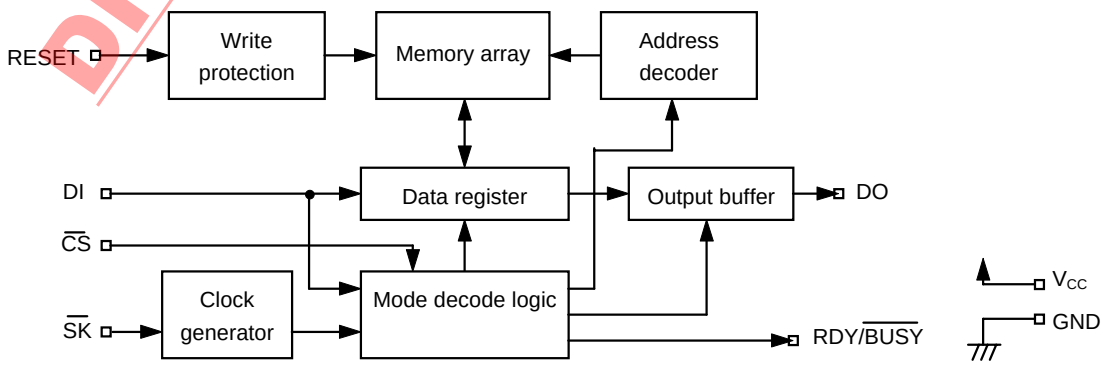


Figure 2

■ Instruction Set

Table 1

Instruction		Op code	Address		Data
			S-29255A	S-29355A	
READ (Read data)		10101000	A_0 to A_6 0	A_0 to A_7	D_0 to D_{15}
PROGRAM (Program)		10100100	A_0 to A_6 0	A_0 to A_7	D_0 to D_{15}
WRAL (Write all)*		10100001	A_0 to A_6 0	A_0 to A_7	D_0 to D_{15}
ERAL (Erase all)*		10100010	xxxxxxxx	xxxxxxxx	—
EWEN (Program enable)		10100011	xxxxxxxx	xxxxxxxx	—
EWDS (Program disable)		10100000	xxxxxxxx	xxxxxxxx	—
Status output	Busy flag	10101001	00xxxxxx	00xxxxxx	0 : BUSY 1 : READY
	Write permission		10xxxxxx	10xxxxxx	0 : Permission 1 : Inhibit
	ECC flag		01xxxxxx	01xxxxxx	"0" is always output**

x : Doesn't matter

* : ERAL and WRAL are options. Normally these can not be used.

** : S-29255A/29355A doesn't have redundant memory.

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to+95	°C
Storage temperature	T_{stg}	-65 to+150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read		1.8	—	6.5	V
		Write		2.7	—	6.5	V
High level input voltage	V_{IH}	V_{CC}=2.7 to 6.5V	$\overline{CS}$, $\overline{SK}$	0.8×V_{CC}	—	V_{CC}	V
			DI, RESET	0.7×V_{CC}	—	V_{CC}	V
		V_{CC}=1.8 to 2.7V		0.8×V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC}=2.7 to 6.5V	$\overline{CS}$, $\overline{SK}$	0.0	—	0.2×V_{CC}	V
			DI, RESET	0.0	—	0.3×V_{CC}	V
		V_{CC}=1.8 to 2.7V		0.0	—	0.2×V_{CC}	V
Operating temperature	T_{opr}			-40	—	+85	°C

■ Rewriting Times

Table 4

(Ta=-40°C to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rewriting times	N_W	10^5	—	—	times/word

■ Pin Capacitance

Table 5

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V	—	—	8	pF
Output capacitance	C_{OUT}	V_{OUT}=0 V	—	—	10	pF

■ DC Electrical Characteristics

Table 6

(Ta=-40°C to 85°C)

Parameter	Smbl	Conditions	Read/write operations						Read operation			Unit
			V_{CC}=5.0 V±10 %			V_{CC}=3.0 V±10 %			V_{CC}=1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	2.0	—	—	1.0	—	—	0.5	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	5.0	—	—	2.0	—	—	—	mA

Table 7

(Ta=-40°C to 85°C)

Parameter	Smbl	Conditions	Read/write operations						Read operation			Unit
			V_{CC}=5.0 V±10 %			V_{CC}=2.7 to 6.5 V			V_{CC}=1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	Input: V_{CC} or GND	—	—	1.0	—	—	1.0	—	—	1.0	µA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Low level output voltage	V_{OL}	CMOS I_{OL}=100 µA	—	—	0.1	—	—	0.1	—	—	0.1	V
		TTL I_{OL}=2.1 mA	—	—	0.45	—	—	--	—	—	—	V
High level output voltage	V_{OH}	CMOS V_{CC}=2.7 to 6.5 V: I_{OH}=-100 µA V_{CC}=1.8 to 2.7 V: I_{OH}=-10 µA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—	V
		TTL I_{OH}=-400 µA	2.4	—	—	—	—	—	—	—	—	V
Write enable latch data hold voltage	V_{DH}		1.5	—	—	1.5	—	—	1.5	—	—	V
Schmitt width	V_{WD}	$\overline{CS}$, SK	V_{CC}×0.1	—	—	V_{CC}×0.1	—	—	0.05	—	—	V

■ AC Electrical Characteristics

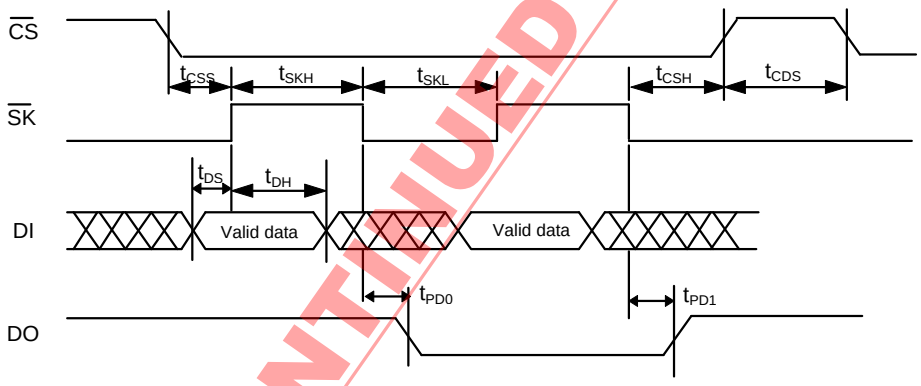
Table 8 Measuring conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Output reference voltage	$0.5\times V_{CC}$
Output load	100 pF

Table 9

(Ta=-40°C to 85°C)

Parameter	Symbol	Read / Write operations						Read operation			Unit
		V_{CC}=5.0 V±10 %			V_{CC}=2.7 to 6.5 V			V_{CC}=1.8 to 2.7 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{CS}$ setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ setup time (CPU)	$t_{CSS(CPU)}$	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ hold time (CPU)	$t_{CSH(CPU)}$	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ deselect time	t_{CDS}	0.4	—	—	1.0	—	—	2.0	—	—	µs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	µs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	µs
1 data output delay	t_{PD1}	—	—	0.4	—	—	1.0	—	—	2.0	µs
0 data output delay	t_{PD0}	—	—	0.4	—	—	1.0	—	—	2.0	µs
Clock frequency	f_{SK}	0.0	—	2.0	0.0	—	1.0	0.0	—	0.2	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.25	—	—	0.5	—	—	2.5	—	—	µs
Output disable time	t_{HZ}	0	50	150	0	500	1000	—	—	—	ns
Program time	t_{PR}	—	4.0	10	—	4.0	10	—	—	—	ms



Input data is fetched at the rise of $\overline{SK}$.
Output data is triggered at the fall of $\overline{SK}$.

Figure 3 Timing chart

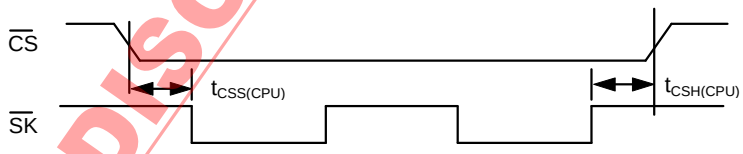
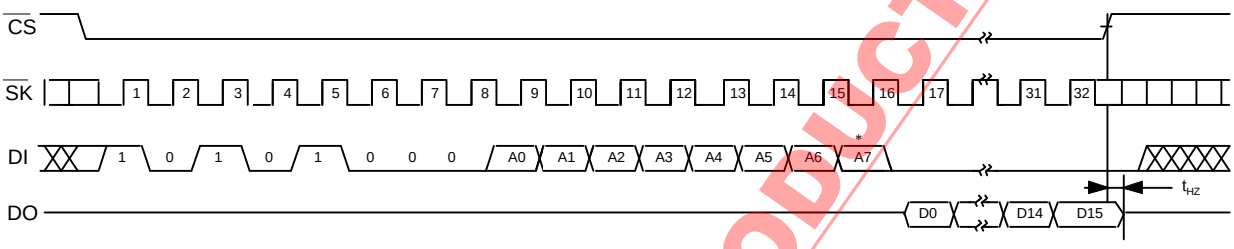


Figure 4 Timing chart of $t_{CSS(CPU)}$ and $t_{CSH(CPU)}$ when connected to CPU

■ Operation

For each instraction, input op code, address and data per Table 1. After $\overline{CS}$ goes from "H" to "L", DI is latched, synchronized with the rise of $\overline{SK}$. After the entire data is latched, the instructions input can be completed by changing $\overline{CS}$ to "H". Even after changing $\overline{CS}$ to low, instructions can not be latched by inputting a pulse to $\overline{SK}$ while DI remains low.
NOTE: Between instructions, $\overline{CS}$ must be "H" during $t_{CDS.}$

1. Read mode (READ)
The READ instruction reads data from the specified address.
Through the READ instruction, the op code and address are latched, synchronized with the rise of $\overline{SK}$. At the falling edge of the 16th $\overline{SK}$ clock cycle from the start bit, (and all of the addresses are input), DO changes from high impedance (Hi-Z) status to data output status, and data is output, synchronized with the fall of $\overline{SK}$.



* "L" for S-29255A.

2. Write mode (PROGRAM, WRAL, and ERAL)
There are three write instructions, PROGRAM, WRAL, and ERAL. Each write instruction automatically starts the write operation to nonvolatile memory after completing the specified clock input. The write operation is completed in 10 ms (tPR max.) , and the average write period is 4 to 5 ms.
The S-29255A/29355A offer the following two methods to check the completion of the write operation to choose the shortest writing cycle.

- By reading the status of the RDY/$\overline{BUSY}$ output pin
  While the write operation is continued, low level is output. And when the write operation is completed, high level is output.
- By reading the status output signal
  After inputting a write instruction, a status output instruction must be performed (for the status output instruction, refer to "4. Status output") .
  NOTE:
  - After starting the write operation, $\overline{CS}$ need not be "H".
  - During the write operation, no instruction can be accepted except for status output. When using $\overline{SK}$ or DI during the write operation, the $\overline{SK}$ and DI signals should not be a status output instruction, or, $\overline{CS}$ must be "H".
  - The write operation can be performed when the RESET pin is at "L". After RESET is "H", even during write operation, the write operation is terminated, and data is unstable. Therefore, when writing is not performed, fix the RESET pin at "H" to inhibit all write operation and to avoid erroneous writing.
  - When the status output instruction is input after the write instruction, $\overline{CS}$ need not be "H".

2.1 Program (PROGRAM) mode

This mode writes 16-bit data to the specified address. After $\overline{CS}$ goes to "L", input op code, address, and 16-bit data. The write operation starts at the rising edge of the 32nd $\overline{SK}$ clock cycle from the start bit.
It is not necessary to make the data be "1" before the data write operation.

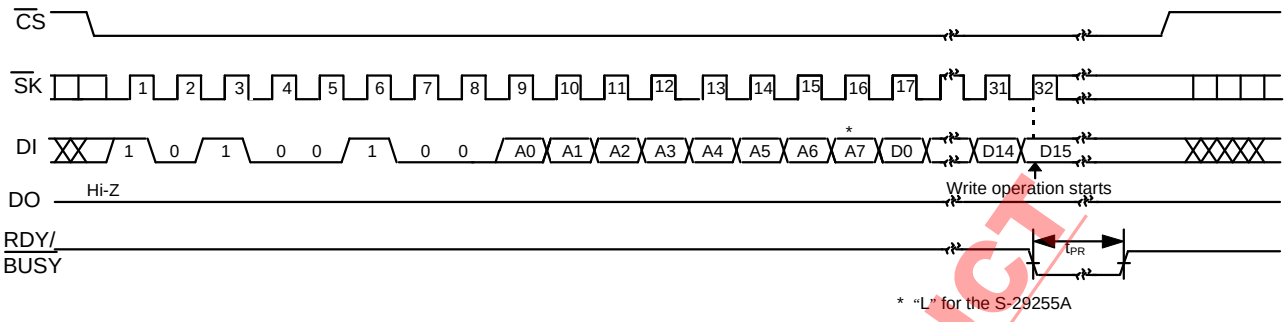


Figure 6

2.2 Write all (WRAL) mode: option

The same 16-bit data is written into all address areas in the memory. After $\overline{CS}$ changes from "H" to "L", input the op code, address, and 16-bit data. The write operation starts at the rising edge of the 32nd $\overline{SK}$ clock cycle from the start bit.
It is not necessary to make the data be "1" before the data write operation.

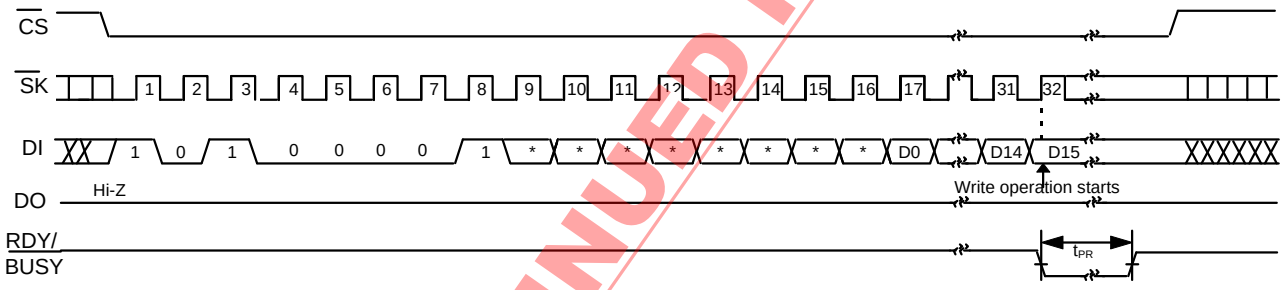


Figure 7

2.3 Erase all (ERAL) mode: option

Data in all address areas is erased. After erasing the data, all of the data is set to "1". After $\overline{CS}$ changes from "H" to "L", input the op code and address. The erase operation starts at the rising edge of the 16th $\overline{SK}$ clock cycle from the start bit.

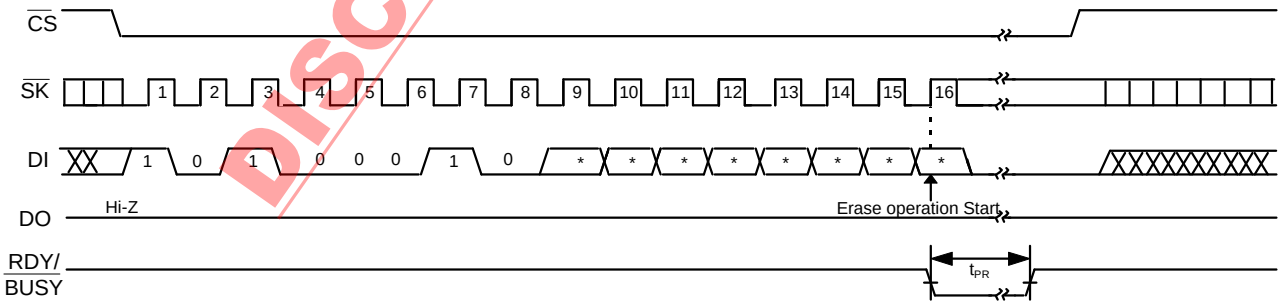


Figure 8

3. Program enable (EWEN) and program disable (EWDS) modes

EWEN enables the write operation, and EWDS disables the write operation. The status to enable the write operation is called the program enable mode, and the status to disable the write operation is called the program disable mode. The S-29255A/29355A is in program disable mode when the power is turned on.

To prevent unexpected erroneous writing because of noise and CPU runaway, the S-29255A/29355A should be in program disable mode when writing is not performed.

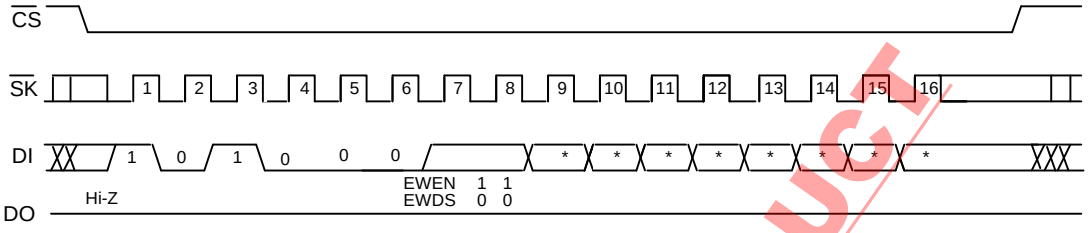


Figure 9

4. Status output

The status output instruction outputs several kinds of IC inside status (ready/busy, write inhibit/permit, and ECC set). Through the status output instruction, the op code and flag set code are latched, synchronized with the rise of $\overline{SK}$. At the falling edge of 16th clock cycle from the start bit, DO is changed from high impedance (Hi-Z) status to data output status, and the data that shows the IC inside status is output synchronized with the fall of $\overline{SK}$. The data is retained until $\overline{CS}$ goes to "H".

NOTE : Even if the $\overline{SK}$ and DI inputs are changed when outputting data, the output data is not changed.

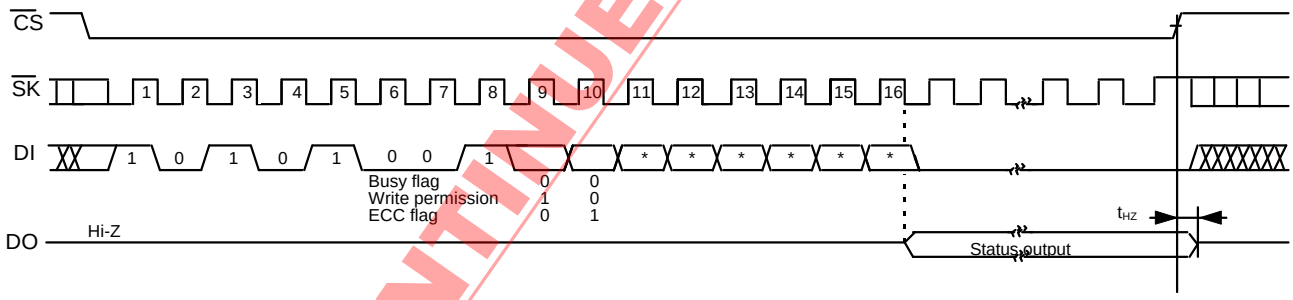


Figure 10

Table 10 IC inside status

Flag name	Flag set	"L"output	"H"output	Remarks
Write status flag	00	During writing	Completed writing	—
Write permission flag	10	Program enable mode	Program disable mode	—
ECC flag	01	Showing not modified	—	For maintaining compatibility with M6M80021/41, "L" is always output. Redundant memory is not included.

5. Reset operation

After RESET goes to "H" during the write operation, the write operation is terminated. At that time, only READ, EWEN, EWDS, and the status output instruction can be performed.

Although RESET can be connected with $\overline{CS}$, RESET must be fixed at "L" during writing. If RESET goes to "H" during writing, for 0.1 ms from the rise of RESET, no instruction except for status output can be accepted.

■ Three-wire Interface • DI-DO direct connecting

Although usually, a four-wire interface with $\overline{CS}$, $\overline{SK}$, DI, and DO is used for configuring a serial interface, a three-wire interface can be also used for configuring a serial interface by connecting DI and DO. However, since the three-wire system has a possibility that the data output from the serial memory IC interferes with the data output from the CPU, install a resistor between DI and DO (See Figure 11) to give preference to data output from CPU into DI.

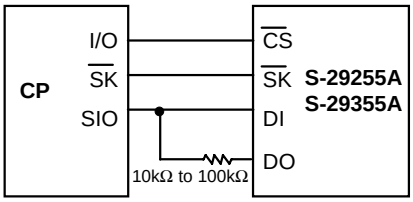
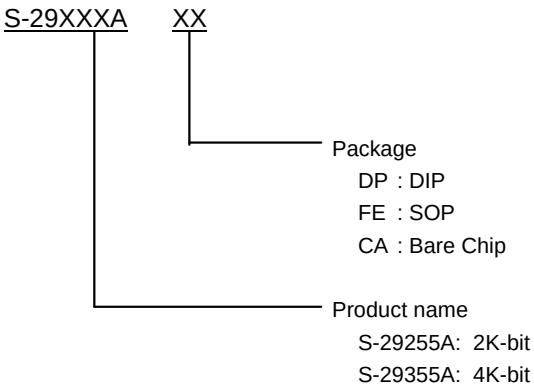


Figure 11

•Please refer Application Note “S-29 & S-93C series EEPROMs Tips, Tricks & Traps” for equivalent circuit of each pin.

■ Ordering Information

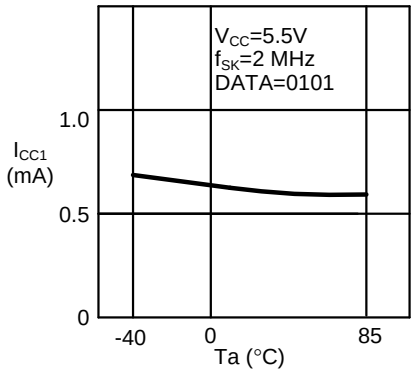


Note: Each bit is set to 1 before delivery (except bare chip) .

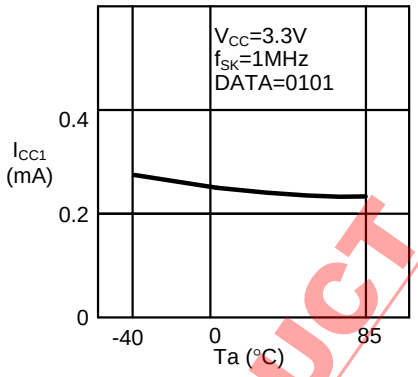
■ Characteristics

1. DC characteristics

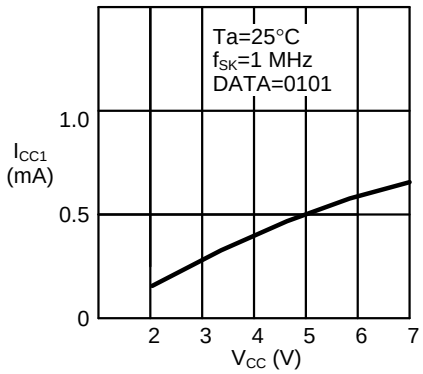
1.1 Current consumption (READ) I_{CC1} - Ambient temperature Ta



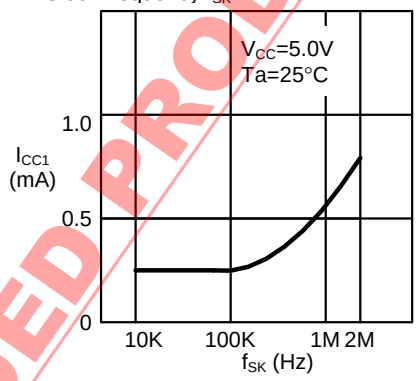
1.2 Current consumption (READ) I_{CC1} - Ambient temperature Ta



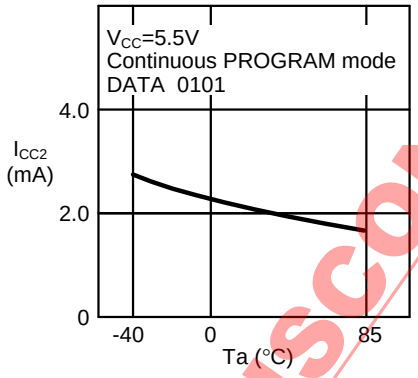
1.3 Current consumption (READ) I_{CC1} - Power supply voltage V_{CC}



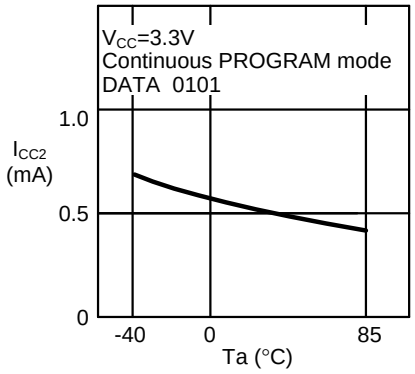
1.4 Current consumption (READ) I_{CC1} - Clock frequency f_{SK}



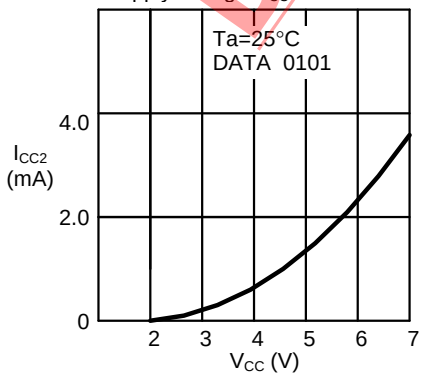
1.5 Current consumption (PROGRAM) I_{CC2} - Ambient temperature Ta



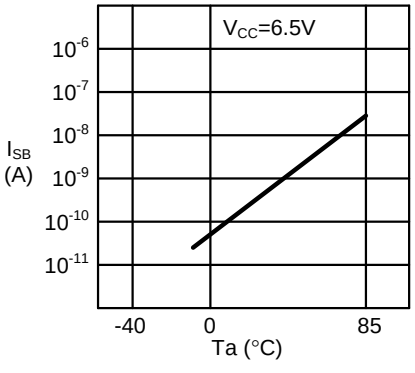
1.6 Current consumption (PROGRAM) I_{CC2} - Ambient temperature Ta



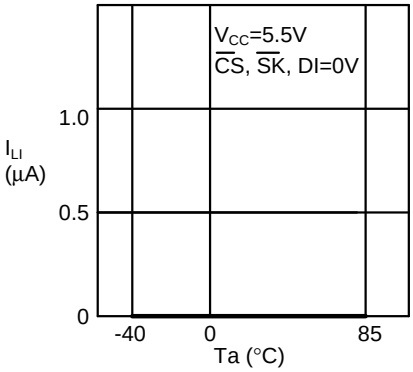
1.7 Current consumption (PROGRAM) I_{CC2} - Power supply voltage V_{CC}



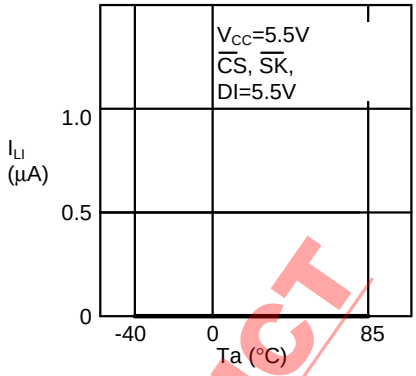
1.8 Standby current consumption I_{SB} - Ambient temperature Ta



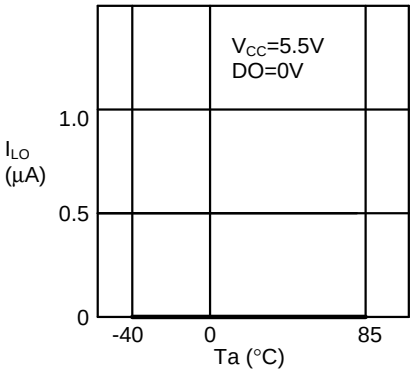
1.9 Input leakage current I_{LI} - Ambient temperature Ta



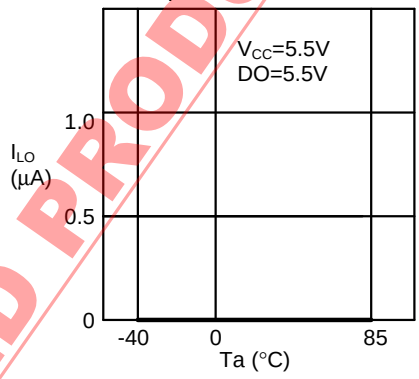
1.10 Input leakage current I_{LI} - Ambient temperature Ta



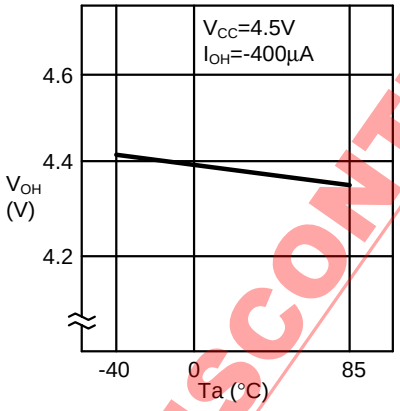
1.11 Output leakage current I_{LO} - Ambient temperature Ta



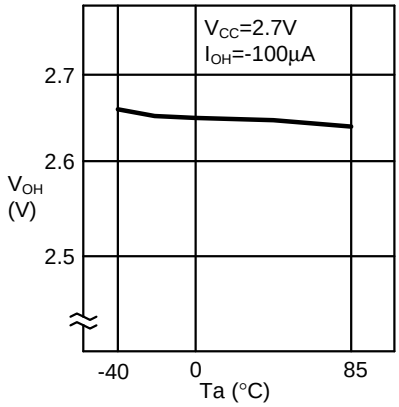
1.12 Output leakage current I_{LO} - Ambient temperature Ta



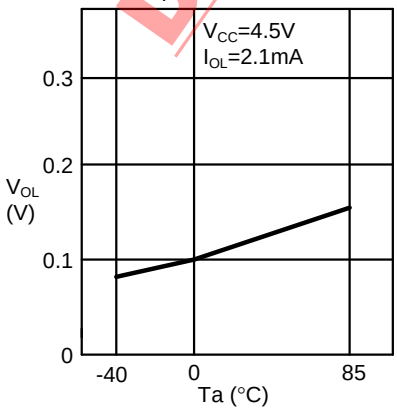
1.13 High level output voltage V_{OH} - Ambient temperature Ta



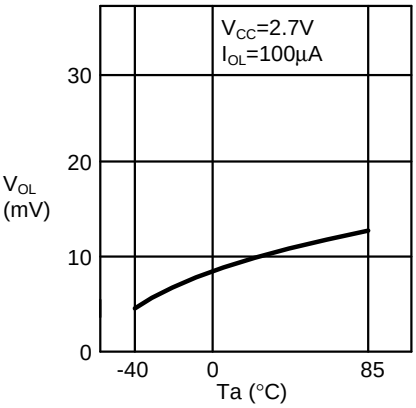
1.14 High level output voltage V_{OH} - Ambient temperature Ta



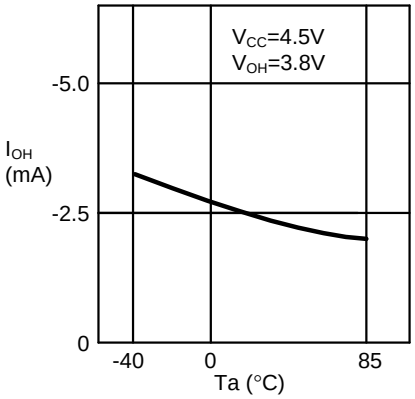
1.15 Low level output voltage V_{OL} - Ambient temperature Ta



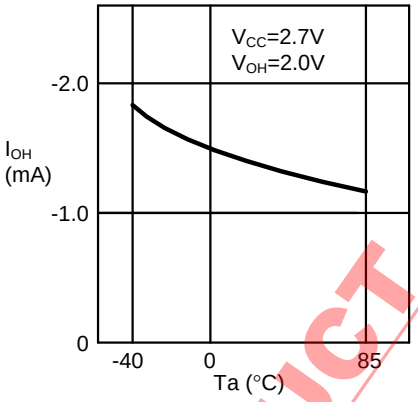
1.16 Low level output voltage V_{OL} - Ambient temperature Ta



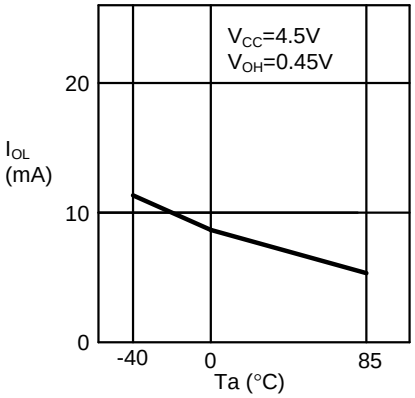
1.17 High level output current I_{OH} - Ambient temperature Ta



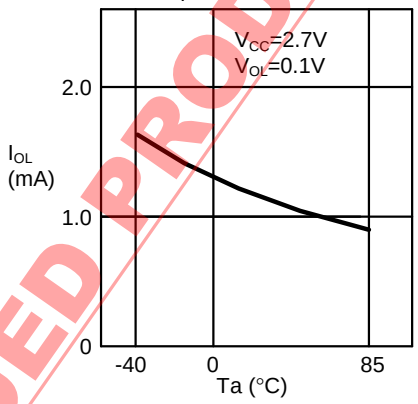
1.18 High level output current I_{OH} - Ambient temperature Ta



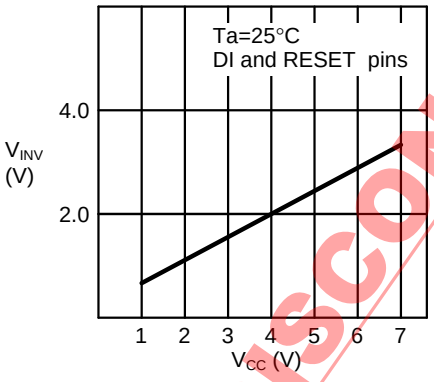
1.19 Low level output current I_{OL} - Ambient temperature Ta



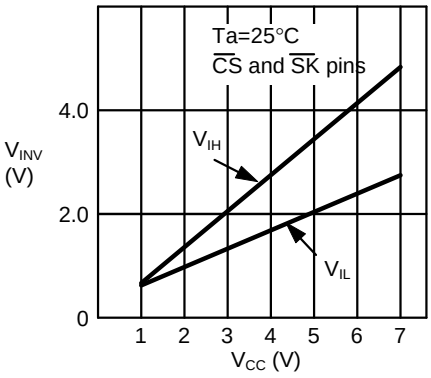
1.20 Low level output current I_{OL} - Ambient temperature Ta



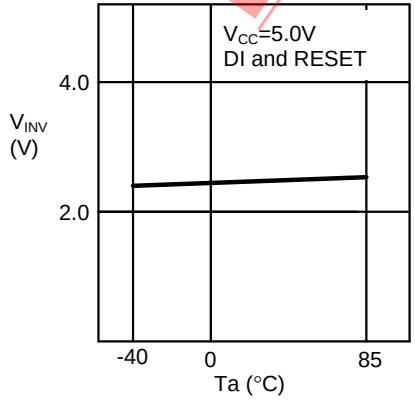
1.21 Input reversal voltage V_{INV} - Power supply voltage V_{CC}



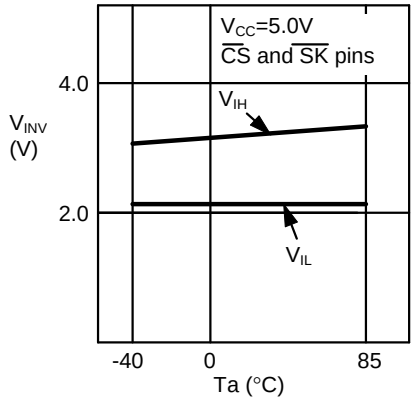
1.22 Input reversal voltage V_{INV} - Power supply voltage V_{CC}



1.23 Input reversal voltage V_{INV} - Ambient temperature Ta

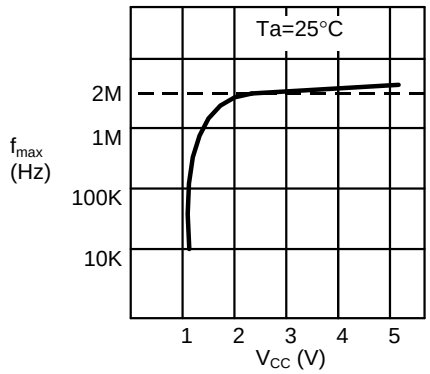


1.24 Input reversal voltage V_{INV} - Ambient temperature Ta

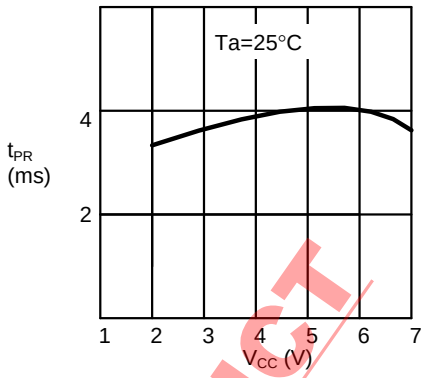


2. AC characteristics

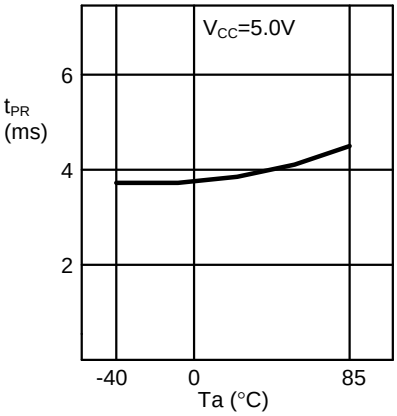
2.1 Maximum operating frequency f_{max} - Power supply voltage V_{CC}



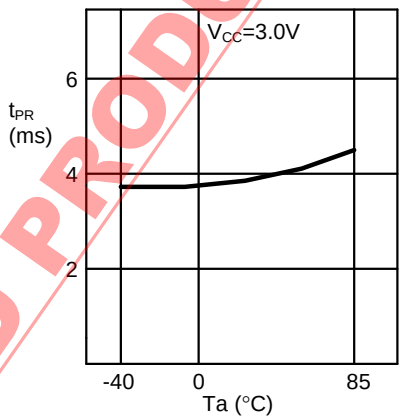
2.2 Program time t_{PR} - Power supply voltage V_{CC}



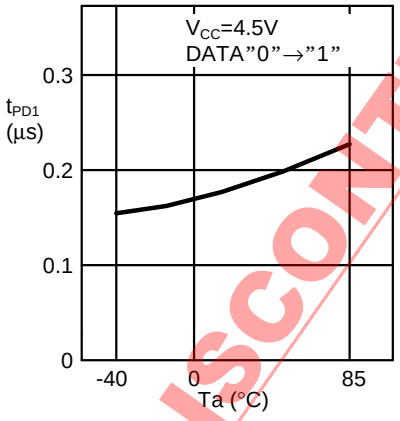
2.3 Program time t_{PR} - Ambient temperature Ta



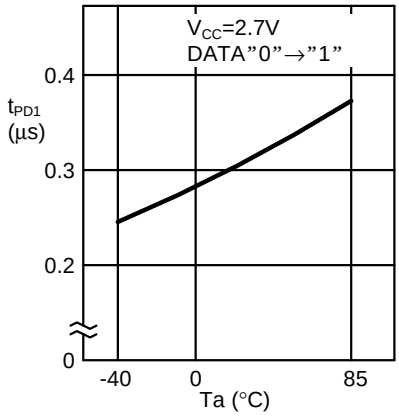
2.4 Program time t_{PR} - Ambient temperature Ta



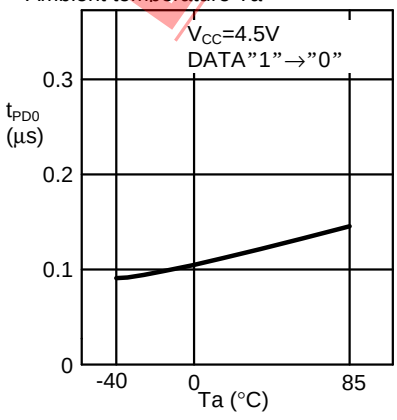
2.5 1 data output delay time t_{PD1} - Ambient temperature Ta



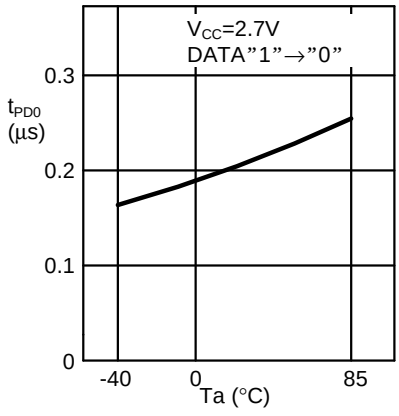
2.6 1 data output delay time t_{PD1} - Ambient temperature Ta



2.7 0 data output delay time t_{PD0} - Ambient temperature Ta



2.8 0 data output delay time t_{PD0} - Ambient temperature Ta

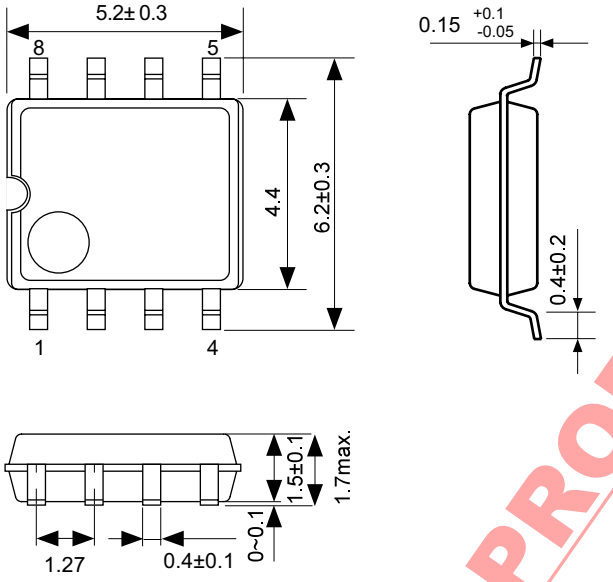


■ 8-Pin SOP

FE008-A Rev.1.0 020128

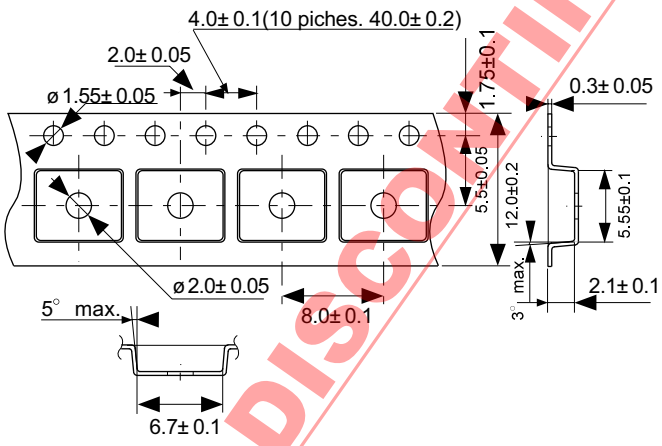
●Dimensions

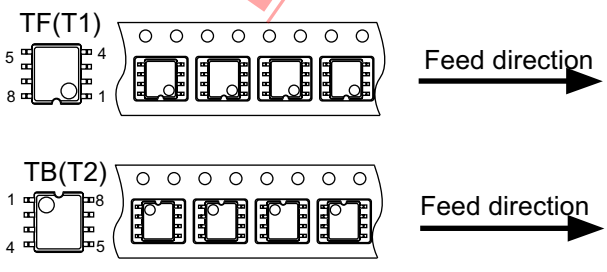
Unit:mm



No. : FE008-A-P-SD-1.0

●Taping Specifications

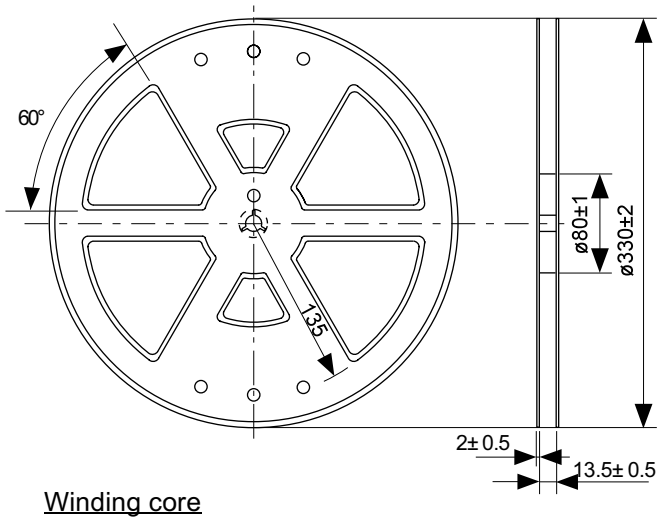




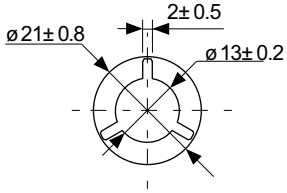
No. : FE008-A-C-SD-3.0

●Reel Specifications

1 reel holds 2000 ICs.



Winding core



No. : FE008-A-R-SD-1.0

■ 8-pin DIP

DP008-A 011022

●Dimensions

Unit:mm