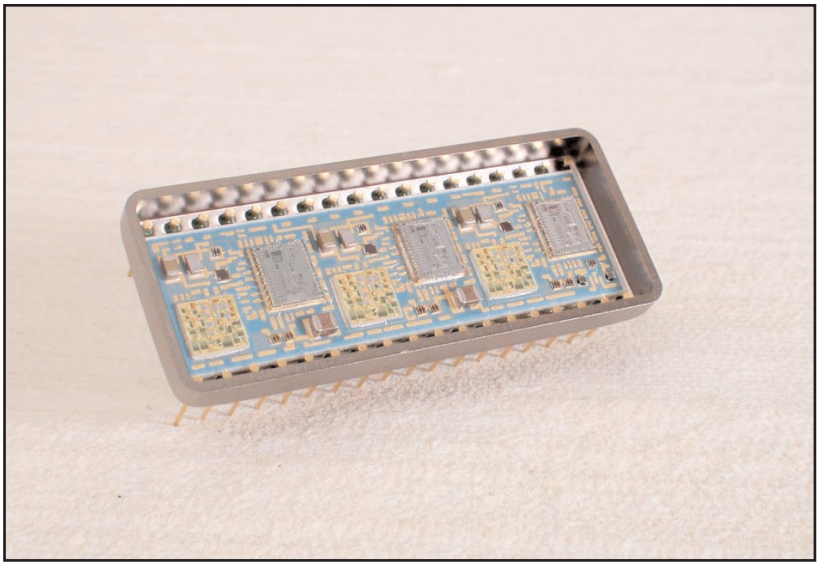
SDC-14610/15 Series

Three Channel 14- and 16-Bit Tracking S/R-D Converters



DESCRIPTION

The SDC-14610/15 Series are small low cost three channel Synchro- or Resolver-to-Digital (S/R-D) converters. The SDC-14610 Series are fixed at 14 bits, the SDC-14615 at 16 bits. The three channels are independent tracking types but share digital output pins and a common reference.

The SDC-14610/15 “S” option offers synthesized reference circuitry to correct for phase shifts between the reference and the signal voltage.

The Velocity Output (VEL) from the SDC-14610/15 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 1% of output voltage.

A $\overline{\text{BIT}}$ output is optional and is a logic line that indicates LOS (Loss Of Signal) or excessive converter error and LOR (Loss Of Reference - option “S” only). Due to pin limitations this option will exclude the velocity output. (See option “T”.)

SDC-14610/15 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and MIL-PRF-38534 processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14610/15 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

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FEATURES

- Synthesized Reference Option
- Fixed 14- or 16-Bit Resolution
- Small Size 36-Pin DDIP Package
- Three Independent Converters
- Low Cost per Channel
- Velocity Output Eliminates Tachometer
- Optional $\overline{\text{BIT}}$ Output (LOS and LOR)
- High Reliability Single Chip Monolithic
- -55°C to +125°C Operating Temperature Range
- MIL-PRF-38534 Processing Available

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

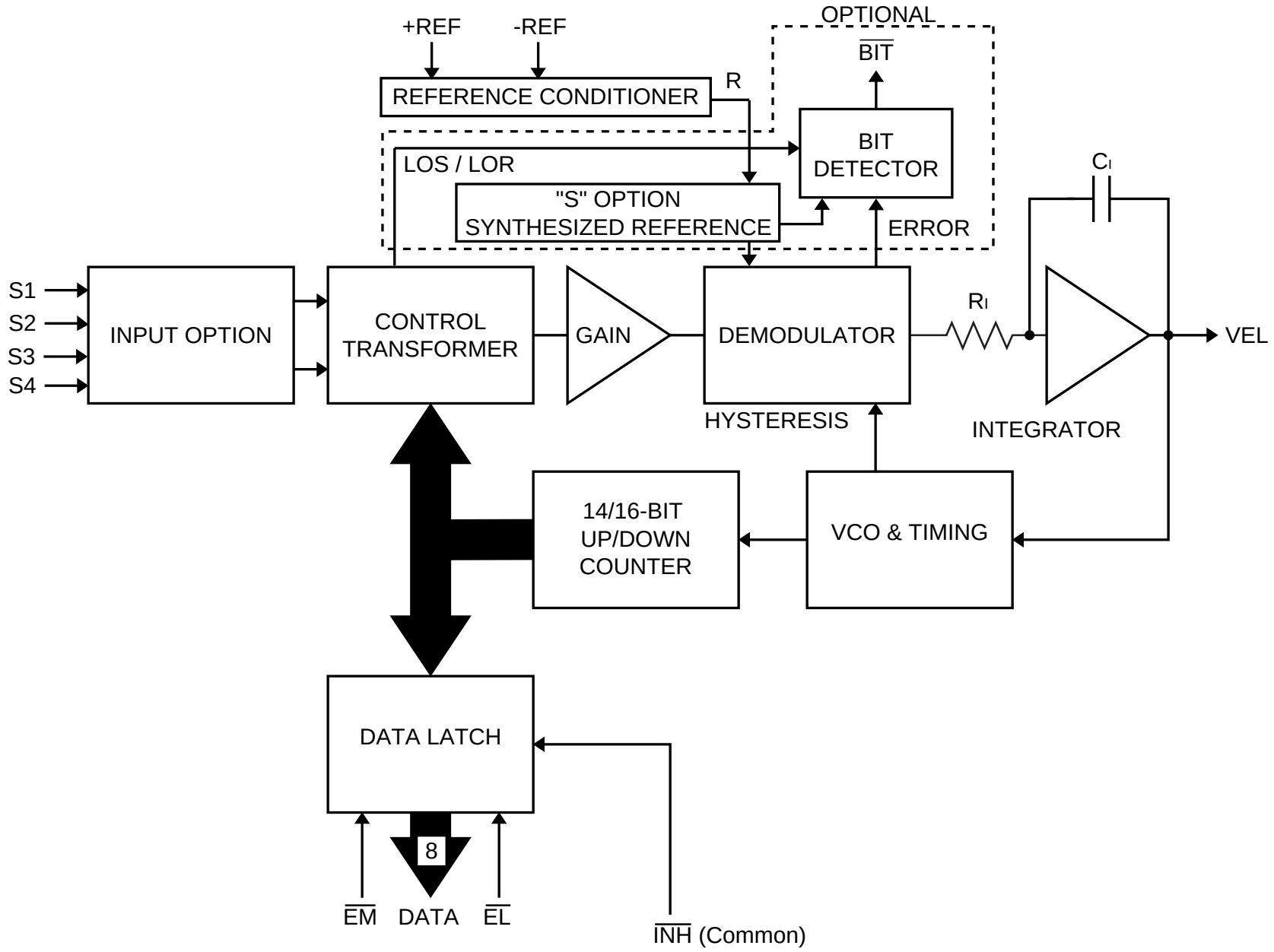


FIGURE 1. SDC-14610/15 BLOCK DIAGRAM (ONE CHANNEL)

TABLE 1. SDC-14610/15 SPECIFICATIONS

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. (Values are for each channel unless stated otherwise.)

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4 +1 LSB	2 or 4 +1 LSB 1 +1 LSB ("S" only*)
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		**(+REF, -REF), COMMON TO ALL CHANNELS DIFFERENTIAL**	
Type		**2 & 11.8V UNITS**	**90V UNIT**
Voltage Range	Vrms	2-35	10-130
Frequency	Hz	360-5000	see note **
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common-Mode Range	Vpeak	50,100 transient	200, 300 transient
Option "S"			
Voltage Range	Vrms	2-35	—
Frequency	Hz	1k-5k	—
Input Impedance			—
single ended	Ohm	40k	—
differential	Ohm	80k	—
Common-Mode Range	Vpeak	50,100 transient	—
±Sig/Ref Phase Shift	deg.	45 max	—
SIGNAL INPUT CHARACTERISTICS		**EACH CHANNEL**	
90V Synchro Input (L-L)		(Not Available on "S" option)	
Zin line-to-line	Ohm	123k	
Zin line-to-ground	Ohm	80k	
Common-Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)		(Not Available on "S" option)	
Zin line-to-line	Ohm	52k	
Zin line-to-ground	Ohm	34k	
Common-Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Zin line-to-line	Ohm	140k	
Zin line-to-ground	Ohm	70k	
Common-Mode Voltage	V	30 max	
2V Direct Input (L-L)		(Not Available on "S" option)	
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M//10 pF min	
2V Resolver Input (L-L)		("S" option only)	
Zin single ended	Ohm	11k	
Zin differential	Ohm	22k	
Common-Mode Voltage	V	4.9 max	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max Logic 1 = 2.0V min Loading (per channel) =10 µa max P.U. current source to +5V //5 pF max CMOS transient protected	
		EACH CHANNEL	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits; Data stable within 0.5 µs	
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 ns	
Enable Bits 9 to 14(16) ($\overline{EL}$)			

TABLE 1. SDC 14610/15 SPECIFICATIONS (CONT.)

PARAMETER	UNIT	VALUE				
DIGITAL INPUT/OUTPUT (Cont.)		Logic 1 = High Impedance Data High Z within 100 ns				
OUTPUTS		**Common To All Channels**				
Parallel Data [1-14(16)]	bits	8 parallel lines; 2 bytes natural binary angle, positive logic				
Built-In-Test ($\overline{BIT}$) (Optional)		Logic 0 = BIT condition ±100 LSBs of error with a filter of 500 µs or LOS / (LOR-"S" only)				
		EACH CHANNEL				
Drive Capability		50 pF +				
	TTL	Logic 0; 1 TTL load, 1.6 mA at 0.4V max				
		Logic 1; 10 TTL loads, -0.4 mA at 2.8V min				
		Logic 0; 100 mV max driving				
	CMOS	Logic 1; +5V supply minus 100 mV min driving				
DYNAMIC CHARACTERISTICS		**Device Type**				**"S" OPTION**
		60 HZ		**400 HZ**		
Each Channel						
Input Frequency	Hz	47-5 k		360-5 k		1 k-5 k
Bandwidth(Closed Loop)	Hz	15		103		150
Ka	$1/s^2$	830		53k		110k
A1	1/s	0.17		1.33		2.47
A2	1/s	5k		40k		44.4k
A	1/s	29		230		333
B	1/s	14.5		115		166
Resolution	bits	**14**	**16**	**14**	**16**	**16**
Tracking Rate						
typical	rps	1.25	0.31	10	2.5	2.5
minimum	rps	1	0.25	8	2	2
Acceleration (1 LSB lag)	deg/s^2	18	4.5	1160	290	610
Settling Time (179° step max)	msec	1100	2500	140	320	232
VELOCITY CHARACTERISTICS		**EACH CHANNEL**				
Polarity		Positive for increasing angle				
Voltage Range(Full Scale)	±V	4.5 typ, 4 min				
Voltage Scaling	rps/FS	10				
Scale Factor	±%	10 typ	20 max			
Scale Factor TC	ppm/°C	100 typ	200 max			
Reversal Error	±%	1 typ	2 max			
Linearity	±%	0.5 typ	1 max			
Zero Offset	mV	5 typ	10 max			
Zero Offset TC	µV/°C	15 typ	30 max			
Load	kOhm		20 max			
Noise	(Vp/V)%	1 typ	2 max			
POWER SUPPLIES		**TOTAL DEVICE**				
Nominal Voltage	V	+5	-5			
Voltage Range	±%	5	10			
Max Volt. w/o Damage	V	+7	-7			
Current (Ea.)	mA	36 typ, 51 max				
TEMPERATURE RANGE						
Operating						
-30X	°C	0 to +70				
-10X	°C	-55 to +125				
Storage	°C	-65 to +150				
Junction-to-case	°C/W	55				
JC Thermal Rise	°C	+9***				
Junction Temperature max.	°C	140				

Notes: * Applies to "S" Option only
** 47 - 5k for 90V, 60 Hz; 360 - 5k for 90V, 400 Hz
***Applied to operating temperature.

TABLE 1. SDC 14610/15 SPECIFICATIONS (CONT.)		
PARAMETER	**UNIT**	**VALUE**
PHYSICAL CHARACTERISTICS		
Size	in (mm)	1.70 x 0.78 x 0.21 (43.2 x 19.8 x 5.3)
Weight	oz(g)	0.66(18.7)

THEORY OF OPERATION

The SDC-14610/15 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver-to-digital converter.

Figure 1 is the Functional Block Diagram of the SDC-14610/15 Series. The converter operates with ±5VDC power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14-bit digital angle f. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of SINqCOSf - COSqSINf = SIN(q - f) using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters, ratioed capacitors are used in the CT instead of more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The DC error is integrated yielding a velocity voltage which, in turn, drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its functional block diagram and its Bode plots (open and closed loop); these are shown in figureS 1 and 2 respectively.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient
and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod)

- Integrator Gain = $\frac{1}{R_i C_i}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25\ R_v C_v}$ LSBs per second per volt

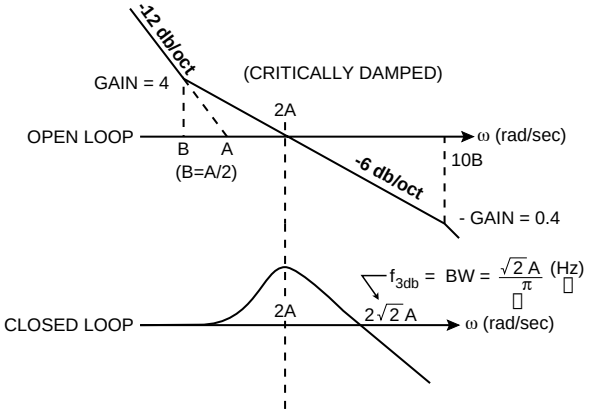


FIGURE 2. BODE PLOTS

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when connecting the SDC-14610/15 Series converters:

1) Power supplies are ±5VDC. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.

2) Direct inputs are referenced to AGND.

3) Connect pin 5 (GND) to pin 6 (AGND) close to the hybrid.

INHIBIT AND ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in six bytes. The Enable MSB ($\overline{EM}$-A, $\overline{EM}$-B, or $\overline{EM}$-C) is used for the most significant 8 bits and Enable LSB ($\overline{EL}$-A, $\overline{EL}$-B, or $\overline{EL}$-C) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

$\overline{BIT}$, BUILT-IN-TEST ("T" OPTION)

This output is a logic line that will flag an internal fault condition, or LOS (Loss-Of-Signal). The internal fault detector monitors the internal error and, when it exceeds ±100 LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500 µs filter) $\overline{BIT}$ will set for an overvelocity condition because the converter loop can't maintain input/output sync. $\overline{BIT}$ will also be set if a total LOS (loss of all signals) occurs or an LOR (loss of reference - "S" option only) occurs.

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB" (or 180° bit) is "toggled" on and off, a converter without the "false 180° reading" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver cannot change its output 180° instantaneously. The condition is most often noticed during wraparound verification tests, simulations, or troubleshooting.

SYNTHESIZED REFERENCE

The synthesized reference section ("S" option) eliminates errors due to phase shift between the reference and signal inputs. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. As shown in FIGURE 1, the converter synthesizes its own internal reference signal based on the SIN and COS signal inputs. Therefore, the phase of the synthesized (internal) reference is determined by the signal input, resulting in reduced quadrature errors. The synthesized reference circuit also eliminates the 180 degree false error null hang up.

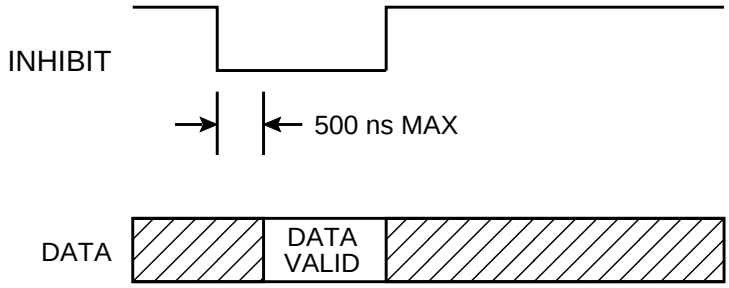


FIGURE 3. INHIBIT TIMING

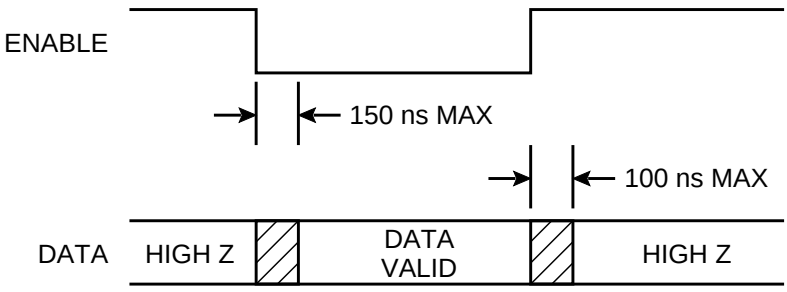
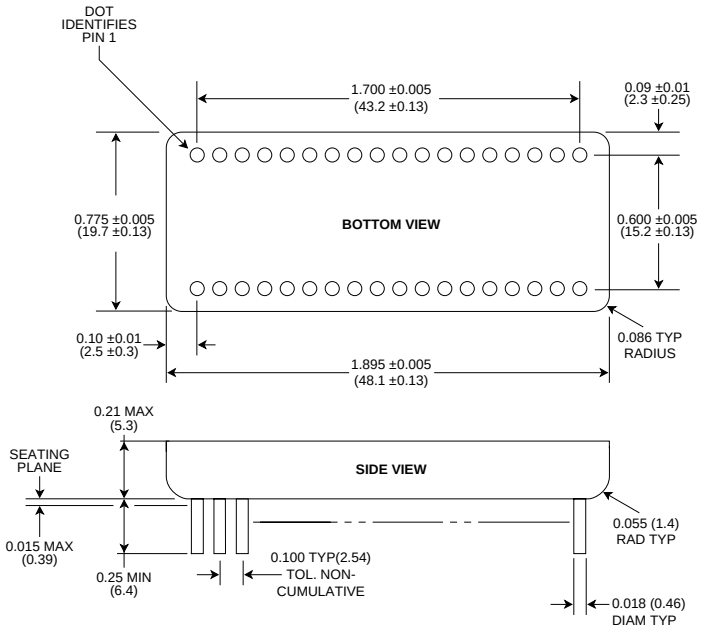


FIGURE 4. ENABLE TIMING

TABLE 2. PINOUTS (36 PIN) (SEE NOTE 1)					
1	S1A(S)	S1A(R)	N.C.	36	VEL A (Velocity Output) (see Note 2)
2	S2A(S)	S2A(R)	+COSA(D)	36	$\overline{EM}$-A (Enable MSBs)
3	S3A(S)	S3A(R)	+SINA(D)	34	$\overline{EL}$-A (Enable LSBs)
4	N.C.	S4A(R)	N.C.	33	$\overline{INH}$ (Inhibit)
5	GND (Ground)(see Note 4)			32	VEL B (Velocity Output) (see Note 2)
6	AGND (Analog Ground) (see Note 4)			31	$\overline{EM}$-B (Enable MSBs)
7	S1B(S)	S1B(R)	N.C.	30	$\overline{EL}$-B (Enable LSBs)
8	S2B(S)	S2B(R)	+COSB(D)	29	Bit 8/Bit 16 (see Note 3)
9	S3B(S)	S3B(R)	+SINB(D)	28	Bit 7/Bit 15 (see Note 3)
10	N.C.	S4B(R)	N.C.	27	Bit 6/Bit 14
11	-5V (Power Supply)			26	Bit 5/Bit 13
12	+5V (Power Supply)			25	Bit 4/Bit 12
13	S1C(S)	S1C(R)	N.C.	24	Bit 3/Bit 11
14	S2C(S)	S2C(R)	+COSC(D)	23	Bit 2/Bit 10
15	S3C(S)	S3C(R)	+SINC(D)	22	Bit 1/Bit 9
16	N.C.	S4C(R)	N.C.	21	VEL C (Velocity Output) (see Note 2)
17	-REF (-Reference Input)			20	$\overline{EL}$-C (Enable LSBs)
18	+REF (+Reference Input)			19	$\overline{EM}$-C (Enable MSBs)

Notes: 1. (S) = Synchro; (R) = Resolver; (D) = 2 V Resolver Direct
2. Replaced with BIT - "T" option
3. SDC-14615 Series only
4. Connect pin 5 (GND) to pin 6 (AGND) close to the hybrid



Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

FIGURE 5. SDC-14610/15 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-1461XX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = 100% Pull Test
- Q = 100% Pull Test and Pre-Cap Source Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source Inspection
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 2 = 4 minutes + 1 LSB
- 4 = 2 minutes + 1 LSB (Not available with 14-bit units.)
- 5 = 1 minute + 1 LSB (Available with “S” option only.)

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table on next page)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See TABLE 3)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Option:
- Blank = Standard Velocity Output (VEL)
- T = Built-In-Test Output (LOS and LOR), instead of VEL
- S = Synthesized Reference with Built-In-Test Output instead of VEL (Only available with input option 6 or 8)

Input Option:
- 0 = 11.8V, Synchro, 14 bit, 400 Hz
- 1 = 11.8V, Resolver, 14 bit, 400 Hz
- 2 = 90V, Synchro, 14 bit, 400 Hz
- 3 = 2V, Direct, 14 bit, 400 Hz
- 4 = 90V, Synchro, 14 bit, 60 Hz
- 5 = 11.8V, Synchro, 16 bit, 400 Hz
- 6 = 11.8V, Resolver, 16 bit, 400 Hz (1kHz with “S” option)
- 7 = 90V, Synchro, 16 bit, 400 Hz
- 8 = 2V, Direct 16 bit, 400 Hz (2V, Differential 16 Bit, 1kHz for option “S” only)
- 9 = 90V, Synchro, 16 bit, 60 Hz

*Standard DDC Processing with burn-in and full temperature test—see table on next page.

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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