HS-6564RH

NOT RECOMMENDED FOR NEW DESIGNS
See HS-65647RH

September 1997

Radiation Hardened
8K x 8, 16K x 4 CMOS RAM Module

Features

- **Radiation Hardened EPI CMOS**
  - **Total Dose 1 x 10^5 RAD (Si)**
  - **Transient Upset > 1 x 10^8 RAD (Si)/s**
  - **Latch-Up Free to > 1 x 10^{12} RAD (Si)/s**
- **Low Power Standby 4.4mW Maximum**
- **Low Power Operation 308mW/MHz Maximum**
- **Data Retention 3.0V Minimum**
- **TTL Compatible In/Out**
- **Three State Outputs**
- **Fast Access Time 250ns Maximum**
- **Military Temperature Range -55°C to +125°C**
- **On Chip Address Registers**
- **Organizable 8K x 8 or 16K x 4**
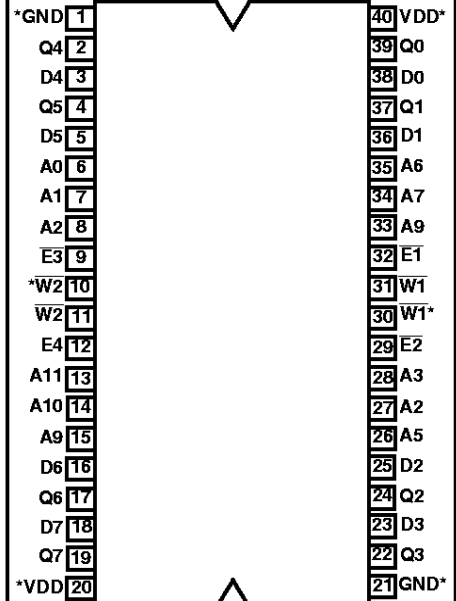- **40 Pin DIP Pinout 2.000" x 0.900"**

Description

The HS-6564RH is a radiation hardened 64K bit, synchronous CMOS RAM module. It consists of 16 HS-6504RH 4K x 1 radiation hardened CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The individual RAMs are fabricated using the Harris radiation hardened guard ring, self-aligned silicon gate technology. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are seperate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile readswrite memory by using very small batteries mounted directly on the memory circuit board.
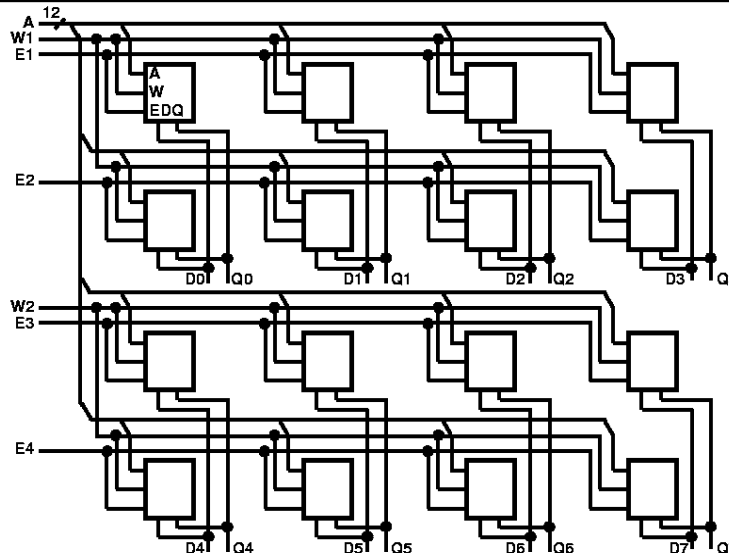
Pinout

HS5-6564RH 40 PIN CERAMIC MODULE
INTERNAL PACKAGE CODE "HSQ"
TOP VIEW

Pin	Signal		Pin	Signal
1	*GND		40	VDD*
2	Q4		39	Q0
3	D4		38	D0
4	Q5		37	Q1
5	D5		36	D1
6	A0		35	A6
7	A1		34	A7
8	A2		33	A9
9	E3		32	E1
10	*W2		31	W1
11	W2		30	W1*
12	E4		29	E2
13	A11		28	A3
14	A10		27	A2
15	A9		26	A5
16	D6		25	D2
17	Q6		24	Q2
18	D7		23	D3
19	Q7		22	Q3
20	*VDD		21	GND*

* Pins 20 and 40 (VDD) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect both VDD pins and both Ground pins to the board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram

File Number **3032.1**

Specifications HS-6564RH

Absolute Maximum Ratings

Supply Voltage . . . . -3.0V to +7.0V
Input or Output Voltage Applied . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature . . . . +175°C
Lead Temperature (Soldering 10s) . . . . +300°C
Typical Derating Factor . . . . 48mA/MHz Increase in IDDOP
ESD Classification . . . . Class 1

Reliability Information

		θ$_{ja}$	θ$_{jc}$
Thermal Resistance			
40 Pin Ceramic Module Package		TBD	TBD

Maximum Package Power Dissipation at +125°C
 40 Pin Ceramic Module Package . . . . .TBD
Gate Count . . . . 53,336 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range . . . . +4.5V to +5.5V   Operating Temperature Range . . . .-55°C to +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	1600	µA
Operating Supply Current (8K x 8) (Note 1)	IDDOP1	f = 1MHz, IO = 0 VI = VDD or GND	-	56	mA
Operating Supply Current (16K x 4) (Note 1)	IDDOP2	f = 1MHz, IO = 0 VI = VDD or GND	-	28	mA
Data Retention Supply Current	IDDDR	IO = 0, VDD = 3.0 VI = VDD or GND	-	1200	µA
Data Retention Supply Current	VDDDR		3.0	-	V
Address Input Leakage	IIA	GND ≤ VI ≤ VDD	-20	+20	µA
Data Input Leakage (8K x 8)	IID1	GND ≤ VI ≤ VDD	-3	+3	µA
Data Input Leakage (16K x 4)	IID2	GND ≤ VI ≤ VDD	-5	+5	µA
Enable Input Leakage (8K x 8)	IIE1	GND ≤ VI ≤ VDD	-10	+10	µA
Enable Input Leakage (16K x 4)	IIE2	GND ≤ VI ≤ VDD	-5	+5	µA
Write Enable Input Leakage (Each)	IIW	GND ≤ VI ≤ VDD	-10	+10	µA
Output Leakage (8K x 8)	IOZ1	GND ≤ VO ≤ VDD	-20	+20	µA
Output Leakage (16K x 4)	IOZ2	GND ≤ VO ≤ VDD	-40	+40	µA
Input Low Voltage	VIL		-	0.8	V
Input High Level (Except $\overline{E}$ and $\overline{W}$)	VIH1		VDD -1.5	-	V
Input High Level ($\overline{E}$ and $\overline{W}$)	VIH2		VDD -1.0	-	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTES:
1. Operating supply current is proportional to operating frequency. IDDOP is specified at an operating frequency of 1MHz indicating repetitive accessing at a 1µs rate. Operating at slower rates will decrease IDDOP proportionally.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	350	ns
Address Access Time (TAVQV = TELQV + TAVEL)	TAVQV	Note 1	-	400	ns
Chip Enable Low	TELEH	Note 1	350	-	ns
Chip Enable High	TEHEL	Note 1	130	-	ns
Address Setup Time	TAVEL	Note 1	50	-	ns
Address Hold Time	TELAX	Note 1	50	-	ns
Write Enable Low	TWLWH	Note 1	150	-	ns
Write Enable Setup Time	TWLEH	Note 1	250	-	ns
Early Write Setup Time	TWLEL	Note 1	10	-	ns
Early Write Hold Time	TELWX	Note 1	100	-	ns
Data Setup Time	TDVWL	Note 1	10	-	ns
Early Write Data Setup Time	TDVEL	Note 1	90	-	ns
Data Hold Time	TWLDX	Note 1	100	-	ns
Early Write Data Hold Time	TELDX	Note 1	100	-	ns
Early Write Pulse Hold Time	TELWH	Note 1	250	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20ns: Outputs : CLOAD = 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Address Input Capacitance	CIA	f = 1MHz, VI = VDD or GND	-	200	pF
Data Input Capacitance (8K x 8)	CID1	f = 1MHz, VI = VDD or GND	-	50	pF
Data Input Capacitance (16K x 4)	CID2	f = 1MHz, VI = VDD or GND	-	100	pF
Enable Input Capacitance (8K x 8)	CIE1	f = 1MHz, VI = VDD or GND	-	160	pF
Enable Input Capacitance (16K x 4)	CIE2	f = 1MHz, VI = VDD or GND	-	80	pF
Write Enable Input Capacitance (Each)	CIW	f = 1MHz, VI = VDD or GND	-	100	pF
Output Capacitance (8K x 8)	CO1	f = 1MHz, VO = VDD or GND	-	50	pF
Output Capacitance (16K x 4)	CO2	f = 1MHz, VO = VDD or GND	-	100	pF
Output Enable Time	TELQX		-	75	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Output Disable Time	TEHQZ		-	75	ns
Data Valid to Write (Read-Modify-Write)	TQVWL		100	-	ns
Read or Write Cycle Time	TELEL		480	-	ns

NOTE:

1. Inputs: TRISE = TFALL ≤ 20ns. Outputs: CLOAD = 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

NOTE: Circuits are Burned-in as HS-6504RH discrete units, see HS-6504RH for appropriate burn-in delta information.

TABLE 6. APPLICABLE SUBGROUPS

NOTE: Quality Conformance Inspection (QCI) applies to the individual HS-6564RH devices, not to the assembled module. See HS-6504RH for further information.