# 16M x 1Bit CMOS Dynamic RAM with Static Column Mode

## DESCRIPTION

This is a family of 16,777,216 x 1 bit Static Column Mode CMOS DRAMs. Static Column Mode offers high speed random access of memory cells within the same row. Access time(-5, -6, -7 or -8) and package type (SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{RAS}$-only refresh and Hidden Refresh capabilities.
This 16Mx1 Static Column Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width and high reliability. It may be used as main memory unit for high level computer and high performance microprocessor systems.

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## FEATURES

- Part Identification
  - KM41C16002A(5V, 4K Ref.)

- Active Power Dissipation

Unit : mW

| Speed | Power dissipation |
|---|---|
| -5 | 495 |
| -6 | 440 |
| -7 | 385 |
| -8 | 330 |

- Refresh cycles

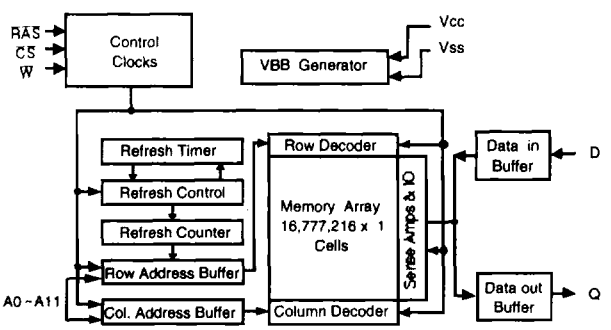
| | Refresh cycle | Refresh Period |
|---|---|---|
| KM41C16002A | 4K | 64ms |

- Performance range:

| Speed | tRAC | tCAC | tRC | tSC |
|---|---|---|---|---|
| -5 | 50ns | 13ns | 90ns | 30ns |
| -6 | 60ns | 15ns | 110ns | 35ns |
| -7 | 70ns | 20ns | 130ns | 40ns |
| -8 | 80ns | 20ns | 150ns | 45ns |

- Static Column Mode operation
- $\overline{CS}$-before-$\overline{RAS}$ refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or Output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

## FUNCTIONAL BLOCK DIAGRAM

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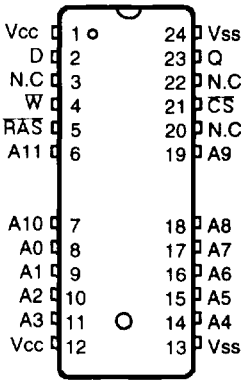
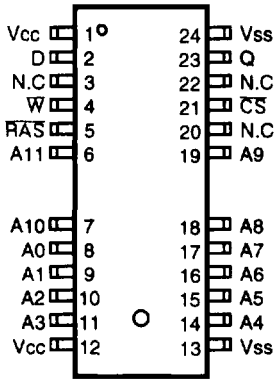
## PIN CONFIGURATION (Top Views)

• KM41C16002AJ



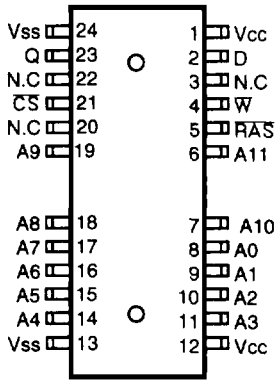

J : 400 mil 24(28) SOJ

• KM41C16002AT



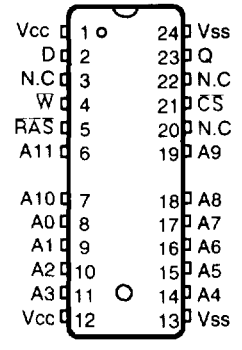

T : 400 mil 24(28) TSOP II

• KM41C16002ATR



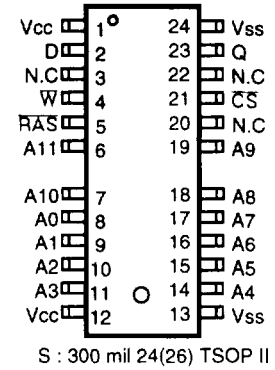

TR : 400 mil 24(28) TSOP II(Rev.)

• KM41C16002AK



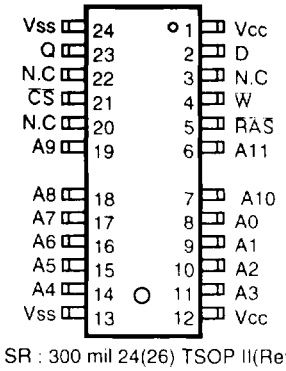

K : 300 mil 24(26) SOJ

• KM41C16002AS




S : 300 mil 24(26) TSOP II

• KM41C16002ASR




SR : 300 mil 24(26) TSOP II(Rev.)

| Pin Name | Pin Function |
|---|---|
| A0 - A11 | Address Inputs |
| D | Data in |
| Q | Data out |
| Vss | Ground |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CS}$ | Chip select input |
| $\overline{W}$ | Read/Write Input |
| Vcc | Power(+5.0V) |
| N.C | No Connection |



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## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$,$V_{OUT}$ | -1 to +7.0 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | -1 to +7.0 | V |
| Storage temperature | Tstg | -55 to +150 | °C |
| Power dissipation | $P_D$ | 1 | W |
| Short circuit output current | $I_{OS}$ | 50 | mA |

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}$, $T_A$= 0 to 70 °C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input high voltage | $V_{IH}$ | 2.4 | - | Vcc+1.0*1 | V |
| Input low voltage | $V_{IL}$ | -1.0*2 | - | 0.8 | V |

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse width is measured at Vss)

## DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input leakage current (Any input 0≤$V_{IN}$≤Vcc+0.5V all other pins not under test=0 volts.) | $I_{I(L)}$ | - 5 | 5 | μA |
| Output leakage current (Data out is disabled, 0V≤$V_{OUT}$≤Vcc) | $I_{O(L)}$ | - 5 | 5 | μA |
| Output high voltage level($I_{OH}$=-5mA) | $V_{OH}$ | 2.4 | - | V |
| Output low voltage level($I_{OL}$=4.2mA) | $V_{OL}$ | - | 0.4 | V |

## DC AND OPERATING CHARACTERISTICS (Continued)

| Symbol | Speed | Max | Units |
|---|---|---|---|
| | | KM41C16002A | |
| $I_{CC1}$ | -5 | 90 | mA |
| | -6 | 80 | mA |
| | -7 | 70 | mA |
| | -8 | 60 | mA |
| $I_{CC2}$ | Don't care | 2 | mA |
| $I_{CC3}$ | -5 | 90 | mA |
| | -6 | 80 | mA |
| | -7 | 70 | mA |
| | -8 | 60 | mA |
| $I_{CC4}$ | -5 | 80 | mA |
| | -6 | 70 | mA |
| | -7 | 60 | mA |
| | -8 | 50 | mA |
| $I_{CC5}$ | Don't care | 1 | mA |
| $I_{CC6}$ | -5 | 90 | mA |
| | -6 | 80 | mA |
| | -7 | 70 | mA |
| | -8 | 60 | mA |

$I_{CC1}$ *: Operating current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

$I_{CC2}$ : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=$V_{IH}$ )

$I_{CC3}$ *: $\overline{RAS}$-only refresh current ($\overline{CS}$=$V_{IH}$, $\overline{RAS}$ ,Address cycling @tRC=min.)

$I_{CC4}$ *: Static Column Mode current ($\overline{RAS}$=$V_{IL}$, $\overline{CS}$, Address cycling @tSC=min.)

$I_{CC5}$ : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=$V_{CC}$-0.2V)

$I_{CC6}$ *: $\overline{CS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

* NOTE : $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In $I_{CC1}$ , $I_{CC3}$ and $I_{CC6}$, address can be changed maximum once while $\overline{RAS}$=$V_{IL}$. In $I_{CC4}$, address can be changed maximum once within one Static Column mode cycle time tSC.

**CAPACITANCE**($T_A$=25°C,Vcc=5V , f=1MHz)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance [A0 - A9] | $C_{IN1}$ | - | 5 | pF |
| Input capacitance [$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$] | $C_{IN2}$ | - | 7 | pF |
| Output Capacitance [DQ0 - DQ3] | $C_{DQ}$ | - | 7 | pF |

**AC CHARACTERISTICS** (0°C≤$T_A$≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, Vih/Vil = 2.4/0.8V, Voh/Vol = 2.4/0.4V

| Parameter | Symbol | -5 | | -6 | | -7 | | -8 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 90 | | 110 | | 130 | | 150 | | ns | |
| Read-modify-write cycle time | tRWC | 110 | | 130 | | 155 | | 175 | | ns | |
| Access time from $\overline{RAS}$ | tRAC | | 50 | | 60 | | 70 | | 80 | ns | 3,4,10 |
| Access time from $\overline{CS}$ | tCAC | | 13 | | 15 | | 20 | | 20 | ns | 3,4,5 |
| Access time from column address | tAA | | 25 | | 30 | | 35 | | 40 | ns | 3,10 |
| $\overline{CS}$ to output in Low-Z | tCLZ | 0 | | 0 | | 0 | | 0 | | ns | 3 |
| Output buffer turn-off delay from $\overline{CS}$ | tOFF | 0 | 13 | 0 | 15 | 0 | 20 | 0 | 20 | ns | 6 |
| Transition time (rise and fall) | tT | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | 2 |
| $\overline{RAS}$ precharge time | tRP | 30 | | 40 | | 50 | | 60 | | ns | |
| $\overline{RAS}$ pulse width | tRAS | 50 | 10K | 60 | 10K | 70 | 10K | 80 | 10K | ns | |
| $\overline{RAS}$ hold time | tRSH | 13 | | 15 | | 20 | | 20 | | ns | |
| $\overline{CS}$ hold time | tCSH | 50 | | 60 | | 70 | | 80 | | ns | |
| $\overline{CS}$ pulse width | tCS | 13 | 10K | 15 | 10K | 20 | 10K | 20 | 10K | ns | |
| $\overline{RAS}$ to $\overline{CS}$ delay time | tRCD | 20 | 37 | 20 | 45 | 20 | 50 | 20 | 60 | ns | 4 |
| $\overline{RAS}$ to column address delay time | tRAD | 15 | 25 | 15 | 30 | 15 | 35 | 15 | 40 | ns | 10 |
| $\overline{CS}$ to $\overline{RAS}$ precharge time | tCRP | 5 | | 5 | | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 10 | | 10 | | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 10 | | 10 | | 15 | | 15 | | ns | |
| Column address hold time | tAR | 40 | | 50 | | 55 | | 60 | | ns | 14 |
| Column address to $\overline{RAS}$ lead time | tRAL | 25 | | 30 | | 35 | | 40 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | 0 | | 0 | | ns | |
| Read command hold time referenced to $\overline{CS}$ | tRCH | 0 | | 0 | | 0 | | 0 | | ns | 8 |
| Read command hold time referenced to $\overline{RAS}$ | tRRH | 0 | | 0 | | 0 | | 0 | | ns | 8 |
| Write command hold time | tWCH | 10 | | 10 | | 15 | | 15 | | ns | |
| Write command hold time referenced to $\overline{RAS}$ | tWCR | 40 | | 45 | | 55 | | 60 | | ns | 14 |
| Write command pulse width | tWP | 10 | | 10 | | 15 | | 15 | | ns | |
| Write command to $\overline{RAS}$ lead time | tRWL | 15 | | 15 | | 20 | | 20 | | ns | |
| Write command to $\overline{CS}$ lead time | tCWL | 13 | | 15 | | 20 | | 20 | | ns | |
| Data set-up time | tDS | 0 | | 0 | | 0 | | 0 | | ns | 9 |

## AC CHARACTERISTICS (Continued)

| Parameter | Symbol | -5 | | -6 | | -7 | | -8 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Data hold time | tDH | 10 | | 10 | | 15 | | 15 | | ns | 9 |
| Data hold time referenced to $\overline{RAS}$ | tDHR | 40 | | 45 | | 55 | | 60 | | ns | 14 |
| Refresh period | tREF | | 64 | | 64 | | 64 | | 64 | ms | |
| Write command set-up time | tWCS | 0 | | 0 | | 0 | | 0 | | ns | 7 |
| $\overline{CS}$ to $\overline{W}$ delay time | tCWD | 13 | | 15 | | 20 | | 20 | | ns | 7 |
| $\overline{RAS}$ to $\overline{W}$ delay time | tRWD | 50 | | 60 | | 70 | | 80 | | ns | 7 |
| Column address to $\overline{W}$ delay time | tAWD | 25 | | 30 | | 35 | | 40 | | ns | 7 |
| $\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh) | tCSR | 5 | | 5 | | 5 | | 5 | | ns | |
| $\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh) | tCHR | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ to $\overline{CS}$ precharge time | tRPC | 5 | | 5 | | 5 | | 5 | | ns | |
| $\overline{CS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle) | tCPT | 20 | | 20 | | 30 | | 30 | | ns | |
| Static Column mode cycle time | tSC | 30 | | 35 | | 40 | | 45 | | ns | |
| Static Column mode read-modify-write cycle time | tSRWC | 53 | | 60 | | 70 | | 80 | | ns | |
| Access time from last write | tALW | | 50 | | 55 | | 65 | | 75 | ns | 3,11 |
| Output data hold time from column address | tAOH | 5 | | 5 | | 5 | | 5 | | ns | |
| Output data enable time from $\overline{W}$ | tOW | | 35 | | 40 | | 45 | | 55 | ns | |
| $\overline{CS}$ precharge time (Static Column cycle) | tCP | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ pulse width (Static Column cycle) | tRASC | 50 | 200K | 60 | 200K | 70 | 200K | 80 | 100K | ns | |
| $\overline{CS}$ pulth width (Static Column cycle) | tCSC | 13 | 200K | 15 | 200K | 20 | 200K | 20 | 200K | ns | |
| Column address hold time referenced to $\overline{RAS}$ rising | tAH | 5 | | 5 | | 5 | | 5 | | ns | |
| Last write to column address delay time | tLWAD | 20 | 25 | 20 | 25 | 25 | 30 | 25 | 35 | ns | |
| Last write to column address hold time | tAHLW | 50 | | 55 | | 65 | | 75 | | ns | |
| Write command inactive time | tWI | 10 | | 10 | | 10 | | 10 | | ns | |
| Write address hold time referenced to $\overline{RAS}$ | tAWR | 40 | | 45 | | 55 | | 60 | | ns | |
| Write command set-up time(Test mode in) | tWTS | 10 | | 10 | | 10 | | 10 | | ns | |
| Write command hold time(Test mode in) | tWTH | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh) | tWRP | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh) | tWRH | 10 | | 10 | | 10 | | 10 | | ns | |

## TEST MODE CYCLE

(Note. 11)

| Parameter | Symbol | -5 | | -6 | | -7 | | -8 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 95 | | 115 | | 135 | | 155 | | ns | |
| Read-modify-write cycle time | tRWC | 140 | | 160 | | 190 | | 210 | | ns | |
| Access time from $\overline{RAS}$ | tRAC | | 55 | | 65 | | 75 | | 85 | ns | 3,4,10 |
| Access time from $\overline{CS}$ | tCAC | | 18 | | 20 | | 25 | | 25 | ns | 3,4,5 |
| Access time from column address | tAA | | 30 | | 35 | | 40 | | 45 | ns | 3,10 |
| $\overline{RAS}$ pulse width | tRAS | 55 | 10K | 65 | 10K | 75 | 10K | 85 | 10K | ns | |
| $\overline{CS}$ pulse width | tCS | 18 | 10K | 20 | 10K | 25 | 10K | 25 | 10K | ns | |
| $\overline{RAS}$ hold time | tRSH | 20 | | 20 | | 25 | | 25 | | ns | |
| $\overline{CS}$ hold time | tCSH | 55 | | 65 | | 75 | | 85 | | ns | |
| Column address to $\overline{RAS}$ lead time | tRAL | 30 | | 35 | | 40 | | 45 | | ns | |
| $\overline{CS}$ to $\overline{W}$ delay time | tCWD | 18 | | 20 | | 25 | | 25 | | ns | 7 |
| $\overline{RAS}$ to $\overline{W}$ delay time | tRWD | 55 | | 65 | | 75 | | 85 | | ns | 7 |
| Column address to $\overline{W}$ delay time | tAWD | 30 | | 35 | | 40 | | 45 | | ns | 7 |
| Static Column mode cycle time | tSC | 35 | | 40 | | 45 | | 50 | | ns | |
| Static Column mode read-modify-write cycle time | tSRWC | 58 | | 65 | | 75 | | 85 | | ns | |
| $\overline{RAS}$ pulse width (Static Column cycle) | tRASC | 55 | 200K | 65 | 200K | 75 | 200K | 85 | 200K | ns | |
| Access time form last write | tALW | | 55 | | 60 | | 70 | | 80 | ns | 3,11 |

## NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min) and $V_{IL}$(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. tAR, tWCR, and tDHR are referenced to $t_{RAD(MAX)}$.