M5M4C900L

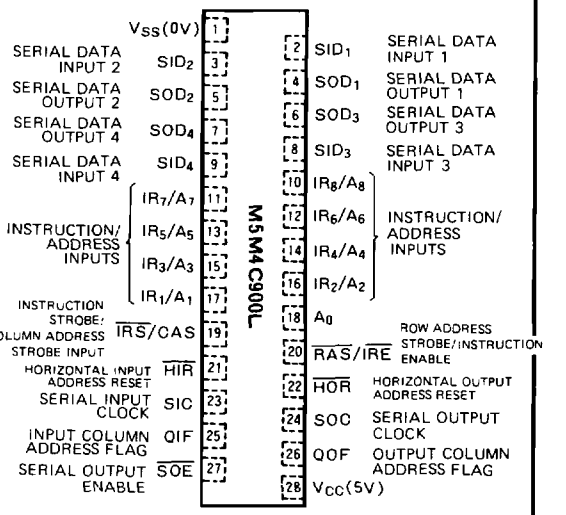
1069056-BIT(267264-WORD BY 4-BIT)FIELD MEMORY

DESCRIPTION

The M5M4C900L is a field memory consisting of a memory array of 288 rows x 928 columns x 4 bits, a serial input memory of 928 x 4 bits, and a serial output memory of 928 x 4 bits. Each serial port can be operated completely independently or asynchronously. The maximum serial input/output rates are 20MHz/33MHz, respectively. The use of triple-layer polysilicon process combined with silicide technology has enabled high integration, high speed and low power consumption.

Semi-random-accessability of row and column addresses, variety of data transfer functions including split transfer, and column address reset functions are the main features of the memory. The memory is housed in a 28-pin ZIP package suitable for high density mounting.

PIN CONFIGURATION (TOP VIEW)



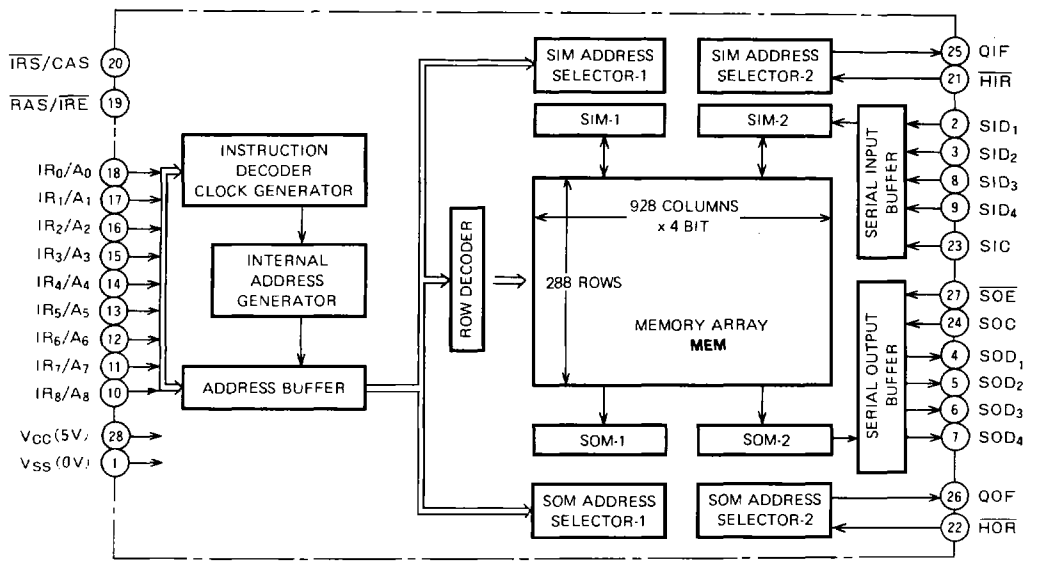
Outline 28P5L

FEATURES

Type name	Serial input cycle time (min.) (ns)	Serial output cycle time (min.) (ns)	Serial access time (max.) (ns)	Data transfer cycle time (min.) (ns)	Power consumption (typ.) (mW)
M5M4C900L	50	30	30	810	150

- Most suitable memory array configuration for high definition TV or VCR application
  . . . . . 288 rows x 928 columns x 4 bits
- Large capacity serial memory needs less data transfer, and less power consumption
  . . . . . 928 x 4 bits (common to input/output sides)
- High-speed serial input and output being clockable independently or asynchronously
  . . . . . minimum serial input cycle = 50ns
  . . . . . minimum serial output cycle = 30ns
- Three-multiplex address inputs
  . . . . . instruction code/row address/column address
- Split register avoids data transfer interval
- $\overline{HIR}$/$\overline{HOR}$ inputs reset input/output column address
- Long data hold time . . . . . 20msec (288 refresh cycles)
- Single 5V±10% power supply
- 28-pin 400 mil ZIP

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin name	Name	I/O	Function
$\overline{IRS}$/CAS	Instruction strobe/ column address strobe	Input	This clock reads the 9 bits of instruction code at the falling edge, 9 bits of column address at the rising edge.
$\overline{RAS}$/$\overline{IRE}$	Row address strobe/ instruction enable	Input	This clock reads the 9 bits of row address at the falling edge, and ends the execution of instruction at the rising edge. This clock can also be used as instruction execution enable.
$IR_0/A_0 \sim IR_8/A_8$	Instruction code/ row address/ column address	Input	This instruction code, row address and column address are multiplexed. Firstly, instruction codes are read at the falling edge of $\overline{IRS}$/CAS, then secondly row address are read in at the falling edge of $\overline{RAS}$/$\overline{IRE}$, and thirdly column address are read in at the rising edge of $\overline{IRS}$/CAS.
SIC	Serial input clock	Input	At the rising edge of SIC, the input data are written into the serial input memory (SIM). The SIM address advances to higher bits after the data are written.
$SID_1 \sim SID_4$	Serial data input	Input	Serial input pin for 4-bit data
SOC	Serial output clock	Input	At the rising edge of SOC, the output data are accessed out of the serial output memory (SOM). The SOM address advances to higher bits after the data are read.
$SOD_1 \sim SOD_4$	Serial data output	Output	Serial output pin for 4-bit data
$\overline{SOE}$	Serial output enable	Input	Enables reading of 6-bit data of serial output memory (SOM).
$\overline{HIR}$	Horizontal input address reset	Input	Reset input column address to the last set value.
$\overline{HOR}$	Horizontal output address reset	Input	Reset output column address to the last set value.
QIF	Input column address flag	Output	Indicates the busy half of the serial input register.
QOF	Output column address flag	Output	Indicates the busy half of the serial output register.