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MOS INTEGRATED CIRCUIT

μPD78P098A

8-BIT SINGLE-CHIP MICROCONTROLLER

★ The μPD78P098A is a member of the μPD78098 subseries of the 78K/0 series products, in which the on-chip mask ROM of the μPD78098A is replaced with one-time PROM.

Because a program can be written by the user, the μPD78P098A is ideal for evaluation of a system under development, small-scale production of a variety of systems, and early start of production of a system.

The functions are explained in detail in the following manuals. Be sure to read these manuals when designing your system.

μPD78098 Subseries User's Manual : IEU-1381

★ **78K/0 Series User's Manual - Instruction: U12326E**

FEATURES

- Pin-compatible with mask ROM model (except V_{PP} pin)
- Internal PROM: 60K bytes[Note 1]
- Internal high-speed RAM : 1024 bytes
- Buffer RAM : 32 bytes
- Internal expansion RAM : 2048 bytes[Note 2]
- Operating voltage same as mask ROM model (V_{DD} = 2.7 to 5.5 V)
- Supports QTOP™ microcontroller

Notes 1. The internal PROM capacity can be changed by using the memory size select register(IMS).

2. Internal expansion RAM capacity can be changed by using the internal expansion RAM size select register(IXS).

Remark "QTOP microcontroller" is a generic name for one-time PROM-containing microcontrollers totally supported by NEC's writing service (writing, marking, screening, and inspection).

The μPD78P098A differs from the mask ROM model in the following points:

- The memory can be mapped in the same manner as the mask ROM model by using the memory size select register(IMS) and internal expansion RAM size select register(IXS).
- The P60 through P63 pins are not provided with pull-up resistors.

Document No. U10203EJ2V0DS00 (2nd edition)
Date Published June 2001 N CP(K)
Printed in Japan

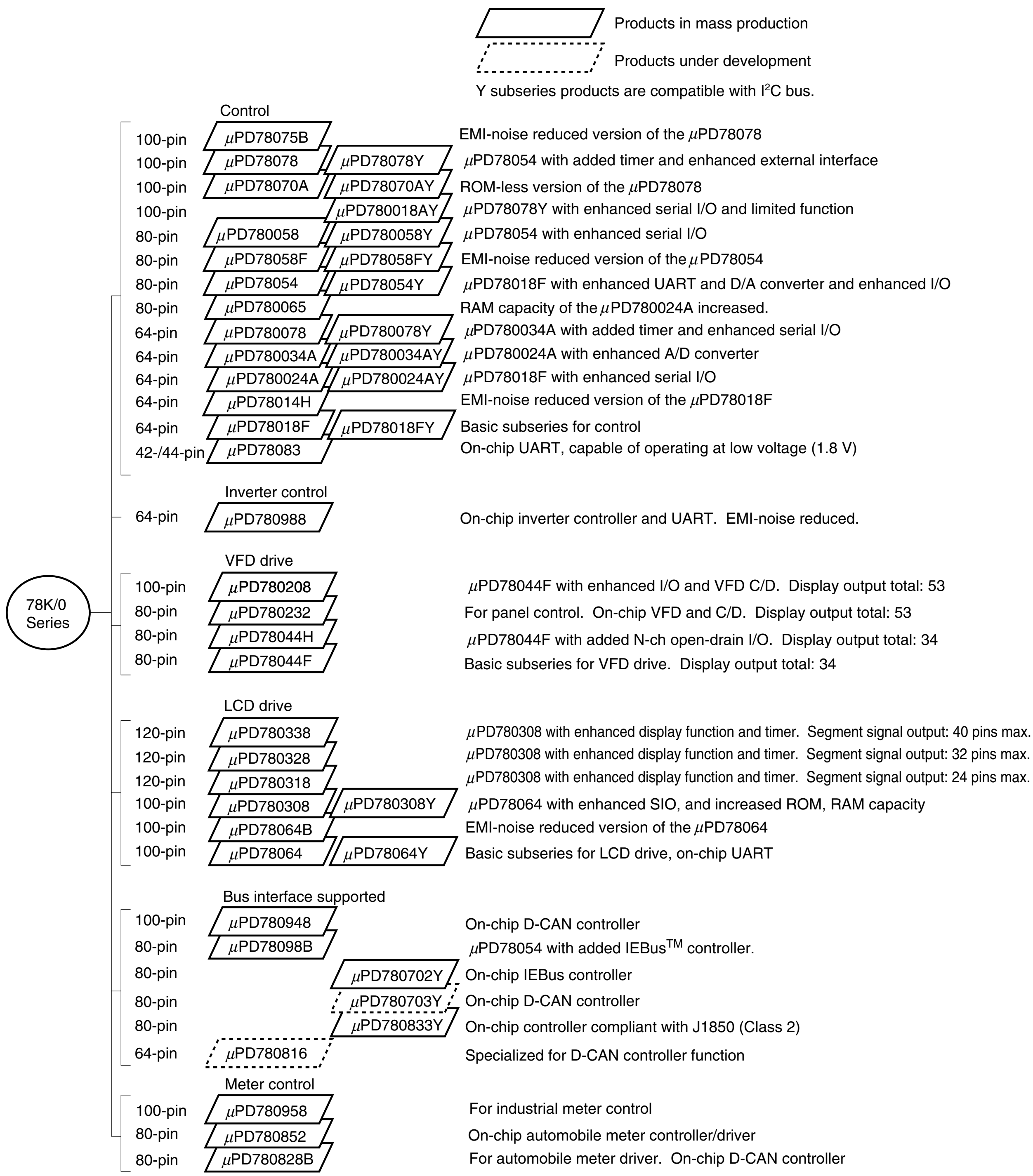
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
★ μPD78P098AGC-8BT	80-pin plastic QFP (14 × 14)

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

Subseries Name		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 64 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

Functional Outline

Item		Function
Internal memory		• PROM : 60K bytes[Note 1] • RAM Internal high-speed RAM : 1024 bytes Buffer RAM : 32 bytes Internal expansion RAM : 2048 bytes[Note 2]
Memory space		64K bytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		Variable instruction execution time
	With main system clock	0.5 μs/1.0 μs/2.0 μs/4.0 μs/8.0 μs/16.0 μs (at 6.0 MHz)
	With subsystem clock	122 μs (at 32.768 kHz)
Instruction set•		16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc.
I/O port		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4
IEBus controller		Effective transmission rate: 3.9 kbps/17 kbps/26 kbps
A/D converter		8-bit resolution × 8 channels
D/A converter		8-bit resolution × 2 channels
Serial interface		• 3-line/SBI/2-line mode selectable : 1 channel • 3-line mode (with function to automatically transfer/ receive 32 bytes max.) : 1 channel • 3-line/UART mode selectable : 1 channel
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 (14-bit PWM output: 1)
Clock output		15.6 kHz, 31.3 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1.0 MHz, 2.0 MHz, 4.0 MHz (with 6.0-MHz main system clock) 32.768 kHz (with 32.768-kHz subsystem clock)
Buzzer output		977 Hz, 1.95 kHz, 3.9 kHz, 7.8 kHz (with 6.0-MHz main system clock)

Notes 1. The internal PROM capacity can be changed by using the memory size select register (IMS).

2. 0 or 2048 bytes can be selected by using the internal expansion RAM size select register (IXS).

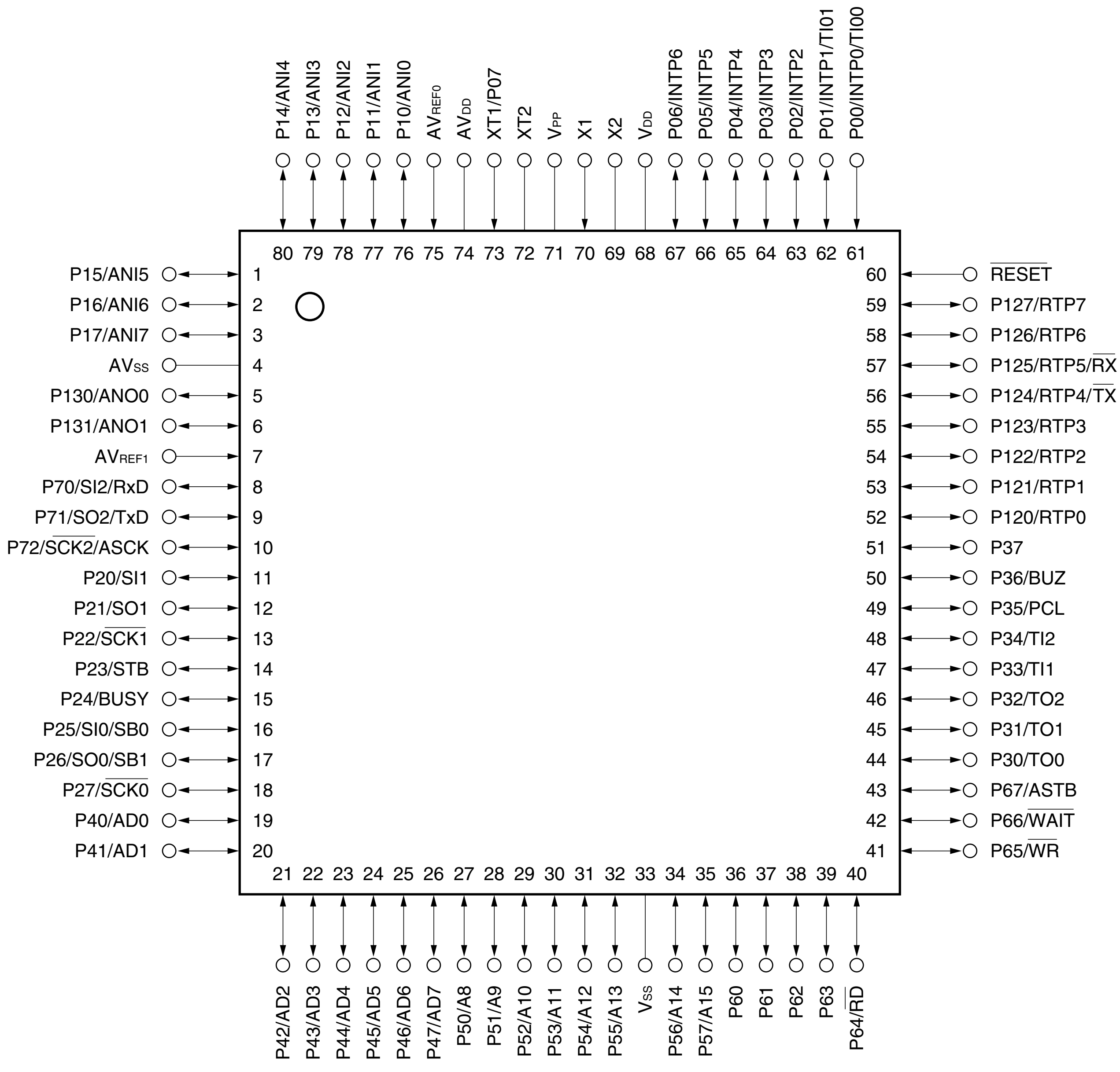
Item		Function
Vector interrupt	Maskable interrupt	Internal: 14, external: 7
	Non-maskable interrupt	Internal: 1
	Software interrupt	1
Test input		Internal: 1, external: 1
Operating voltage		V_{DD} = 2.7 to 5.5 V
★ Package		• 80-pin plastic QFP (14 × 14)

PIN CONFIGURATION (Top View)

(1) Normal operation mode

- **80-pin plastic QFP (14 × 14)**

★ **μPD78P098AGC-8BT**



Cautions 1. Directly connect the V_{PP} pin to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

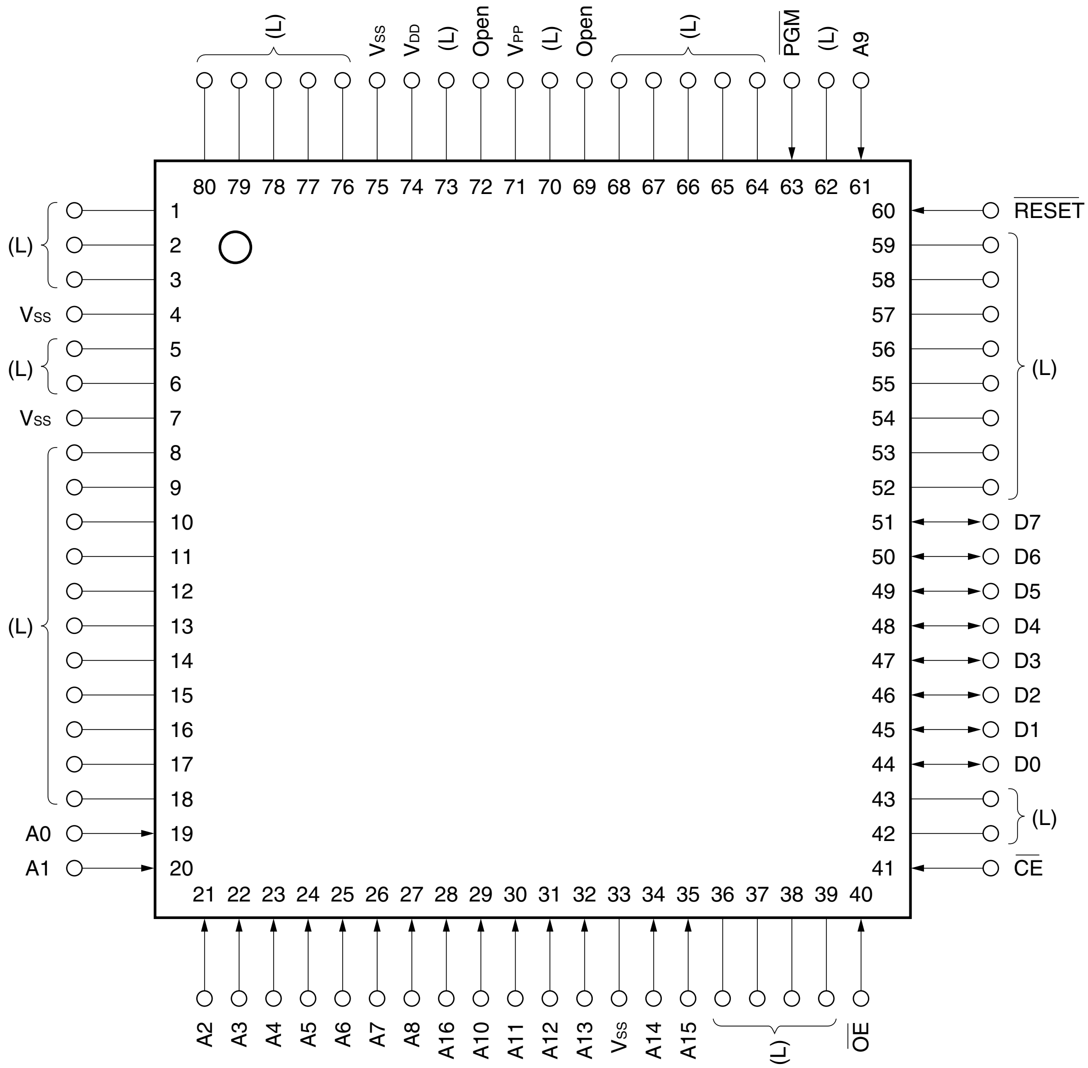
P00-P07	:	Port0
P10-P17	:	Port1
P20-P27	:	Port2
P30-P37	:	Port3
P40-P47	:	Port4
P50-P57	:	Port5
P60-P67	:	Port6
P70-P72	:	Port7
P120-P127	:	Port12
P130, P131	:	Port13
RTP0-RTP7	:	Real-Time Output Port
INTP0-INTP6	:	Interrupt from Peripherals
TI00, TI01	:	Timer Input
TI1, TI2	:	Timer Input
TO0-TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0-SI2	:	Serial Input
SO0-SO2	:	Serial Output
$\overline{SCK0}$-$\overline{SCK2}$	:	Serial Clock
RxD	:	Receive Data (UART)
TxD	:	Transmit Data (UART)
ASCK	:	Asynchronous Serial Clock

$\overline{RX}$	:	Receive Data (IEBus Controller)
$\overline{TX}$	:	Transmit Data (IEBus Controller)
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
AD0-AD7	:	Address/Data Bus
A8-A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0-ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
$AV_{REF0, 1}$	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground

(2) **PROM programming mode**

- **80-pin plastic QFP (14 × 14)**

★ **μPD78P098AGC-8BT**



Cautions 1. (L) : Individually connect these pins to V_{SS} via a pull-down resistor.

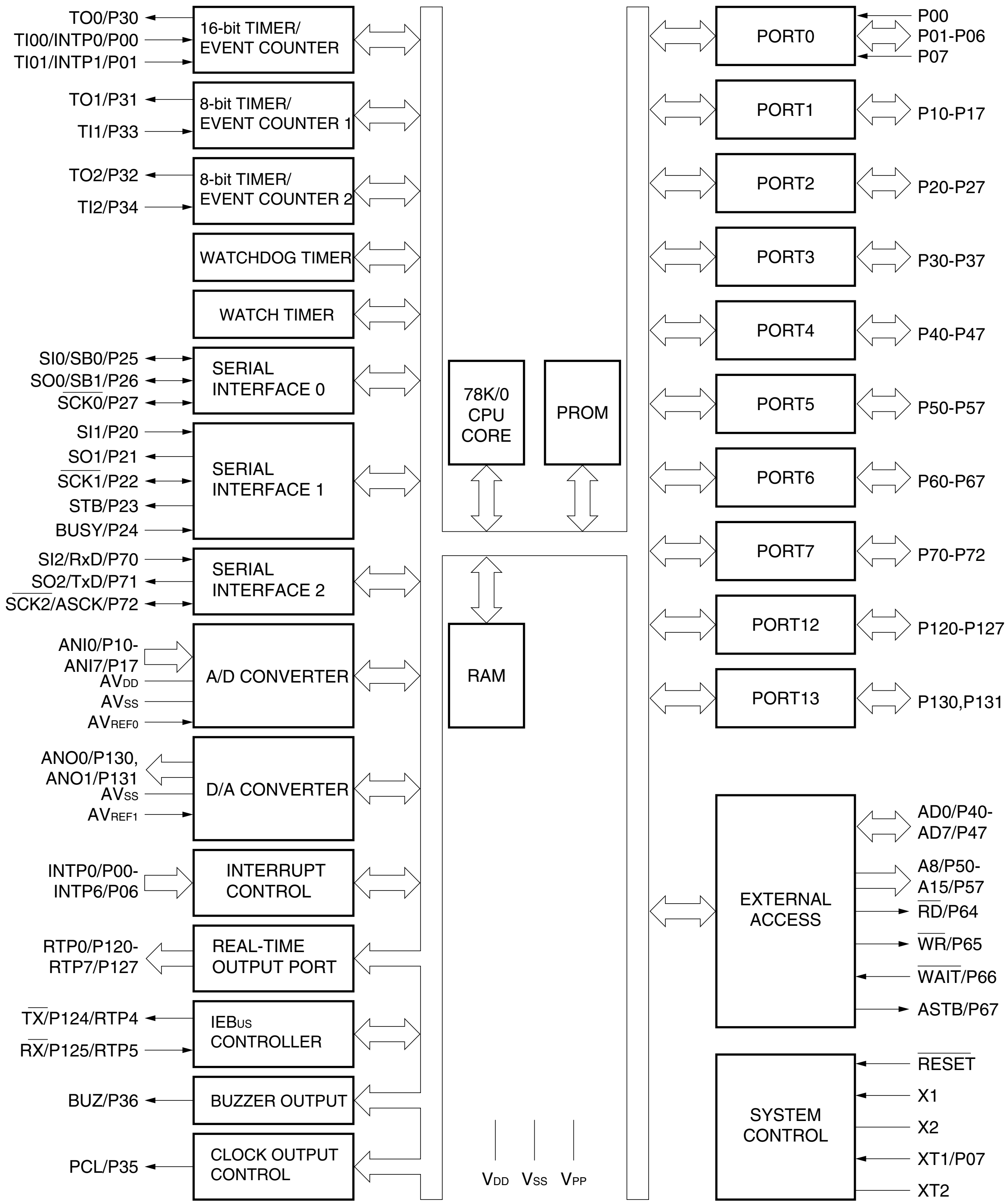
2. V_{SS} : Connect this pin to ground.

3. $\overline{\text{RESET}}$: Keep this pin to the low level.

4. Open : Connect nothing to these pins.

A0-A16	:	Address Bus	$\overline{\text{RESET}}$	:	Reset
D0-D7	:	Data Bus	V_{DD}	:	Poewr Supply
$\overline{\text{CE}}$	:	Chip Enable	V_{PP}	:	Programming Power Supply
$\overline{\text{OE}}$	:	Output Enable	V_{SS}	:	Ground
$\overline{\text{PGM}}$	:	program			

BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN μPD78P098A AND MASK ROM MODEL

★ The μPD78P098A is provided with a one-time PROM to which a program can be written only once.

The functions of the μPD78P098A, except the PROM specification and the mask option of P60 through P63 pins, can be set to be the same as those of the mask ROM model by using the memory size select register and internal expansion RAM size select register.

Table 1-1 shows the differences between the μPD78P098A and mask ROM model.

Table 1-1. Differences between μPD78P098A and Mask ROM Model

Item	μPD78P098A	Mask ROM Model
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
Mask option of P60-P63 pins	Pull-up resistor not provided	Pull-up resistor can be provided by mask option

Cautions 1. The internal ROM capacity of the μPD78P098A can be changed by using the memory size select register. The internal PROM capacity is set to 60K bytes at $\overline{\text{RESET}}$.

2. The internal expansion RAM capacity of the μPD78P098A can be changed by using the internal expansion RAM size select register.
The internal expansion RAM capacity is set to 2K bytes at $\overline{\text{RESET}}$.

2. PIN FUNCTIONS

2.1 Pins in Normal Operation Mode

(1) Port pins (1/2)

Pin Name	I/O	Function		At Reset	Shared with:
P00	Input	Port 0. 8-bit I/O port	Input only	Input	INTP0/TI00
P01	I/O		Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 Note 1	Input		Input only	Input	XT1
P10-P17	I/O	Port 1. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software. Note 2		Input	ANI0-ANI7
P20	I/O	Port 2. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	I/O	Port 3. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as an input port, a pull-up resistor can be connected via software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–

Notes 1. When using the P07/XT1 pin as an input port pin, set bit 6 (FRC) of the processor clock control register to 1 and do not use the feedback resistor of the subsystem clock oscillation circuit.

2. When using the P10/ANI0 through P17/ANI7 pins as analog input pins of the A/D converter, the pull-up resistors are automatically disconnected.

(1) Port pins (2/2)

<table>
<tr><th>Pin Name</th><th>I/O</th><th colspan="2">Function</th><th>At Reset</th><th>Shared with:</th></tr>
<tr><td>P40-P47</td><td>I/O</td><td colspan="2">Port 4.
8-bit I/O port.
Can be set in input or output mode in 8-bit units.
When used as an input port, a pull-up resistor can be connected via software.
Test input flag (KRIF) is set to 1 at falling edge of this port.</td><td>Input</td><td>AD0-AD7</td></tr>
<tr><td>P50-P57</td><td>I/O</td><td colspan="2">Port 5.
8-bit I/O port.
Can directly drive LED.
Can be set in input or output mode in 1-bit units.
When used as an input port, a pull-up resistor can be connected via software.</td><td>Input</td><td>A8-A15</td></tr>
<tr><td>P60</td><td rowspan="8">I/O</td><td rowspan="8">Port 6.
8-bit I/O port.
Can be set in input or output mode in 1-bit units.</td><td rowspan="4">N-ch open-drain I/O port.
Can directly drive LED.</td><td rowspan="4">Input</td><td rowspan="4">–</td></tr>
<tr><td>P61</td></tr>
<tr><td>P62</td></tr>
<tr><td>P63</td></tr>
<tr><td>P64</td><td rowspan="4">When used as an input port, a pull-up Input resistor can be connected via software.</td><td rowspan="4">Input</td><td>$\overline{RD}$</td></tr>
<tr><td>P65</td><td>$\overline{WR}$</td></tr>
<tr><td>P66</td><td>$\overline{WAIT}$</td></tr>
<tr><td>P67</td><td>ASTB</td></tr>
<tr><td>P70</td><td rowspan="3">I/O</td><td colspan="2" rowspan="3">Port 7.
3-bit I/O port.
Can be set in input or output mode in 1-bit units.
When used as an input port, a pull-up resistor can be connected via software.</td><td rowspan="3">Input</td><td>SI2/RxD</td></tr>
<tr><td>P71</td><td>SO2/TxD</td></tr>
<tr><td>P72</td><td>$\overline{SCK2}$/ASCK</td></tr>
<tr><td>P120-P123</td><td rowspan="4">I/O</td><td colspan="2" rowspan="4">Port 12.
8-bit I/O port.
Can be set in input or output mode in 1-bit units.
When used as an input port, a pull-up resistor can be connected via software.</td><td rowspan="4">Input</td><td>RTP0-RTP3</td></tr>
<tr><td>P124</td><td>RTP4/$\overline{TX}$</td></tr>
<tr><td>P125</td><td>RTP5/$\overline{RX}$</td></tr>
<tr><td>P126, P127</td><td>RTP6, RTP7</td></tr>
<tr><td>P130, P131</td><td>I/O</td><td colspan="2">Port 13.
2-bit I/O port.
Can be set in input or output mode in 1-bit units.
When used as an input port, a pull-up resistor can be connected via software.</td><td>Input</td><td>ANO0, ANO1</td></tr>
</table>

(2) Pins other than port pins (1/2)

Pin Name	I/O	Function	At Reset	Shared with:
INTP0	Input	External interrupt input whose valid edge can be specified (rising edge, falling edge, and both rising and falling edges).	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial data input to serial interface.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial data output from serial interface.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial data input/output of serial interface.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial clock input/output of serial interface.	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Strobe signal output for serial interface automatic transmission/reception.	Input	P23
BUSY	Input	Busy input for serial interface automatic transmission/reception.	Input	P24
RxD	Input	Serial data input to asynchronous serial interface.	Input	P70/SI2
TxD	Output	Serial data output from asynchronous serial interface.	Input	P71/SO2
ASCK	Input	Serial clock input to asynchronous serial interface.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer output (TM1).		P31
TO2		8-bit timer output (TM2)		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0-RTP3	Output	Real-time output port outputting data in synchronization with trigger.	Input	P120-P123
RTP4				P124/$\overline{TX}$
RTP5				P125/$\overline{RX}$
RTP6, RTP7				P126, P127
$\overline{TX}$	Output	Data output for IEBus controller.	Input	P124/RTP4
$\overline{RX}$	Input	Data input for IEBus controller.	Input	P125/RTP5

(2) Pins other than port pins (2/2)

Pin Name	I/O	Function	At Reset	Shared with:
AD0-AD7	I/O	Low-order address/data bus when external memory is connected.	Input	P40-P47
A8-A15	Output	High-order address bus when external memory is connected.	Input	P50-P57
$\overline{RD}$	Output	Strobe signal output for read operation on external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation on external memory.	Input	P65
$\overline{WAIT}$	Input	Wait state insertion for external memory access.	Input	P66
ASTB	Output	Strobe output to externally latch address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0-ANI7	Input	Analog input of A/D converter.	Input	P10-P17
ANO0, ANO1	Output	Analog output of D/A converter.	Input	P130, P131
AV_{REF0}	Input	Reference voltage input of A/D converter.	–	–
AV_{REF1}	Input	Reference voltage input of D/A converter.	–	–
AV_{DD}	–	Analog power supply of A/D converter. Connected to V_{DD}.	–	–
AV_{SS}	–	Ground of A/D converter. Connected to V_{SS}.	–	–
$\overline{RESET}$	Input	System reset input.	–	–
X1	Input	Crystal connection for main system clock oscillation.	–	–
X2	–		–	–
XT1	Input	Crystal connection for subsystem clock oscillation.	Input	P07
XT2	–		–	–
V_{DD}	–	Positive power supply.	–	–
V_{PP}	–	High-voltage application for program write/verify. Directly connected to V_{SS} in normal operation mode.	–	–
V_{SS}	–	Ground.	–	–

2.2 Pins in PROM Programming Mode

Pin Name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V_{PP} pin, and low level is applied to the $\overline{RESET}$ pin, PROM programming mode is set.
V_{PP}	Input	PROM programming mode setting and high voltage application for program write/verify.
A0-A16	Input	Address bus.
D0-D7	I/O	Data bus.
$\overline{CE}$	Input	PROM enable input/program pulse input.
$\overline{OE}$	Input	Read strobe input to PROM.
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	–	Positive power supply.
V_{SS}	–	Ground.

2.3 Pin I/O Circuits and Handling of Unused Pins

Table 2-1 shows the types of the I/O circuits for the various pins and handling of unused pins.

For the configuration of the various I/O circuits, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection When Not Used
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	I/O	Individually connect to V_{SS} via resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD} or V_{SS}.
P10/ANI0-P17/ANI7	11	I/O	Individually connect to V_{DD} or V_{SS} via resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0-P47/AD7	5-E		Individually connect to V_{DD} via resistor.
P50/A8-P57/A15	5-A		Individually connect to V_{DD} or V_{SS} via resistor.
P60-P63	13-D		Individually connect to V_{DD} via resistor.
P64/$\overline{RD}$	5-A		Individually connect to V_{DD} or V_{SS} via resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 2-1. I/O Circuit Type of Each Pin (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection When Not Used
P70/SI2/RxD	8-A	I/O	Individually connect to V_{DD} or V_{SS} via resistor.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0-P123/RTP3	5-A		
P124/RTP4/$\overline{TX}$			
P125/RTP5/$\overline{RX}$			
P126/RTP6, P127/RTP7			
P130/ANO0, P131/ANO1	12-A		Individually connect to V_{SS} via resistor.
$\overline{RESET}$	2	Input	–
XT2	16	–	Open
AV_{REF0}	–		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
V_{PP}			Directly connect to V_{SS}.

Figure 2-1. I/O Circuits of Pins (1/2)

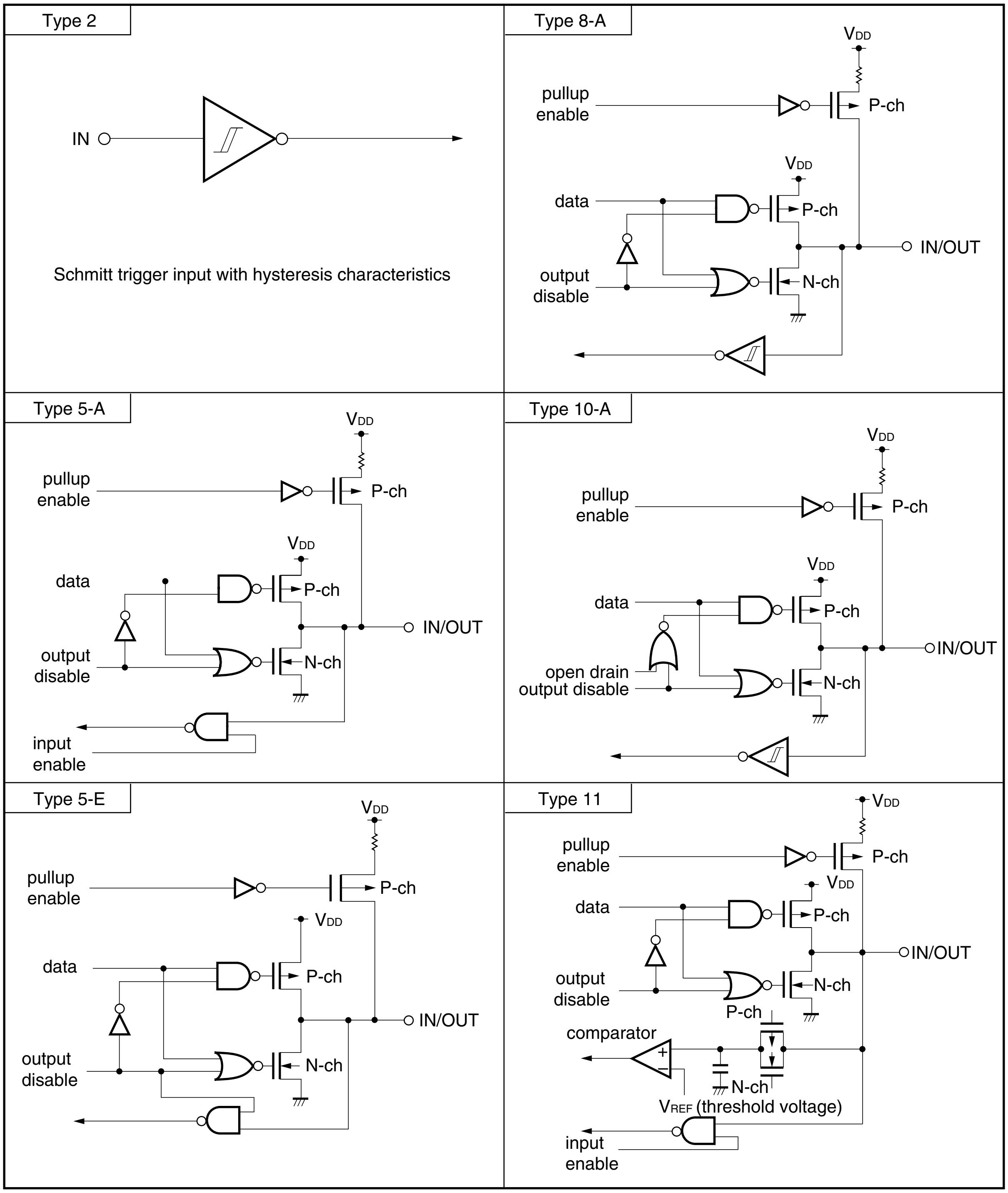
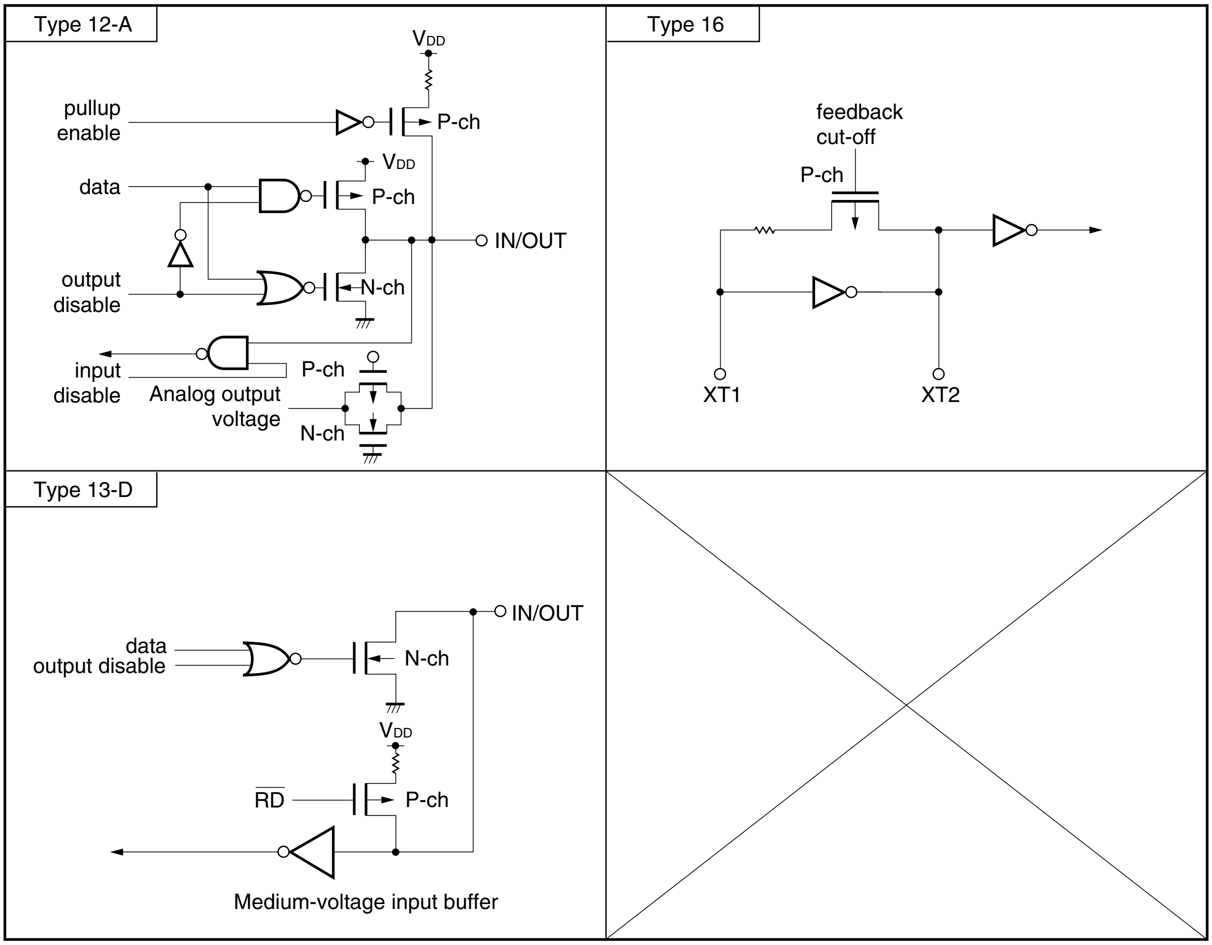


Figure 2-1. I/O Circuits of Pins (2/2)



3. MEMORY SIZE SELECT REGISTER (IMS)

This register specifies via software that part of the internal memory is not used. By using this register, the internal memory (ROM) of the μPD78P098A can be mapped in the same manner as a mask ROM model.

IMS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to CFH at $\overline{\text{RESET}}$.

Figure 3-1. Format of the Memory Size Select Register

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
1	0	0	0	32K bytes
1	0	1	0	40K bytes
1	1	0	0	48K bytes
1	1	1	0	56K bytes[Note]
1	1	1	1	60K bytes
Others				Setting prohibited

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
1	1	0	1024 bytes
Others			Setting prohibited

Note When using the external device expansion function, set the internal PROM capacity to 56K bytes or less.

Table 3-1 shows the value settings of IMS to map the memory of the μPD78P098A in the same manner as the respective mask ROM models.

Table 3-1. Value Settings of the Memory Size Select Register

Mask ROM Model	IMS Value Setting
μPD78094	C8H
μPD78095	CAH
μPD78096	CCH
μPD78098A	CFH

4. INTERNAL EXPANSION RAM SIZE SELECT REGISTER (IXS)

This register specifies the internal expansion RAM capacity via software. By using this register, the internal expansion RAM of the μPD78P098A can be mapped in the same manner as a mask ROM model.

IXS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to 08H at $\overline{\text{RESET}}$.

Figure 4-1. Format of Internal Expansion RAM Size Select Register

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	08H	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selects internal expansion RAM capacity
1	1	0	0	No internal expansion RAM
1	0	0	0	2048 bytes (F000H-F7FFH)
Others				Setting prohibited

Table 4-1 shows the value settings of IXS to map the internal expansion RAM of the μPD78P098A in the same manner as the respective mask ROM models.

Table 4-1. Value Settings of Internal Expansion RAM Size Select Register

Mask ROM Model	IXS Value Setting
μPD78094	0CH Note
μPD78095	
μPD78096	
μPD78098A	08H

Note Even when a program for the μPD78P098A in which "MOV IXS, #0CH" is coded is executed on the μPD78094, 78095, or 78096, operation is unaffected.

5. PROM PROGRAMMING

The μPD78P098A is provided with a 60K-byte PROM as a program memory. When programming this memory, it must be set in the PROM programming mode by using the V_{PP} and $\overline{\text{RESET}}$ pins. For the handling of the unused pins, refer to **(2) PROM programming mode** in **PIN CONFIGURATION (Top View)**.

Caution Write the program to addreses in the range 0000H through EFFFH (specify the last address as EFFFH). A program cannot be written with a PROM programmer that cannot specify write addresses.

5.1 Operation Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and low level is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set. In this mode, the operation modes shown in Table 5-1 can be selected by using the $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{PGM}}$ pins.

The contents of the PROM can be read in the read mode.

Table 5-1. Operation Modes in PROM Programming Mode

Pin / Operation Mode	$\overline{\text{RESET}}$	V_{PP}	V_{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

Remark ×: L or H

(1) Read mode

This mode is set when both the $\overline{CE}$ and $\overline{OE}$ pins are made low.

(2) Output disable mode

When the $\overline{OE}$ pin is made high, data output goes into a high-impedance state, and the output disable mode is set.

If two or more μPD78P098As are connected to the data bus, therefore, data can be read from any one of the devices by controlling the $\overline{OE}$ pin.

(3) Standby mode

The standby mode is set when the $\overline{CE}$ pin is made high.

In this mode, data output goes into a high-impedance state regardless of the status of the $\overline{OE}$ pin.

(4) Page data latch mode

The page data latch mode is set when the $\overline{CE}$ and $\overline{PGM}$ pins are made high and the $\overline{OE}$ pin is made low at the beginning of the page write mode.

In this mode, data of 1 page and 4 bytes is latched to the internal address/data latch circuit.

(5) Page write mode

Page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with the $\overline{CE}$ and $\overline{OE}$ pins made high after addresses and data of 1 page and 4 bytes have been latched in the page data latch mode. After that, the program can be verified by making both the $\overline{CE}$ and $\overline{OE}$ pins low.

If the program cannot be written by one program pulse, writing and verifying are repeated X times ($X \leq 10$).

(6) Byte write mode

Byte write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with the $\overline{CE}$ pin made low and $\overline{OE}$ pin high. The program is verified by later making the $\overline{OE}$ pin low.

If the program cannot be written by one program pulse, writing and verifying are repeated X times ($X \leq 10$).

(7) Program verify mode

Program verify mode is set when the $\overline{CE}$ and $\overline{OE}$ pins are made low and the $\overline{PGM}$ pin is made high.

After writing the program, check in this mode whether the program has been correctly written.

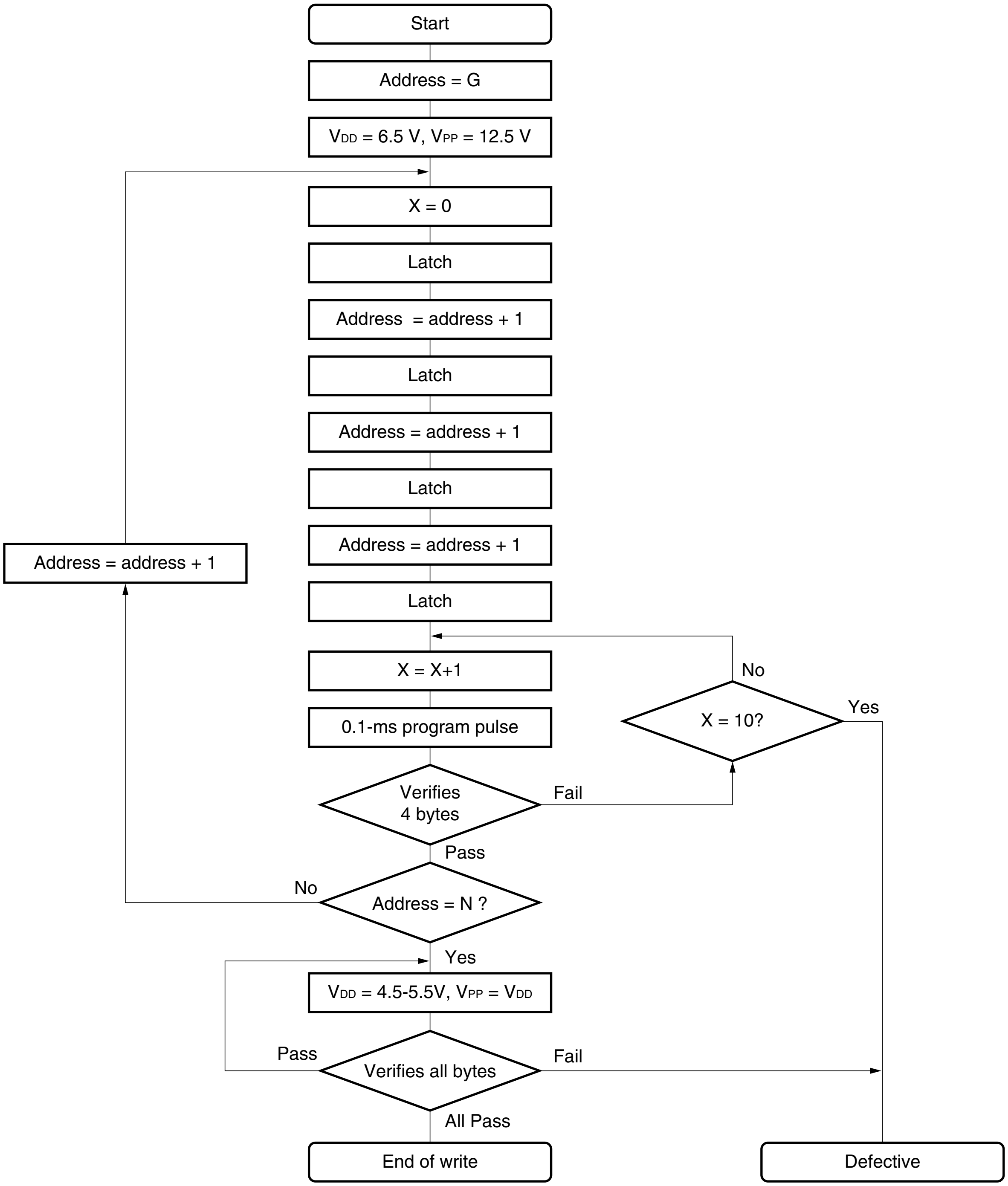
(8) Program inhibit mode

This mode is used to write a program to one of two or more μPD78P098As with the $\overline{OE}$, V_{PP}, and D0 through D7 pins connected in parallel.

To write a program, the page write or byte write mode described above is used. At this time, the program is not written to those devices whose $\overline{PGM}$ pin is made high.

5.2 PROM Writing Procedure

Figure 5-1. Page Program Mode Flowchart



G = start address

N = end address of program

Figure 5-2. Page Program Mode Timing

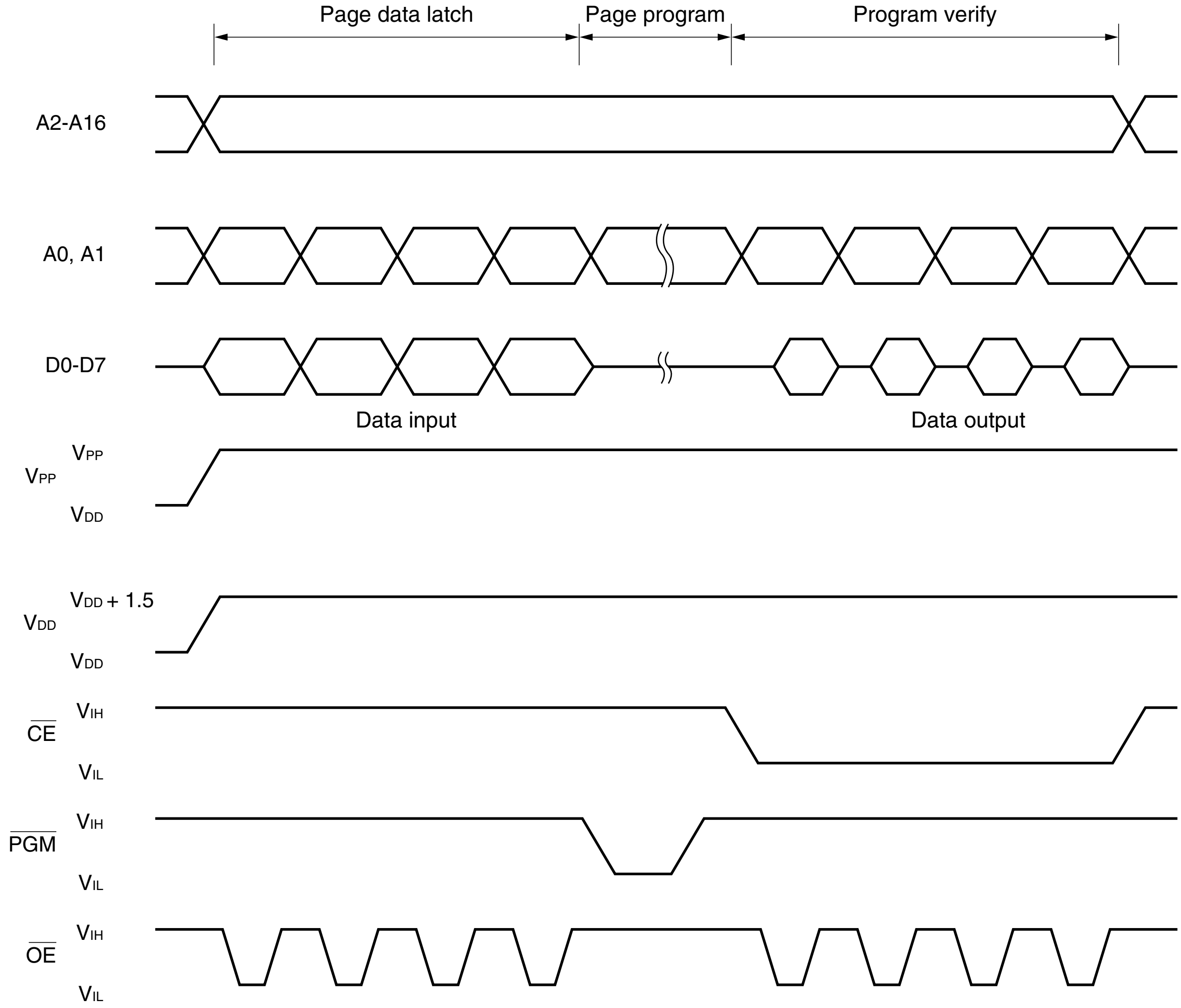
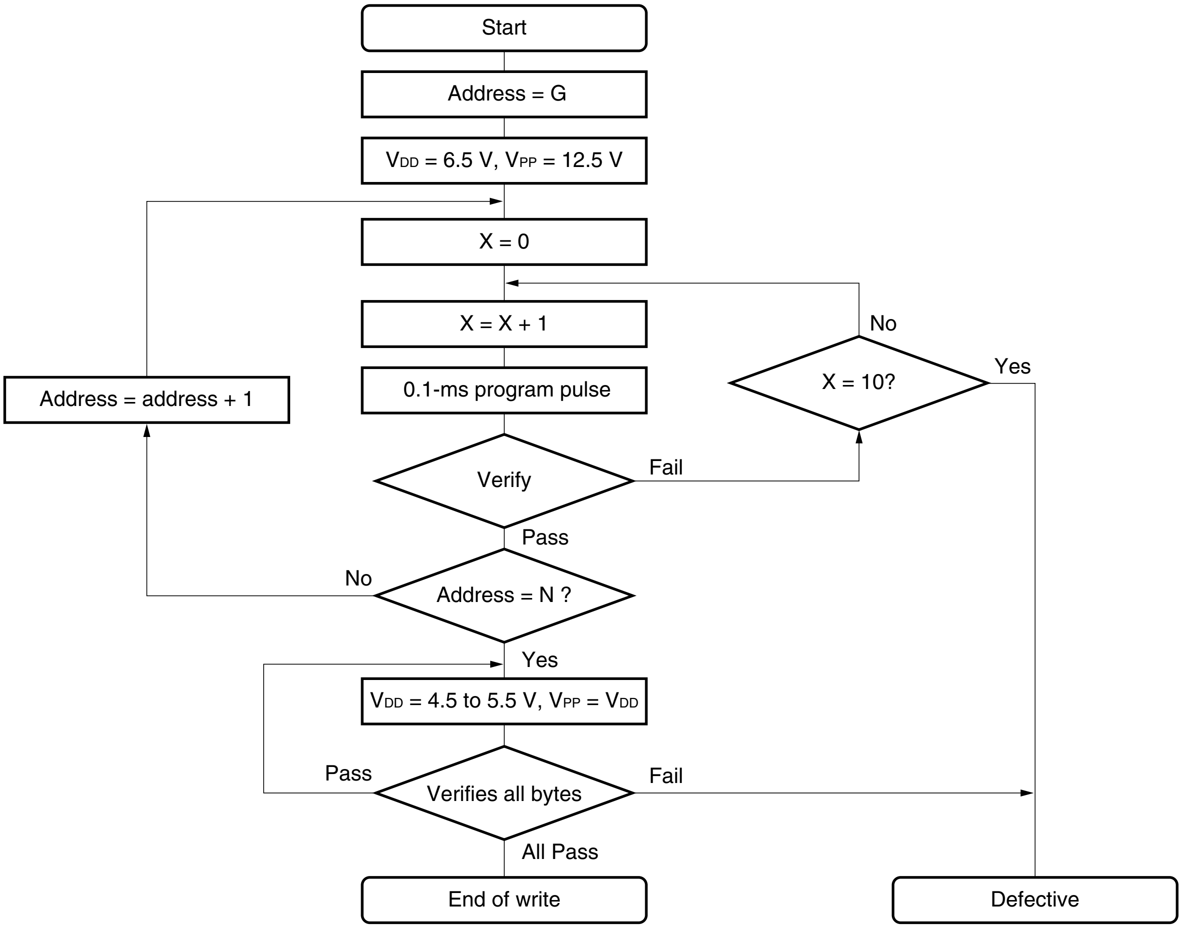


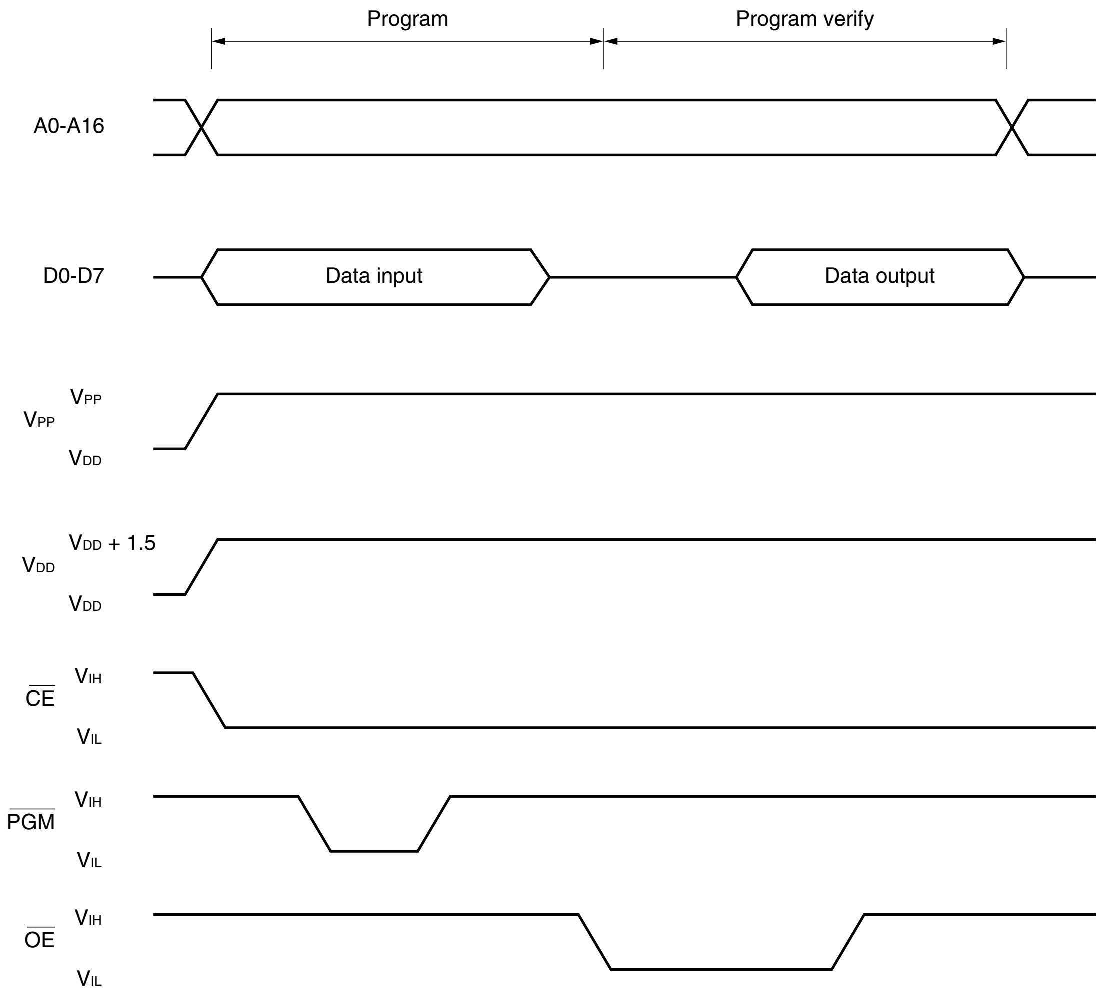
Figure 5-3. Byte Program Mode Flowchart



G = start address

N = end address of program

Figure 5-4. Byte Program Mode Timing



Cautions 1. Apply V_{DD} before V_{PP} and turn off V_{DD} after V_{PP}.

2. Keep V_{PP} from going above +13.5 V, including overshoot.

3. If the device is inserted into or pulled out of the socket while +12.5 V is applied to V_{PP}, the reliability may be adversely affected.

5.3 PROM Read Procedure

The contents of the PROM can be read out to the external data bus (D0 through D7) in the following procedure:

(1) Fix the $\overline{\text{RESET}}$ pin to the low level. Supply +5 V to the V_{PP} pin. Process the unused pins as described in **(2) PROM programming mode** in **PIN CONFIGURATION (Top View)**.

(2) Supply +5 V to the V_{DD} and V_{PP} pins.

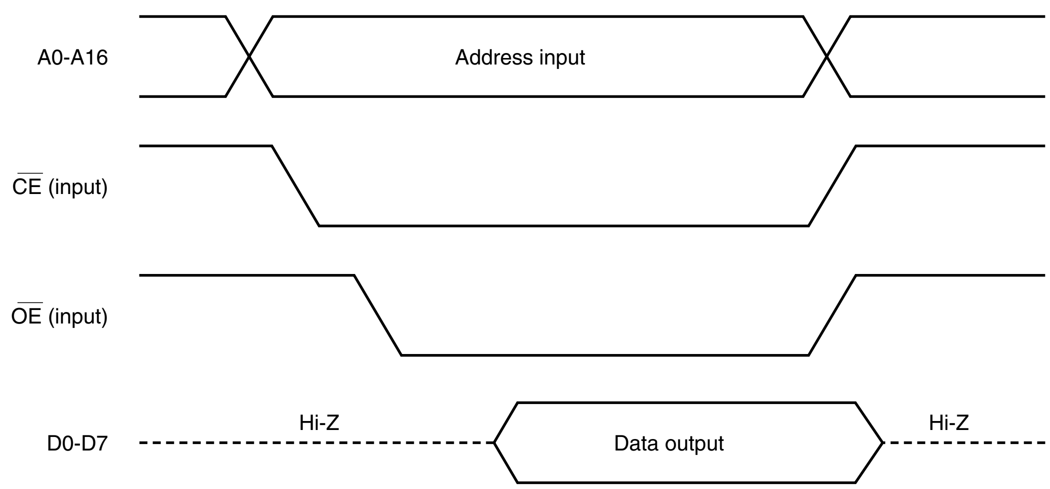
(3) Input the address of the data to be read to the A0 through A16 pins.

(4) The read mode is set.

(5) Data is output to the D0 through D7 pins.

Figure 5-5 shows the timing of steps (2) through (5) above.

Figure 5-5. PROM Read Timing



6. SCREENING OF ONE-TIME PROM MODEL

★ The one-time PROM model (μPD78P098AGC-8BT) cannot be completely tested by NEC before shipment. It is recommended that screening be implemented to verify the PROM after data has been written to the PROM and the device has been stored under the following conditions:

Storage Temperature	Storage Time
125 °C	24 hours

NEC provides a writing, marking, screening, and verifying service for one-time PROMs, called QTOP microcontroller. This service for the μPD78P098A is in preparation. For details, consult NEC.

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

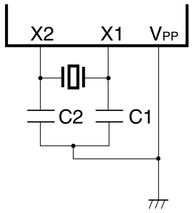
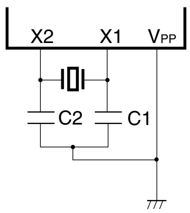
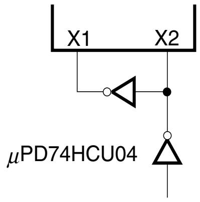
Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} +0.3	V
	AV_{REF0}			–0.3 to V_{DD} +0.3	V
	AV_{REF1}			–0.3 to V_{DD} +0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to 47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{RESET}$		–0.3 to V_{DD} +0.3	V
	V_{I2}	P60 to P63	N-ch open drain	–0.3 to +16	V
	V_{I3}	A9	PROM programming mode	–0.3 to +13.5	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} –0.3 to AV_{REF0} +0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127		–15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		–15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			R.m.s. value	15	mA
		Total for P50 to P55	Peak value	100	mA
			R.m.s. value	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			R.m.s. value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	Peak value	50	mA
			R.m.s. value	20	mA
		Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127	Peak value	50	mA
			R.m.s	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C
Total power dissipation	P_d			650	mW

Note The r.m.s. value should be calculated as follows: [R.m.s. value] = [Peak value] x $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T$_A$ = –40 to +85°C, V$_{DD}$ = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillatior frequency (f$_X$)Note1	V$_{DD}$ = Oscillation voltage range	1.0	6.0	6.29	MHz
		Oscillatior stabilization timeNote2	After V$_{DD}$ has reached MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillatior frequency (f$_X$)Note1		1.0	6.0	6.29	MHz
		Oscillatior stabilization timeNote2	V$_{DD}$ = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f$_X$)Note1		1.0	6.0	6.29	MHz
		X1 input high-/low-level width (t$_{XH}$/t$_{XL}$)	When f$_{XX}$ = f$_X$	85		500	ns
			Other than above	72		500	ns

Notes 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.

2. This is the time required for oscillation to stabilize after a reset or STOP mode release.

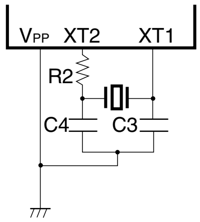
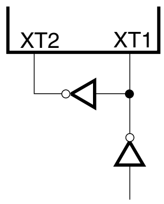
Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V$_{SS}$.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

SUBSYSTEM CLOCK OSILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note1]		32	32.768	35	MHz
		Oscillation stabilization time[Note2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		X1 input frequency (f_{XT})[Note1]		32		100	kHz
		X1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.
2. This is the time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63, N-ch open drain		0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD}–0.5		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131		0		0.3 V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	P60 to P63, N-ch open drain	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P07, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} –1.0			V
		I_{OH} = –100 μA		V_{DD} –0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 5.5 V, Open drain, at pulled up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3 Note	μA
Output leakage current high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	VIN = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 ≤ V_{DD} < 4.5 V	20		500	kΩ

Note For P60-P63, a low-level input leak current of –200 μA (MAX.) flows only during the 1.5 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 1.5 clocks following execution a read-out instruction, the current is –3 μA (MAX.).

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note2]	V_{DD} = 5.0V±10%[Note6]		5	15	mA
			V_{DD} = 3.0V±10%[Note7]		0.7	2.7	mA
		5.0 MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note3]	V_{DD} = 5.0V±10%[Note6]		9	30	mA
			V_{DD} = 3.0V±10%[Note7]		1	3.7	mA
		6.29 MHz crystal oscillation operating mode (f_{XX} = 2.1 MHz)[Note4]	V_{DD} = 5.0V±10%[Note6]		4.8	17.4	mA
		6.29 MHz crystal oscillation operating mode (f_{XX} = 4.19 MHz)[Note5]	V_{DD} = 5.0V±10%[Note6]		8.5	28.5	mA

Notes 1. Currents AV_{REF0}, AV_{REF1}, AV_{DD}, and the port current (including the current flowing in the internal pull-up resistor) are not included.

2. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.

3. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.

4. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.

5. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.

6. When in high-speed mode (when the processor clock control register has been set to 00H).

7. When in low-speed mode (when the processor clock control register has been set to 04H).

Remark f_{XX}: Main system clock frequency

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0V±10% Note 7		1.5	4.5	mA
			V_{DD} = 3.0V±10% Note 8		0.5	1.5	mA
		5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0V±10% Note 7		1.8	5.4	mA
			V_{DD} = 3.0V±10% Note 8		0.7	2.1	mA
		6.29 MHz crystal oscillation HALT mode (f_{XX} = 2.1 MHz) Note 4	V_{DD} = 5.0V±10% Note 7		1.5	4.5	mA
		6.29 MHz crystal oscillation HALT mode (f_{XX} = 4.19 MHz) Note 5	V_{DD} = 5.0V±10% Note 7		1.8	5.4	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode Note 6	V_{DD} = 5.0V±10%		135	270	μA
			V_{DD} = 3.0V±10%		95	190	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 6	V_{DD} = 5.0V±10%		25	55	μA
			V_{DD} = 3.0V±10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode Feedback resistor used	V_{DD} = 5.0V±10%		1	30	μA
			V_{DD} = 3.0V±10%		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode Feedback resistor not used	V_{DD} = 5.0V±10%		0.1	30	μA
			V_{DD} = 3.0V±10%		0.05	10	μA

Notes 1. Currents AV_{REF0}, AV_{REF1}, AV_{DD}, and the port current (including the current flowing in the internal pull-up resistor) are not included.

2. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.

3. When bit 0 of clock switchover selection register 1 has been set to 0, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.

4. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 00H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.

5. When bit 0 of clock switchover selection register 1 has been set to 1, bit 0 of clock switchover selection register 2 has been set to 0, and the oscillator mode selection register has been set to 01H.
Indicates only the power supply current characteristic. For IEBus ratings, refer to the IEBus controller characteristics.

6. When the main system clock is stopped.

7. When in high-speed mode (when the processor clock control register has been set to 00H).

8. When in low-speed mode (when the processor clock control register has been set to 04H).

Remark f_{XX} : Main system clock frequency

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time	T_{CY}	Operating on main	$f_{XX} = f_X/3$	4.0 V ≤ V_{DD} ≤ 5.5 V	0.95		64	μs
(minimum instruction		system clock	$f_{XX} = f_X/6$	2.7 V ≤ V_{DD} ≤ 5.5 V	1.91		64	μs
execution timke)		(MCS = 0 Note 1)	$f_{XX} = f_X/9$	4.0 V ≤ V_{DD} ≤ 5.5 V	2.86		64	μs
			$f_{XX} = f_X/2$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8		64	μs
		Operating on main	$f_{XX} = 2f_X/3$	4.5 V ≤ V_{DD} ≤ 5.5 V	0.48		32	μs
		system clock		4.0 V ≤ V_{DD} < 4.5 V	0.95		32	μs
		(MCS = 1 Note 2)	$f_{XX} = f_X/3$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.95		32	μs
			$f_{XX} = 2f_X/9$	4.0 V ≤ V_{DD} ≤ 5.5 V	1.43		32	μs
			$f_{XX} = f_X$	4.5 V ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
				2.7 V ≤ V_{DD} < 4.5 V	0.8		32	μs
		Operating on subsystem clock			114	122	125	μs
TI00 input	t_{TIH00},	3.5 V ≤ V_{DD} ≤ 5.5 V			$2/f_{sam}+0.1$ Note3			μs
high-/low-level width	t_{TIL00}	2.7 V ≤ V_{DD} < 3.5 V			$2/f_{sam}+0.2$ Note3			μs
TI01 input high-/low-level width	t_{TIH01}, t_{TIL01}				10			μs
TI1, TI2 input	t_{TI1}	4.5 V ≤ V_{DD} ≤ 5.5 V			0		4	MHz
frequency					0		275	kHz
TI1, TI2 input	t_{TIH1},	4.5 V ≤ V_{DD} ≤ 5.5 V			100			ns
high-/low-level width	t_{TIL1}				1.8			μs
Interrupt input	t_{INTH},	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}+0.1$ Note3			μs
high-/low-level width	t_{INTL}		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}+0.2$ Note3			μs
		INTP1 to INTP6			10			μs
		KR0 to KR7			10			μs
$\overline{RESET}$ low-level width	t_{RST}				10			μs

Notes 1. When oscillation mode selection register is set to 00H.

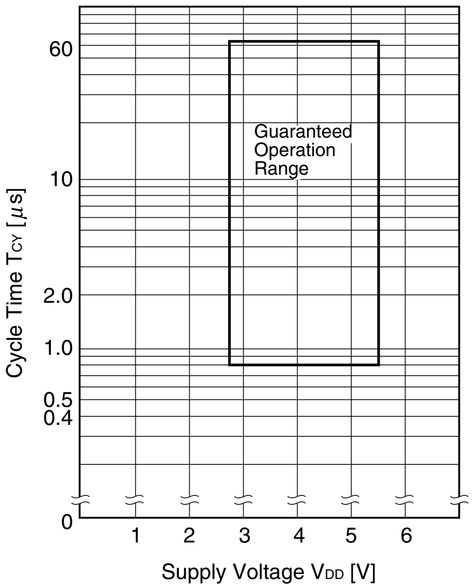
2. When oscillation mode selection register is set to 01H.

3. f_{sam} can be selected as $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, or $f_{XX}/128$ by bits 0 and 1 (SCS0 and SCS1) of the sampling clock selection register (N = 0 to 4).

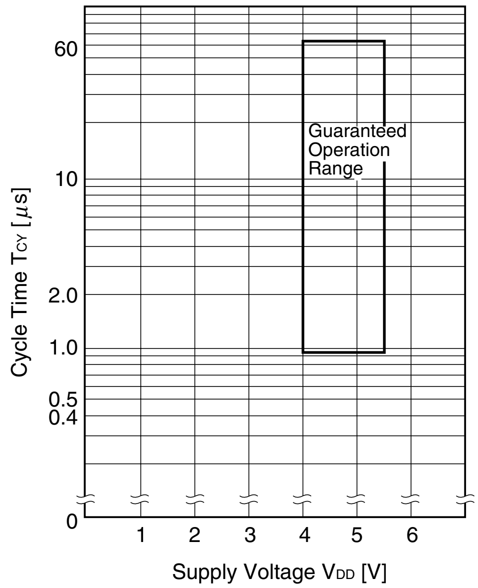
Remarks 1. f_{XX} : Main system clock frequency (f_X or $f_X/2$)

2. f_X : Main system clock oscillatior frequency

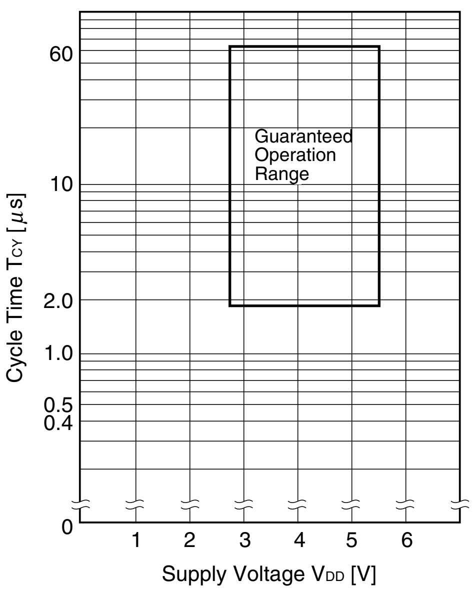
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 0, MCS = 0) Operation)



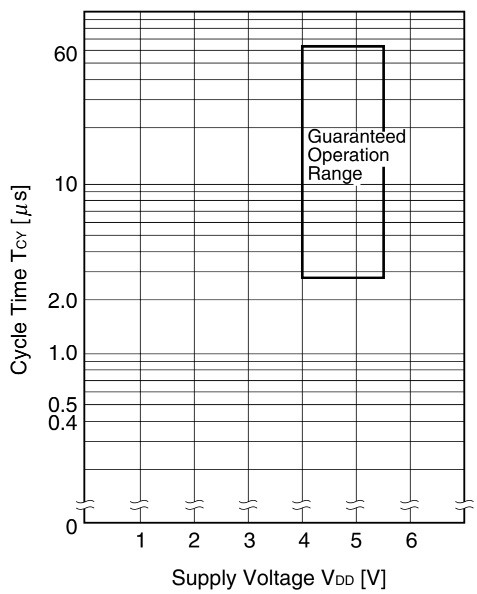
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 0, MCS = 0) Operation)



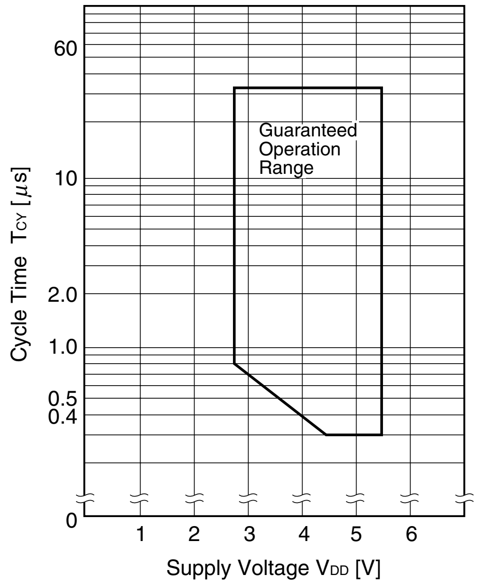
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 1, MCS = 0) Operation)



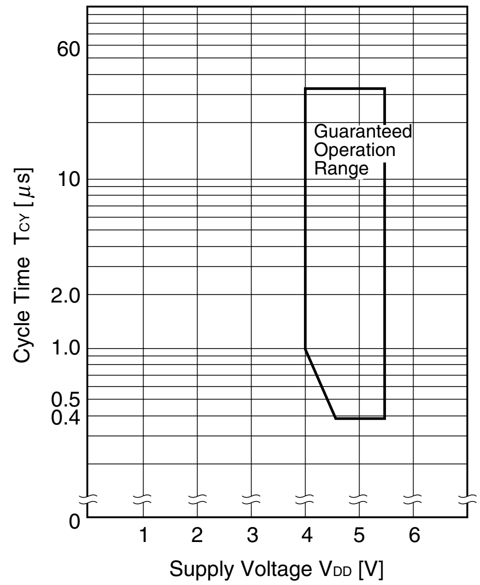
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 1, MCS = 0) Operation)



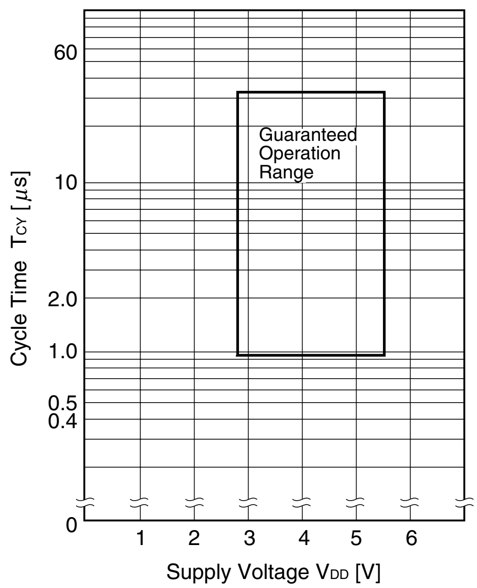
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 0, MCS = 1) Operation)



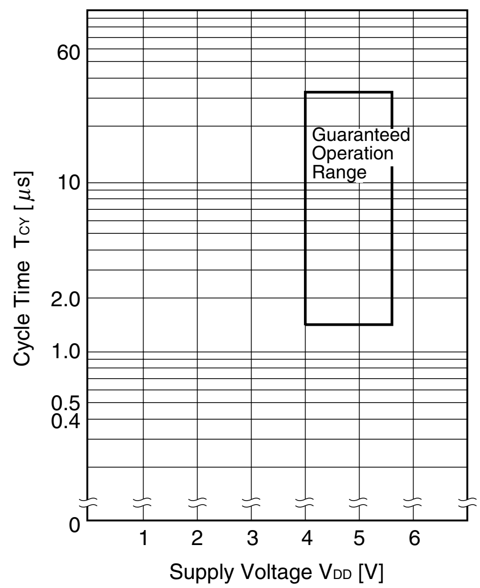
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 0, MCS = 1) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 1, MCS = 1) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 1, MCS = 1) Operation)



(2) Read/Write Operations

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ –50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ –50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85+2n)t_{CY}$–80	ns
	t_{ADD2}			$(4+2n)t_{CY}$–100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			$(2+2n)t_{CY}$–100	ns
	t_{RDD2}			$(2.85+2n)t_{CY}$–100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2+2n)t_{CY}$–60		ns
	t_{RDL2}		$(2.85+2n)t_{CY}$–60		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			$0.85t_{CY}$ –50	ns
	t_{RDWT2}			$2t_{CY}$ –60	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			$2t_{CY}$ –60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15+2n)t_{CY}$	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85+2n)t_{CY}$–100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.85+2n)t_{CY}$–60		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY}$+20		ns
ASTB↑delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		$0.85t_{CY}$–10	$1.15t_{CY}$+20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		$0.85t_{CY}$–50	$1.15t_{CY}$+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}$+40	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		$1.15t_{CY}$+40	$3.15t_{CY}$+40	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		$1.15t_{CY}$+30	$3.15t_{CY}$+30	ns

Remarks
1. MCS: Bit 0 of the oscillation mode selection register
2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register
3. $t_{CY} = T_{CY}/4$
4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} –80		ns
Address setup time	t_{ADS}		t_{CY} –80		ns
Address hold time	t_{ADH}		0.4t_{CY} –10		ns
Data input time from address	t_{ADD1}			(3+2n)t_{CY}–160	ns
	t_{ADD2}			(4+2n)t_{CY}–200	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(1.4+2n)t_{CY}–70	ns
	t_{RDD2}			(2.4+2n)t_{CY}–70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4+2n)t_{CY}–20		ns
	t_{RDL2}		(2.4+2n)t_{CY}–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			t_{CY} –100	ns
	t_{RDWT2}			2t_{CY} –100	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			2t_{CY} –100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1+2n)t_{CY}	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.4+2n)t_{CY}–60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		(2.4+2n)t_{CY}–20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		0.4t_{CY}–30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		1.4t_{CY}-30		ns
ASTB↑delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}–10	t_{CY}+20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}–50	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		0.4t_{CY}–20		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		0	60	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		t_{CY}	t_{CY}+60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		0.6t_{CY}+180	2.6t_{CY}+180	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		0.6t_{CY}+120	2.6t_{CY}+120	ns

Remarks
1. MCS: Bit 0 of the oscillation mode selection register
2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register
3. $t_{CY} = T_{CY}/4$
4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1},	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2-50			ns
	t_{KL1}		t_{KCY1}/2-100			ns
SI0 setup time (vs. $\overline{SCK0}$↑)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (vs. $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100pF Note			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL2}		800			ns
SI0 setup time (vs. $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (vs. $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100pF Note			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{\text{SCK0}}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 5.5 V	t_{KCY3}/2-50			ns
			t_{KCY3}/2-100			ns
SB0, SB1 setup time (vs. $\overline{\text{SCK0}}$↑)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V	100			ns
			300			ns
SB0, SB1 hold time (vs. $\overline{\text{SCK0}}$↑)	t_{KSI3}		t_{KCY3}/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO3}	R = 1kΩ, C = 100pF$^{\text{Note}}$; V_{DD} = 4.5 to 5.5 V	0		250	ns
		R = 1kΩ, C = 100pF$^{\text{Note}}$	0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}$↑	t_{KSB}		t_{KCY3}			ns
$\overline{\text{SCK0}}$↓ from SB0, SB1↓	t_{SBK}		t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY3}			ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{\text{SCK0}}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 5.5 V	400			ns
			1600			ns
SB0, SB1 setup time (vs. $\overline{\text{SCK0}}$↑)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V	100			ns
			300			ns
SB0, SB1 hold time (vs. $\overline{\text{SCK0}}$↑)	t_{KSI4}		t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO4}	R = 1kΩ, C = 100pF$^{\text{Note}}$; V_{DD} = 4.5 to 5.5 V	0		300	ns
		R = 1kΩ, C = 100pF$^{\text{Note}}$	0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}$↑	t_{KSB}		t_{KCY4}			ns
$\overline{\text{SCK0}}$↓ from SB0, SB1↓	t_{SBK}		t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY4}			ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1kΩ, C = 100pF[Note]	V_{DD} = 4.5 to 5.5 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}			t_{KCY5}/2-160			ns
$\overline{SCK0}$ low-level width	t_{KL5}			t_{KCY5}/2-50			ns
SB0, SB1 setup time (vs. $\overline{SCK0}$↑)	t_{SIK5}		V_{DD} = 4.5 to 5.5 V	300			ns
				350			ns
SB0, SB1 hold time (vs. $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0 and SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 5.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}		650			ns
$\overline{SCK0}$ low-level width	t_{KL6}		800			ns
SB0, SB1 setup time (vs. $\overline{SCK0}$↑)	t_{SIK6}		100			ns
SB0, SB1 hold time (vs. $\overline{SCK0}$↑)	t_{KSI6}		t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1kΩ, C = 100pF[Note]	0		300	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the $\overline{SCK0}$, SB0 and SB1 output line load resistance and load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7},	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2-50			ns
	t_{KL7}		t_{KCY7}/2-100			ns
SI1 setup time (vs. $\overline{SCK1}$↑)	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (vs. $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100pF Note			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL8}		800			ns
SI1 setup time (vs. $\overline{SCK1}$↑)	t_{SIK8}		100			ns
SI1 hold time (vs. $\overline{SCK1}$↑)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100pF Note			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(iii) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V		800			ns
				1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V		t_{KCY9}/2-50			ns
				t_{KCY9}/2-100			ns
SI1 setup time (vs. $\overline{SCK1}$↑)	t_{SIK9}	V_{DD} = 4.5 to 5.5 V		100			ns
				150			ns
SI1 hold time (vs. $\overline{SCK1}$↑)	t_{KSI9}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF Note	V_{DD} = 4.5 to 5.5 V			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}			t_{KCY9}/2-100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}			t_{KCY9}-30		t_{KCY9}+30	ns
Busy signal setup time (vs. busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (vs. busy signal detection timing)	t_{BYH}	V_{DD} = 4.5 to 5.5 V		100			ns
				150			ns
$\overline{SCK1}$↓ from busy inactivation	t_{SPS}					2t_{KCY9}	ns

Note C is the SO1 output line load capacitance.

(iv) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI1 setup time (vs. $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (vs. $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11},	V_{DD} = 4.5 to 5.5 V	t_{KCY11}/2-50			ns
	t_{KL11}		t_{KCY11}/2-100			ns
SI2 setup time (vs. $\overline{SCK2}$↑)	t_{SIK11}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI2 hold time (vs. $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100pF **Note**			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL12}		800			ns
SI2 setup time (vs. $\overline{SCK2}$↑)	t_{SIK12}		100			ns
SI2 hold time (vs. $\overline{SCK2}$↑)	t_{KSI12}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100pF **Note**			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO2 output line load capacitance.

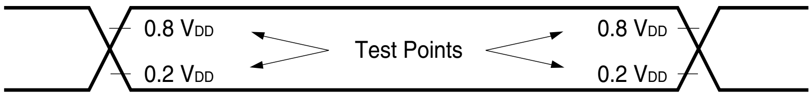
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V			78125	bps
					39063	bps

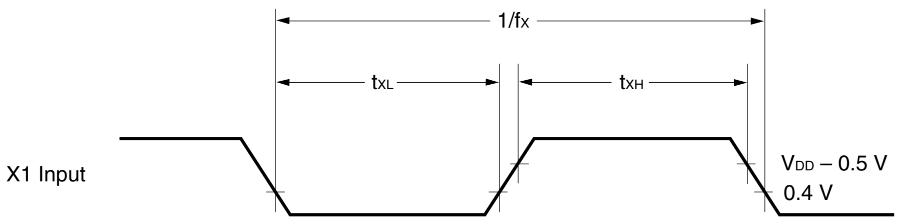
(iv) UART mode (External clock input)

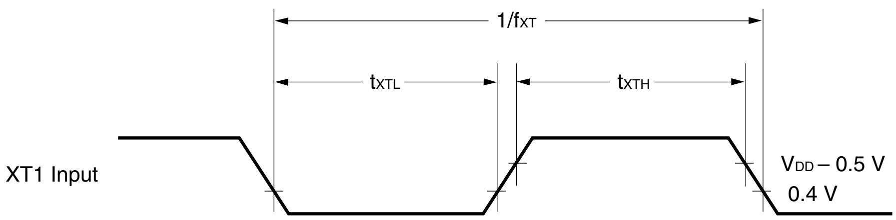
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V_{DD} = 4.5 to 5.5 V			39063	bps
					19531	bps
$\overline{SCK}$ rise, fall time	t_{R13}, t_{F13}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

AC Timing Test Point (Excluding X1, XT1 Input)

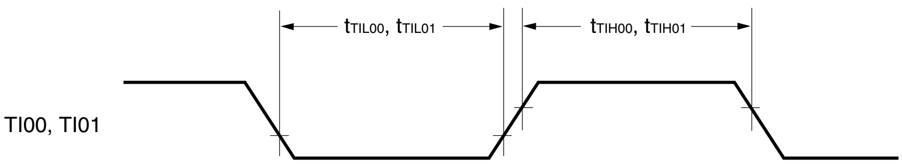


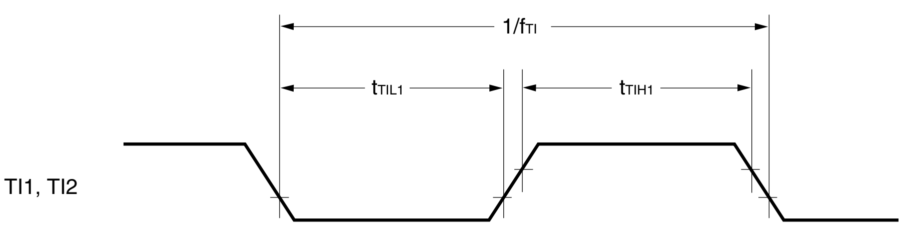
Clock Timing





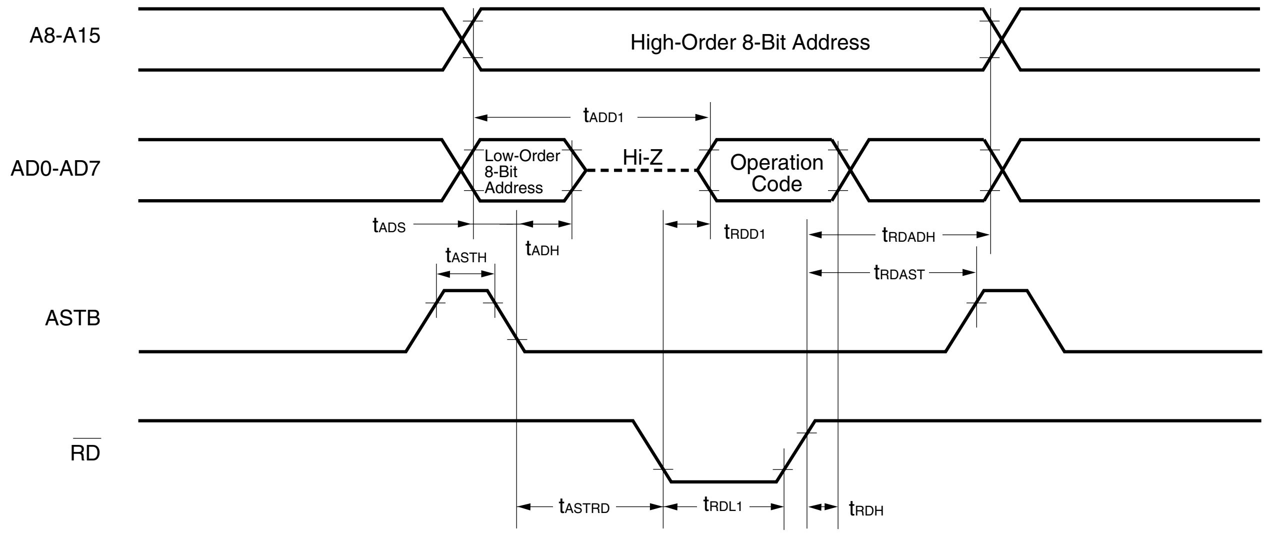
TI Timing



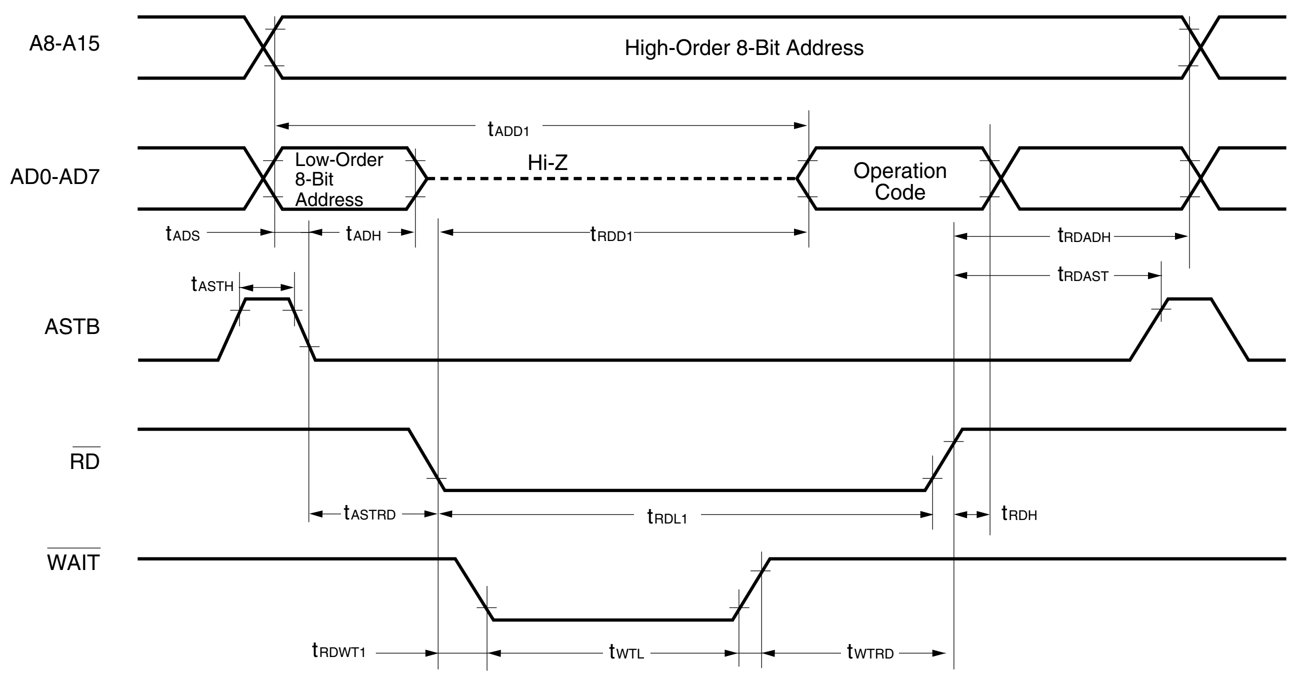


Read/Write Operations

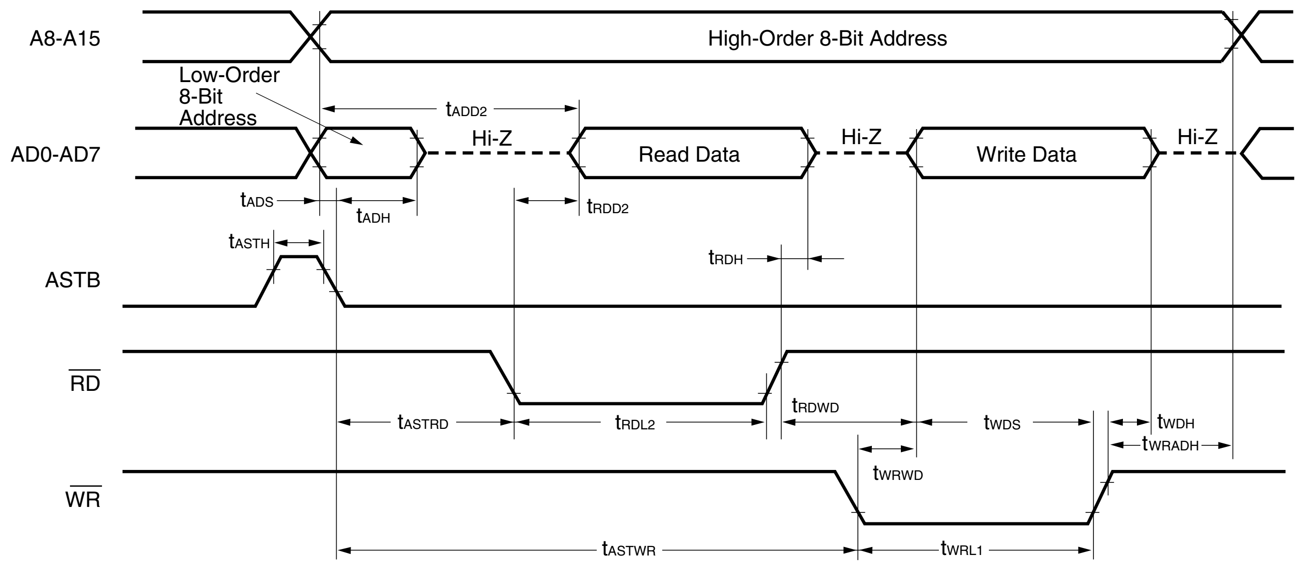
External fetch (no wait):



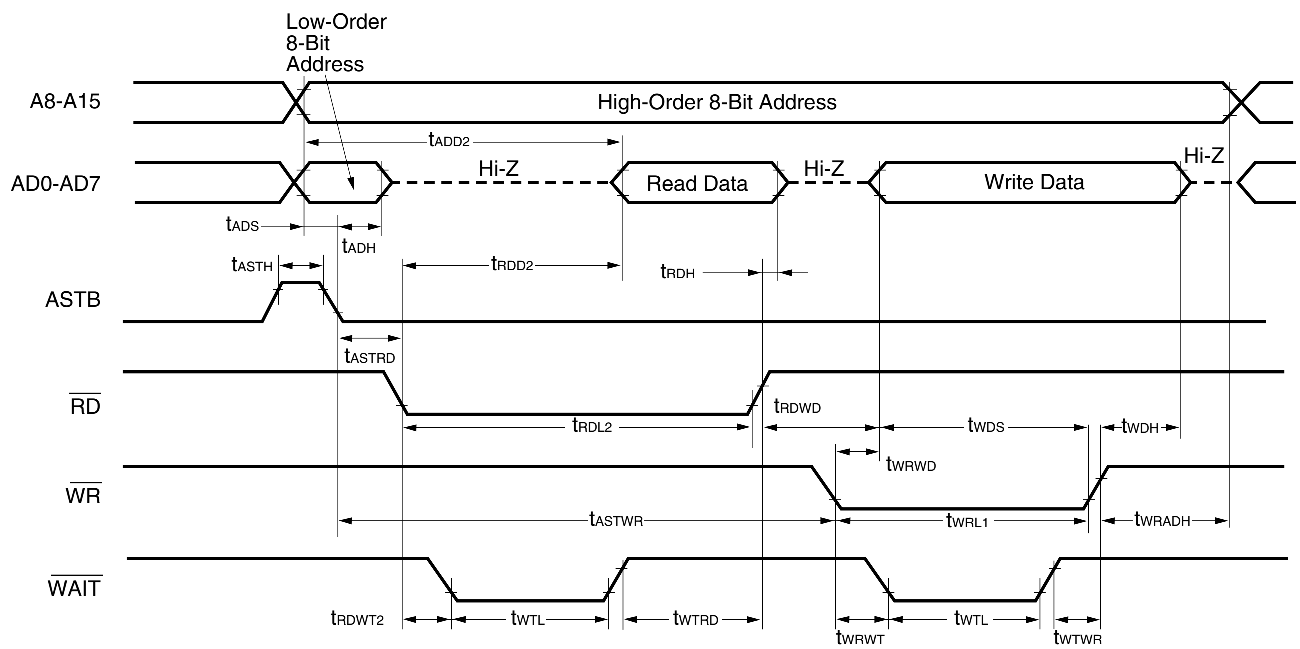
External fetch (wait insertion):



External data access (no wait):

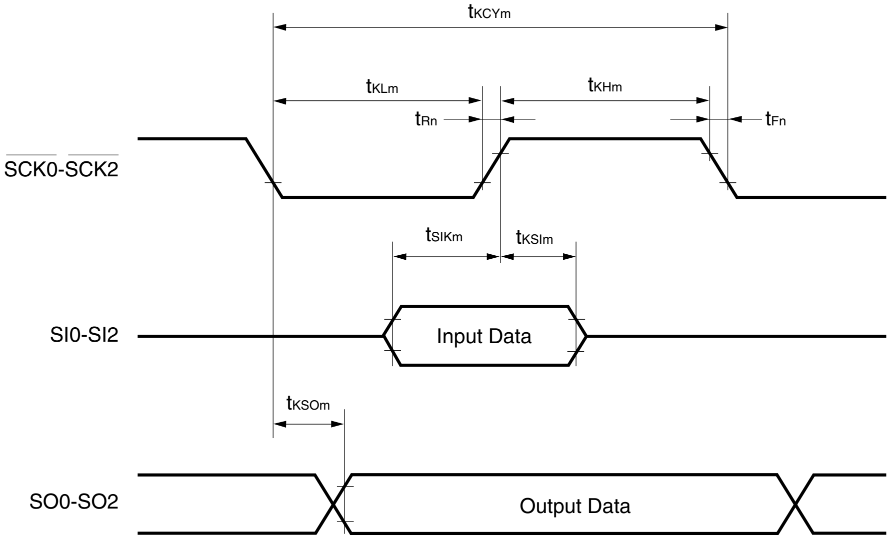


External data access (wait insertion):



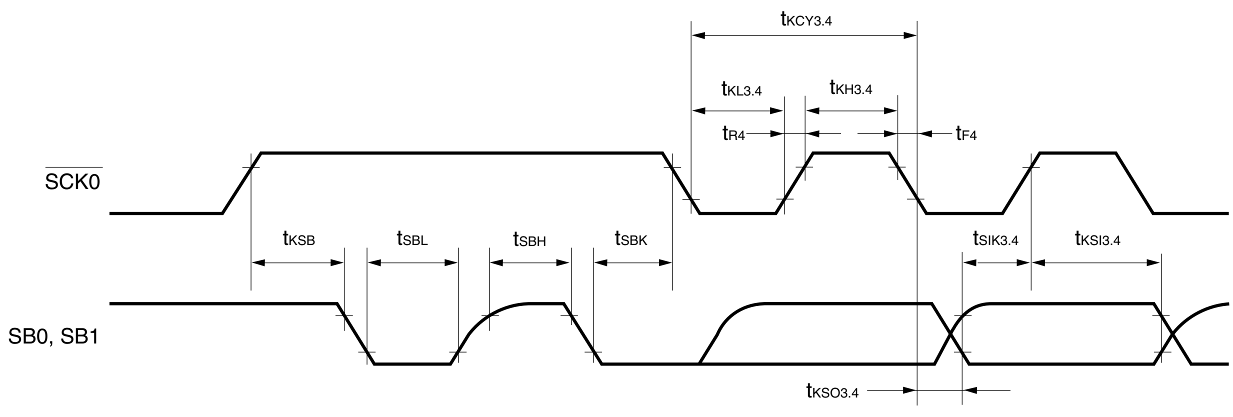
Serial Transfer Timing

3-wire serial I/O mode:

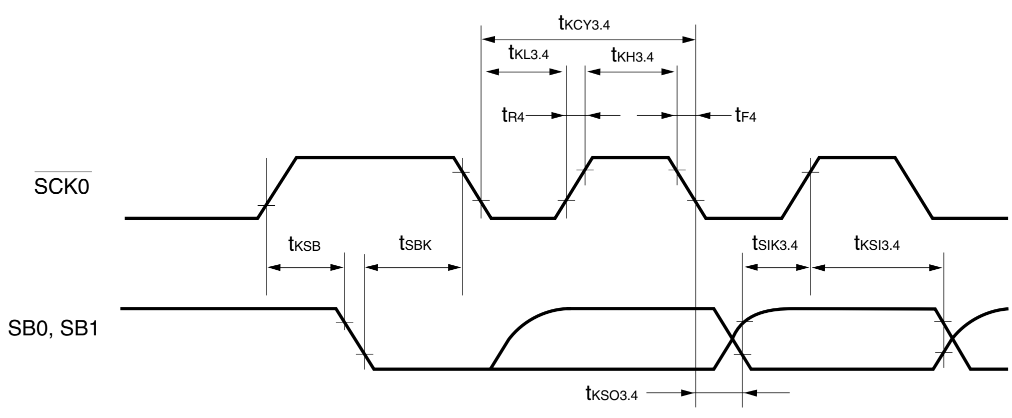


m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

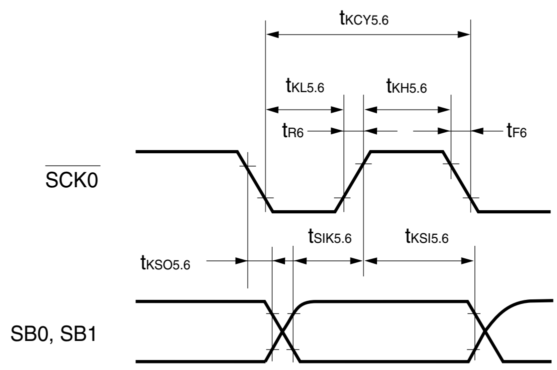
SBI mode (bus release signal transfer):



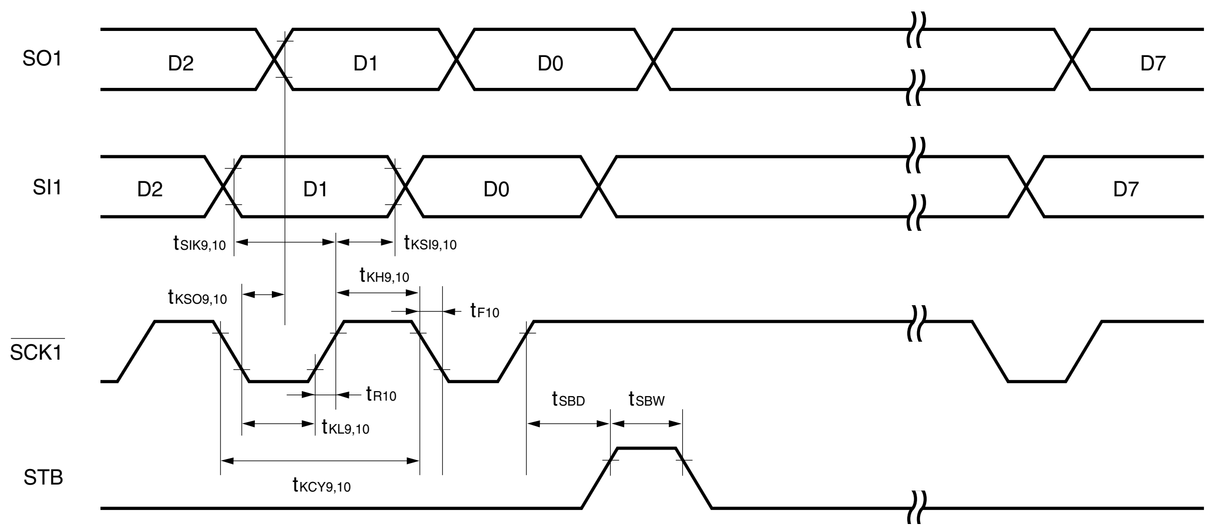
SBI mode (command signal transfer):



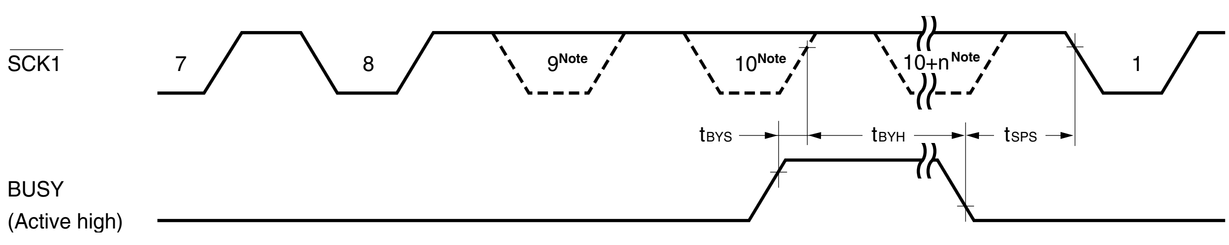
2-wire serial I/O mode:



Automatic transmission/reception function 3-wire serial I/O mode:

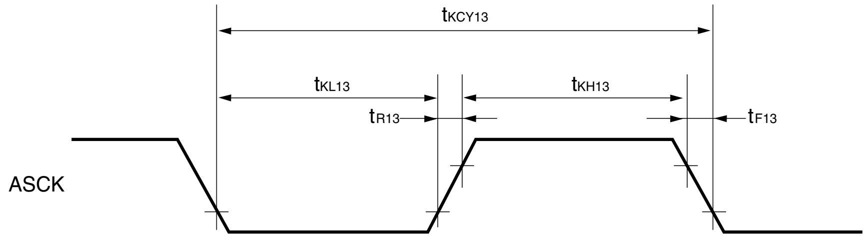


Automatic transmission/reception function 3-wire serial I/O mode (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external Clock Input):



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error[Note]		IEAD = 00H				±1.8	% FSR
		IEAD = 01H	V_{DD} = 4.5 to 5.5 V		±2.2	±3.4	% FSR
					±2.6	±3.8	% FSR
Conversion time	t_{CONV}			19.1		200	μs
Sampling time	t_{SAMP}			12/f_{XX}			μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}			2.7		AV_{DD}	V
AV_{REF0}-AV_{SS} resistance	R_{AIREF0}			4	14		kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value (% FSR).

Remarks **1.** f_{XX} : Main system clock frequency (f_X or f_X/2)

2. f_X : Main system clock oscillatior frequency

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ [Note1]				1.2	%
		R = 4 MΩ [Note1]				0.8	%
		R = 10 MΩ [Note1]				0.6	%
Setting time		C = 30 pF[Note 1]	AV_{REF} = 4.5 to 5.5 V			10	μs
						15	μs
Ouput resistor	R_{O0}	DACS0 = 55H			10		kΩ
	R_{O1}	DACS1 = 55H			10		kΩ
Analog reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	AI_{REF1}	**Note2**				1.5	mA

Notes **1.** R and C are the D/A converter output pin load resistance and load capacitance.

2. Value for one D/A converter channel.

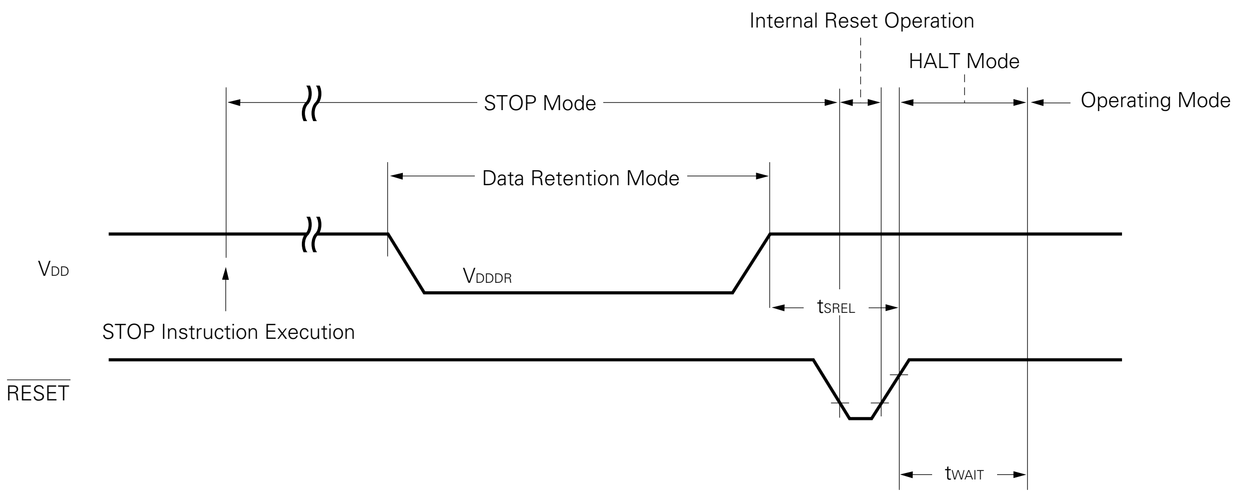
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, feedback resister disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		**Note**		ms

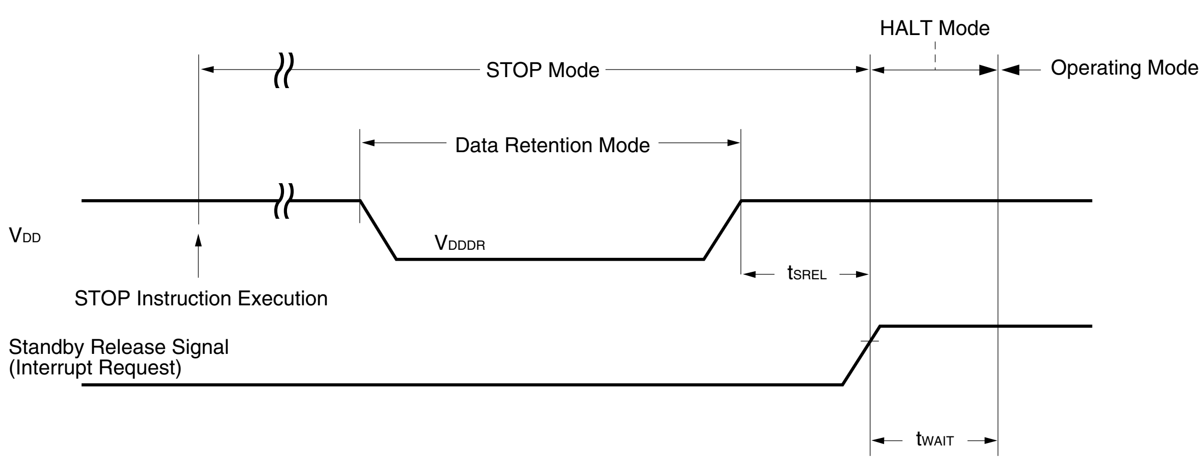
Note $2^{12}/f_{XX}$, or $2^{14}/f_{XX}$ through $2^{17}f_{XX}$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register.

Remark f_{XX} : Main system clock frequency
f_X : Main system clock oscillatior frequency

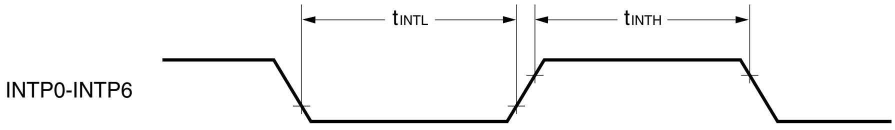
Data Retention Timing (STOP mode release by $\overline{RESET}$)



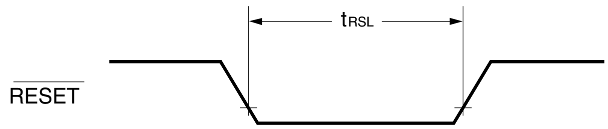
Data Retention Timing (STOP mode release by standby release signal: interrupt signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



IEBus Controller Characteristics (T_A = –40 to +85˚C, V_{DD} = 5 V ± 10%)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
IEBus controller system clock frequency	fs	When using mode 0, 1[Note 1]		5.91	6.00	6.09	MHz
				6.20	6.29	6.39	MHz
		When using mode 2		5.97	6.00	6.03	MHz
				6.26	6.29	6.32	MHz
Driver delay time ($\overline{\text{TX}}$ output → bus line)		C = 50 pF[Note 2]	fs = 6.00 MHz			1.6	μs
			fs = 6.29 MHz			1.5	μs
Receiver delay time (Bus line → $\overline{\text{RX}}$ input)		fs = 6.00 MHz				0.75	μs
		fs = 6.29 MHz				0.7	μs
Propagation delay time on the bus		fs = 6.00 MHz				0.9	μs
		fs = 6.29 MHz				0.85	μs

Notes **1.** For the values in the second row, the IEBus standards are not satisfied.

2. C is the $\overline{\text{TX}}$ output line load capacitance.

PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage low	V_{IL}		0		0.3 V_{DD}	V
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	–10		+10	μA
V_{PP} supply voltage	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	PGM = V_{IL}			50	mA
V_{DD} supply current	I_{DD}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage low	V_{IL}		0		0.3 V_{DD}	V
Output voltage high	V_{OH1}	I_{OH} = –1 mA	V_{DD} –1.0			V
	V_{OH2}	I_{OH} = –100 μA	V_{DD} –0.5			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	–10		+10	μA
Output leakage current	I_{LO}	$0 \leq V_{OUT} \leq V_{DD}$, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}		V_{DD} –0.6	V_{DD}	V_{DD} +0.6	V
V_{DD} supply voltage	V_{DD}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (vs. $\overline{OE}$↓)	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}		2			μs
CE setup time (vs. $\overline{OE}$↓)	t_{CES}		2			μs
Input data setup time (vs. $\overline{OE}$↓)	t_{DS}		2			μs
Address hold time (vs. $\overline{OE}$↑)	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time (vs. $\overline{OE}$↑)	t_{DH}		2			μs
Data output float delay time from $\overline{OE}$↑	t_{DF}		0		250	ns
V_{PP} setup time (vs. $\overline{OE}$↓)	t_{VPS}		1.0			ms
V_{DD} setup time (vs. $\overline{OE}$↓)	t_{VDS}		1.0			ms
Program pulse width	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}$↓	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (vs. $\overline{PGM}$↓)	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}		2			μs
$\overline{CE}$ setup time (vs. $\overline{PGM}$↓)	t_{CES}		2			μs
Input data setup time (vs. $\overline{PGM}$↓)	t_{DS}		2			μs
Address hold time (vs. $\overline{OE}$↑)	t_{AH}		2			μs
Input data hold time (vs. $\overline{PGM}$↑)	t_{DH}		2			μs
Data output float delay time from $\overline{OE}$↑	t_{DF}		0		250	ns
V_{PP} setup time (vs. $\overline{PGM}$↓)	t_{VPS}		1.0			ms
V_{DD} setup time (vs. $\overline{PGM}$↓)	t_{VDS}		1.0			ms
Program pulse width	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}$↓	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

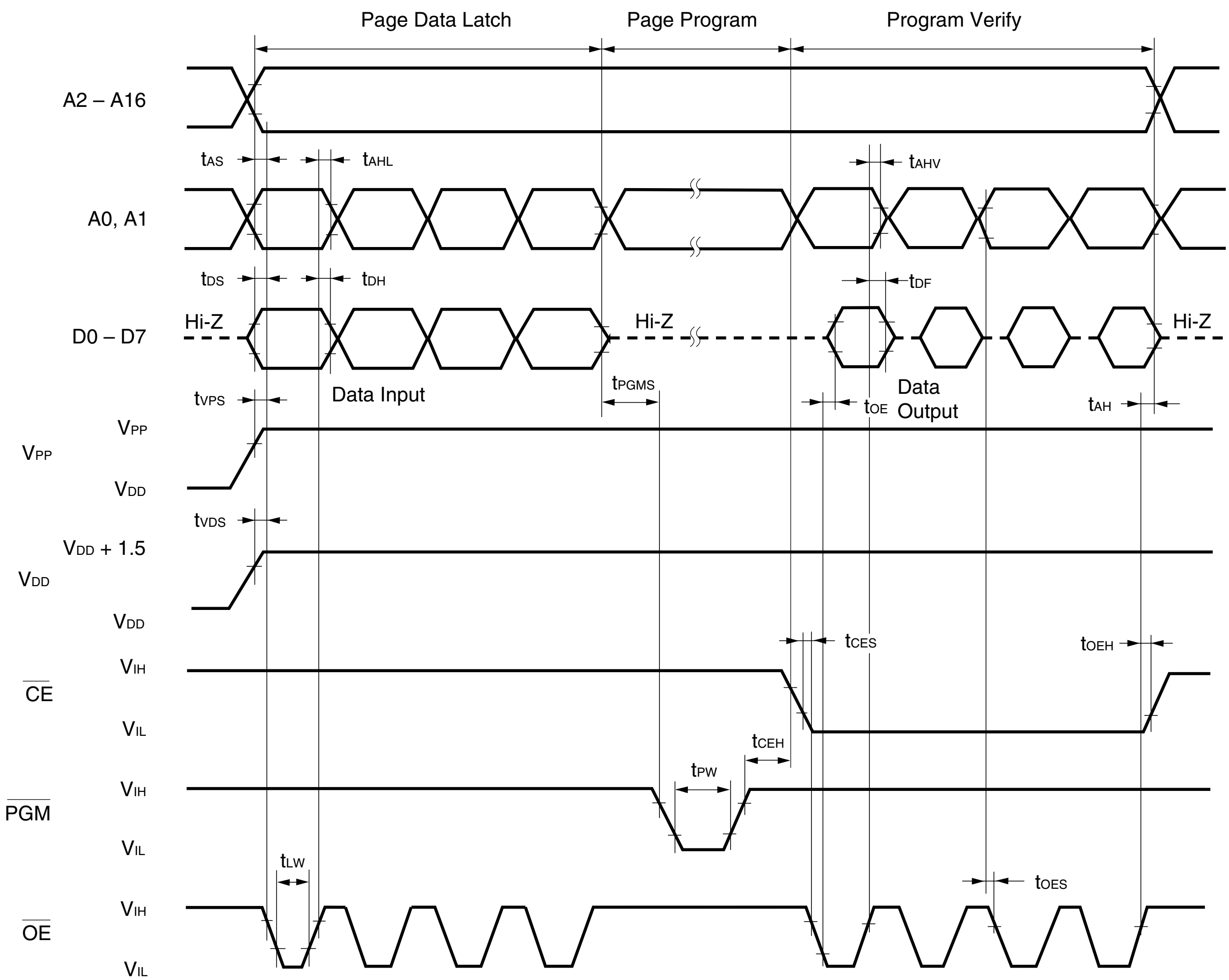
(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

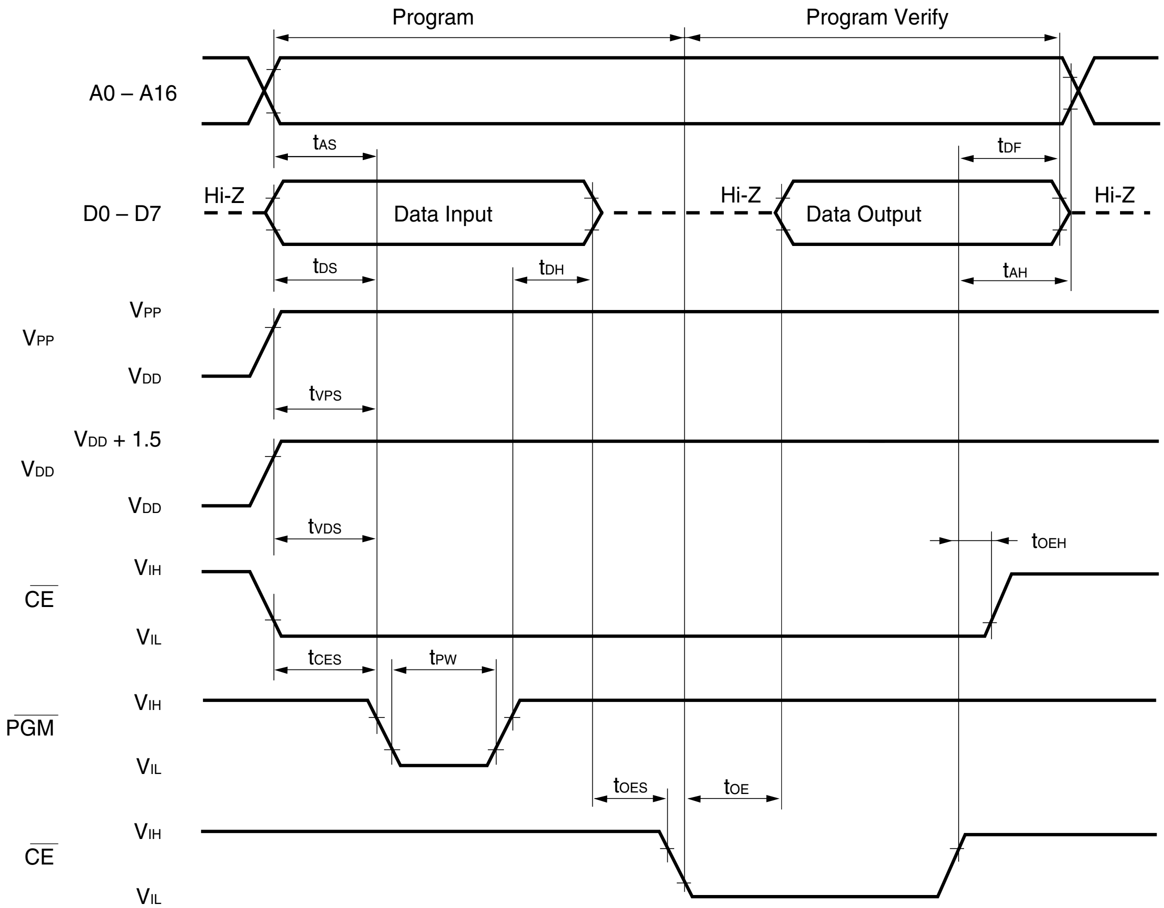
(3) PROM Programming Mode Setting (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programing mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

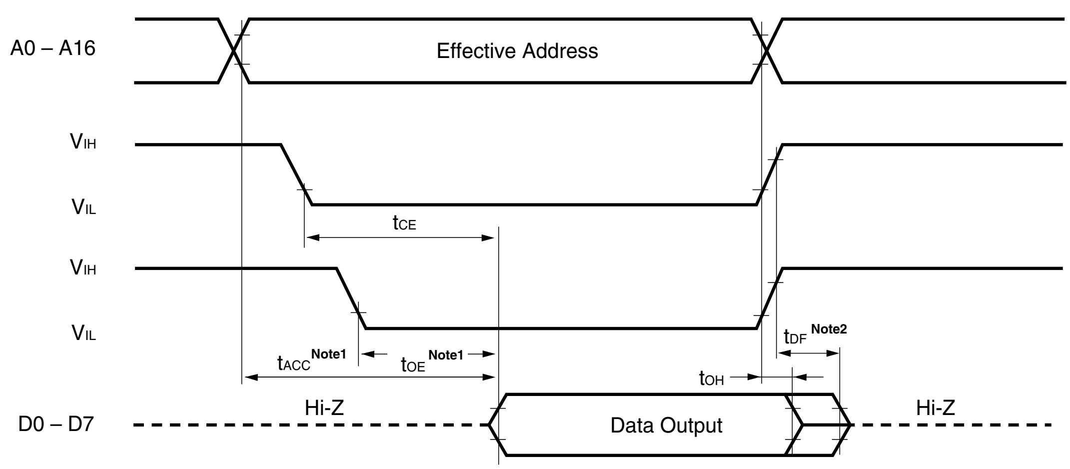


Cautions 1. V_{DD} shonld be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} shonld not exceed +13.5 V including overshoot.

3. Disconnection during application of ±12.5V to V_{PP} may have an adverse effect on reliability.

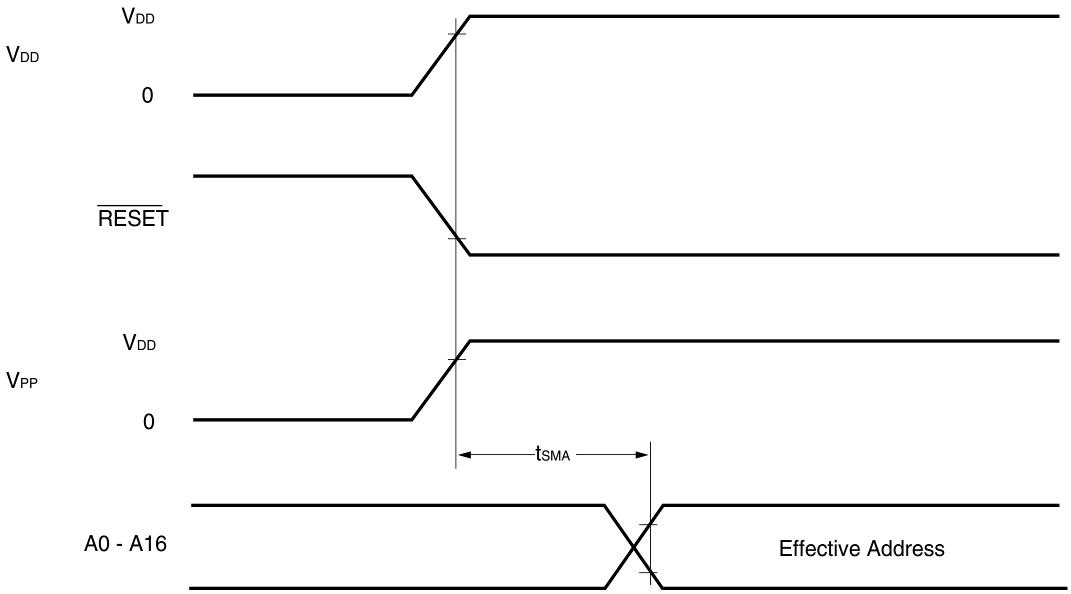
PROM Read Mode Timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maxmum of t_{ACC} – t_{OE}.

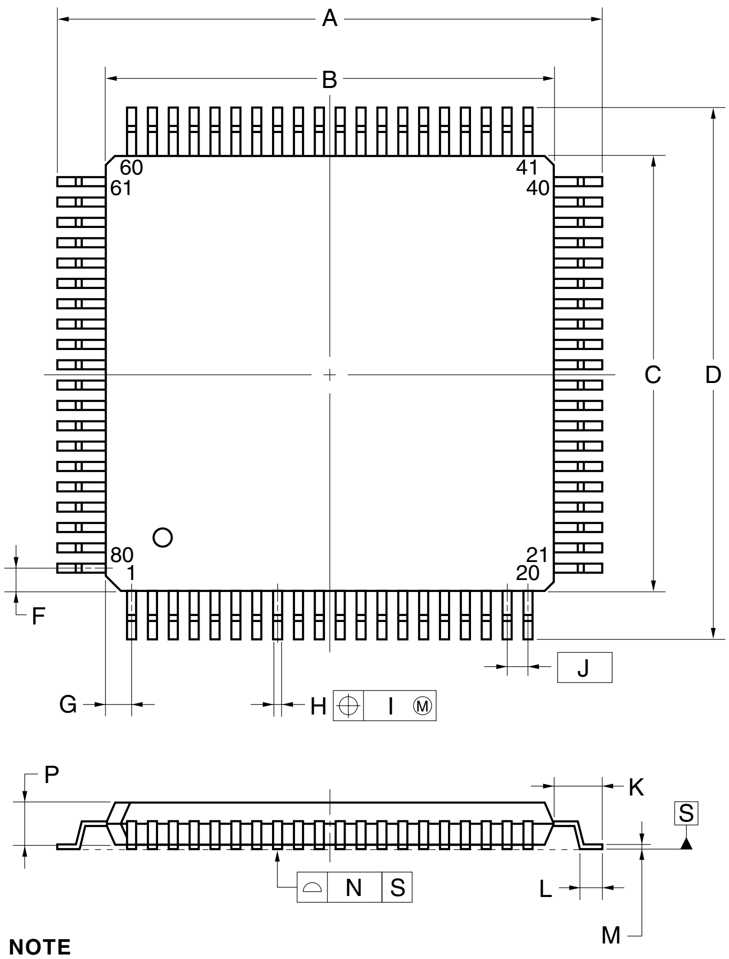
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

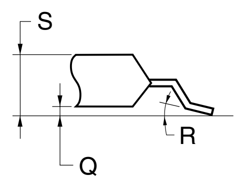
PROM Programming Mode Setting Timing



8. PACKAGE DRAWINGS

★ 80-PIN PLASTIC QFP (14x14)





NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3°^{+7°}_{-3°}$
S	1.70 MAX.

P80GC-65-8BT-1

★ 9. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, please contact your NEC sales representative.

Table 9-1. Surface Mount Type Soldering Conditions

μPD78P098AGC-8BT : 80-pin plastic QFP (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: 2 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: 2 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD78P098A. Also refer to **(6) Notes on using development tools**.

★ **(1) Software package**

SP78K0	Software package common to 78K/0 Series

(2) Language processor software

RA78K0	Common assembler package for 78K/0 series products
CC78K0	Common C compiler package for 78K/0 series products
DF78098	Device file for μPD78098 subseries
CC78K0-L	Common C compiler library source file for 78K/0 series products

(3) PROM writing tools

PG-1500	PROM programmer
PA-78P054GC	Programmer adapter connected to PG-1500
PG-1500 controller	Control program for PG-1500

★ **(4) Debugging tools**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Adapter required when IBM PC/AT compatible is used as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when PC incorporating PCI bus is used as host machine
IE-70000-R-SV3	Interface adapter and cable required when EWS is used as host machine
IE-78098-R-EM	Emulation board to emulate the μPD78098 Subseries
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the EP-78230GC-R and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF78098	Device file for μPD78098 Subseries

(5) Real-time OS

RX78K/0	Real-time OS for 78K/0 series
MX78K0	OS for 78K/0 series

★ **(6) Notes on using development tools**

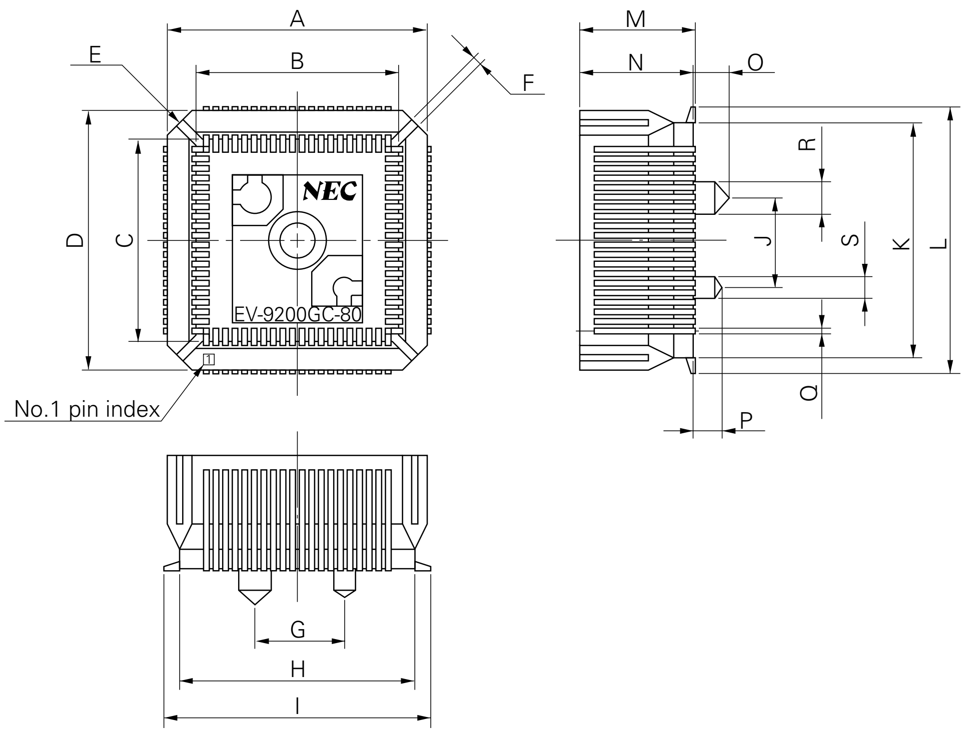
- The ID78K0, and SM78K0 are used in combination with the DF78098.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF78098.
- For third-party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E).**
- The host machines and OS suitable for each software are as follows:

Software \ Host Machine [OS]	PC PC-9800 series [Japanese Windows™] IBM PC/AT compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0	√	—
SM78K0	√	—
RX78K0	√Note	√
MX78K0	√Note	√

Note DOS-based software

DIMENSIONS AND RECOMMENDED MOUNTING PATTERN OF CONVERSION SOCKET

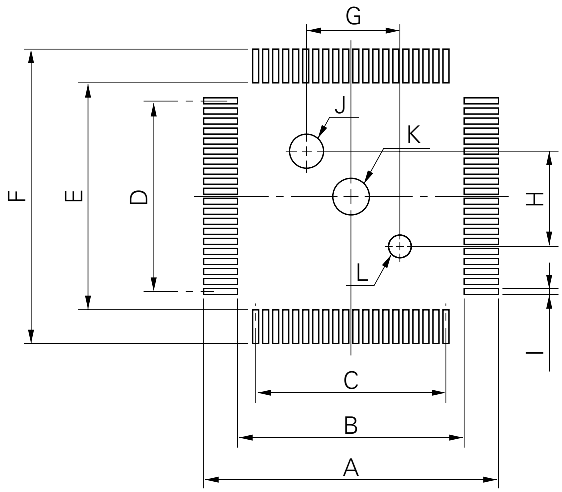
Figure A-1. Dimensions of EV-9200GC-80 (reference)



EV-9200GC-80-G0

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Mounting Pattern of EV-9200GC-80 (reference)



EV-9200GC-80-P0

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0±0.05	$0.236^{+0.003}_{-0.002}$
H	6.0±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

★ APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD78098 Subseries User's Manual	IEU-1381
μPD78094, 78095, 78096, 78098A Data Sheet	U10146E
μPD78P098A Data Sheet	This manual
78K/0 Series User's Manual - Instruction	U12326E
78K/0 Series Application Note - Basic(III)	U10182E

Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Parts User Open Interface Specification	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E
RX78K0 Real-time OS	Fundamentals	U11537E
	Installation	U11536E
MX78K0 Embedded OS	Fundamental	U12257E

Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78001-R-A In-Circuit Emulator	U14142E
IE-78098-R-EM Emulation Board	EEU-1473

Documents Related to PROM Writing (User's Manuals)

Document Name		Document No.
PG-1500 PROM Programmer		U11940E
PG-1500 Controller	PC-9800 Series (MS-DOS)-Based	EEU-1291
	IBM PC Series (PC DOS)-Based	U10540E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products & Package -	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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