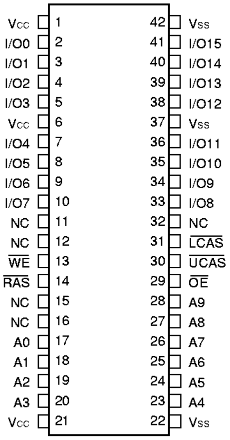
1Mx16 CMOS EDO Dynamic RAM 3.3V *PRELIMINARY**

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-9}	Address Inputs
I/O_{0-15}	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
V_{CC}	Power Supply
V_{SS}	Ground
NC	Not Connected

PLASTIC PLUS™ FEATURES

- Fast Access Time (t_{RAC}): 70ns
- Power Supply: 3.3V ± 0.3V
- Packaging
  - 42 Lead Plastic Surface-Mount SOJ (TJ)
- Industrial and Military Temperature Ranges
- Extended Data Out (EDO) Page Mode Access Cycle.
- TTL-Compatible Inputs and Outputs
- JEDEC and Industry-Standard x16 Timing, Functions, Pinout and Package.
- RAS-Only Refresh
- xCAS Before $\overline{RAS}$ Refresh
- Hidden Refresh
- Byte Write Access Cycle
- 1024 Cycle Refresh in 16ms

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C
Short Circuit Output Current	I_{OS}		50	mA
Power Dissipation	P_T		1	W
Supply Voltage Range*	V_{CC}	-1.0	4.6	V
Voltage Range on any Pin*	V_T	-1.0	5.5	V

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposed to absolute-maximum-rated conditions for extended periods may affect device reliability.

* All voltage values are with respect to Vss.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.0	Vcc +1	V
Input Low Voltage*	V_{IL}	-1.0	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

* The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Max	Unit
A_{0-9} Input Capacitance	$C_{I(A)}$	5	pF
$\overline{RAS}$ and $\overline{CAS}$ Input Capacitance	$C_{I(RC)}$	7	pF
$\overline{OE}$ Input Capacitance	$C_{I(OE)}$	7	pF
$\overline{WE}$ Input Capacitance	$C_{I(WE)}$	7	pF
I/O Capacitance	C_{IO}	7	pF

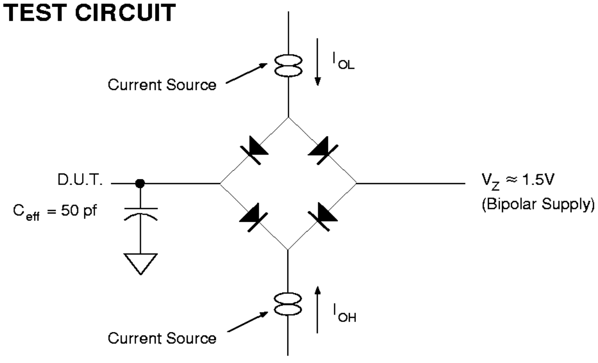
This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V, Vss = 0V, T_A = -55°C to +125°C)

			70		
Parameter	**Test Condition**	**Symbol**	**Min**	**Max**	**Units**
High Level Output Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V
Low Level Output Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V
Input Current (Leakage)	V_I = 0V to Vcc max, Vcc = 3.6V All others = 0V	I_I		10	µA
Output current (Leakage)	VO = 0V to Vcc, CAS high	I_O		10	µA
Read or Write Cycle Current	minimum cycle	I_{CC1}		190	mA
Standby Current	TTL, $\overline{RAS}$ and $\overline{CAS}$ high	I_{CC2}		2	mA
	CMOS, $\overline{RAS}$ and $\overline{CAS}$ high	I_{CC2}		1	mA
Average Page Current	$\overline{RAS}$ low, $\overline{CAS}$ cycling	I_{CC4}		150	mA

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.

I_{OL} & I_{OH} programmable from 0 to 16mA.

Tester Impedance Z_0 = 75 Ω.

V_Z is typically the midpoint of V_{OH} and V_{OL}.

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

AC CHARACTERISTICS

(Notes: 1, 2, 4-7, 12) (V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		Units
		Min	Max	
Column Address Access Time	t_{AA}		35	ns
Column Address Setup to $\overline{\text{CAS}}$ Precharge	t_{ACH}	15		ns
Column Address Hold Time (Reference to $\overline{\text{RAS}}$)	t_{AR}	50		ns
Column Address Setup Time (20)	t_{ASC}	0		ns
Row Address Setup Time (20)	t_{ASR}	0		ns
Column Address to $\overline{\text{WE}}$ Delay Time (8)	t_{AWD}	60		ns
Access Time from $\overline{\text{CAS}}$ (9,20)	t_{CAC}		20	ns
Column Address Hold Time (20)	t_{CAH}	12		ns
$\overline{\text{CAS}}$ Pulse Width (22)	t_{CAS}	13	10,000	ns
$\overline{\text{CAS}}$ Hold Time (CBR Refresh) (3,21)	t_{CHR}	12		ns
Last CAS going Low to first CAS to return High (24)	t_{CLCH}	10		ns
CAS to Output in Low-Z (21)	t_{CLZ}	0		ns
Data Output hold after next CAS Low	t_{COH}	3		ns
CAS Precharge Time (10,25)	t_{CP}	10		ns
Access Time from CAS Precharge (21)	t_{CPA}		40	ns
CAS to RAS Precharge Time (21)	t_{CRP}	5		ns
$\overline{\text{CAS}}$ Hold Time (21)	t_{CSH}	55		ns
$\overline{\text{CAS}}$ Setup Time (CBR Refresh) (3,20)	t_{CSR}	5		ns
$\overline{\text{CAS}}$ to WE Delay Time (8,20)	t_{CWD}	40		ns
Write Command to CAS Lead Time (21)	t_{CWL}	15		ns
Data-In Hold Time (11,20)	t_{DH}	12		ns
Data-In Setup Time (11,20)	t_{DS}	0		ns
Output Disable	t_{OD}	0	15	ns
Output Enable (12, 20)	t_{OE}		20	ns
OE Hold Time from WE during Read-Modify-Write Cycle (13)	t_{OEH}	12		ns
$\overline{\text{OE}}$ High hold from $\overline{\text{CAS}}$ High (13)	t_{OEHC}	10		ns
$\overline{\text{OE}}$ High Pulse Width	t_{OEP}	10		ns
$\overline{\text{OE}}$ Low to CAS High Setup Time	t_{OES}	5		ns
Output Buffer Turn-Off Delay (15,21)	t_{OFF}	0	15	ns

NOTES: See full list on page 5.

AC CHARACTERISTICS

(Notes: 1, 2, 4-7, 12) (V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-70		Units
		Min	Max	
$\overline{\text{OE}}$ Setup Prior to $\overline{\text{RAS}}$ during Hidden Refresh Cycle (26)	t_{ORD}	0		ns
EDO-Page-Mode Read or Write Cycle Time (26)	t_{PC}	35		ns
EDO-Page-Mode Read-Write Cycle Time (14)	t_{PRWC}	85		ns
Access Time from $\overline{\text{RAS}}$ (16)	t_{RAC}		70	ns
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	12		ns
Row Address Hold Time	t_{RAH}	10		ns
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	70	10,000	ns
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode)	t_{RASP}	70	125,000	ns
$\overline{\text{RAS}}$ Pulse Width during Self Refresh	t_{RASS}	100		µs
Random Read or Write Cycle Time	t_{RC}	130		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time (17,20)	t_{RCD}	14	50	ns
Read Command Hold Time (referenced to $\overline{\text{CAS}}$) (18,23)	t_{RCH}	0		ns
Read Command Setup Time (20)	t_{RCS}	0		ns
Refresh Period (1,024 cycles)	t_{REF}		16	ms
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	50		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	t_{RPC}	5		ns
Read Command Hold Time (referenced to $\overline{\text{RAS}}$) (18)	t_{RRH}	0		ns
$\overline{\text{RAS}}$ Hold Time (27)	t_{RSH}	15		ns
Read Write Cycle Time	t_{RWC}	180		ns
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time (8)	t_{RWD}	90		ns
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	18		ns
Transition Time (rise or fall)	t_T	2	50	ns
Write Command Hold Time (27)	t_{WCH}	12		ns
Write Command Hold Time (referenced to $\overline{\text{RAS}}$)	t_{WCR}	55		ns
$\overline{\text{WE}}$ Command Setup Time (8,20)	t_{WCS}	0		ns
Output Disable Delay from $\overline{\text{WE}}$	t_{WHZ}	0	15	ns
Write Command Pulse Width	t_{WP}	5		ns
$\overline{\text{WE}}$ Pulse to Disable at $\overline{\text{CAS}}$ High	t_{WPZ}	12		ns
$\overline{\text{WE}}$ Hold Time (CBR Refresh)	t_{WRH}	10		ns
$\overline{\text{WE}}$ Hold Time (CBR Refresh)	t_{WRP}	10		ns

NOTES: See full list on next page.

NOTES:

1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
2. An initial pause of 100µs is required after power-up is followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$-only or CBR with $\overline{\text{WE}}$ High), before proper device operation is ensured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
3. Enables on-chip refresh and address counters.
4. AC characteristics assume t_T = 2.5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. In addition to meeting the transition rate between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Measured with a load equivalent to two TTL gates and 100pF; and V_{OL} = 0.8V and V_{OH} = 2V.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to Early Write cycles. t_{RWD}, t_{AWD} and t_{CWD} apply to Read-Modify-Write cycles. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an Early Write cycle and the data output will remain an open circuit throughout the entire cycle. $t_{WCS} < t_{WCS}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a Read-Modify-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the data-out is indeterminate. $\overline{\text{OE}}$ held High and $\overline{\text{WE}}$ taken Low after $\overline{\text{CAS}}$ goes Low results in a Late Write ($\overline{\text{OE}}$-controlled) cycle. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not applicable in a Late Write cycle.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. If $\overline{\text{CAS}}$ is Low at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed High for t_{CP}.
11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in Early Write cycles and $\overline{\text{WE}}$ leading edge in Late Write or Read-Modify-Write cycles.
12. If $\overline{\text{OE}}$ is tied permanently Low, Late Write or Read-Modify-Write operations are not permissible and should not be attempted. Additionally, $\overline{\text{WE}}$ must be pulsed during $\overline{\text{CAS}}$ High time in order to place I/O buffers in High-Z.
13. Late Write and Read-Modify-Write cycle must have both t_{OD} and t_{OEH} met ($\overline{\text{OE}}$ High during Write cycle) in order to ensure that the output buffers will be open during the Write cycle. The I/Os will provide the previously read data if $\overline{\text{CAS}}$ remains Low and $\overline{\text{OE}}$ is taken back Low after t_{OEH} is met. If $\overline{\text{CAS}}$ goes High prior to $\overline{\text{OE}}$ going back Low, theI/Os will remain open.
14. Assumes that $t_{RCD} \geq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs first.
16. The t_{RAD} (max) limit is no longer specified. t_{RAD} (max) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (max) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
17. The t_{RCD} (max) limit is no longer specified. t_{RCD} (max) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (max) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} (min) no longer applied). With or without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
18. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
19. The first x$\overline{\text{CAS}}$ edge to transition Low.
20. Output parameter (I/Ox) is referenced to corresponding $\overline{\text{CAS}}$ input: I/O_{0-7} by $\overline{\text{LCAS}}$ and I/O_{8-15} by $\overline{\text{UCAS}}$.
21. Each x$\overline{\text{CAS}}$ must meet minimum pulse width.
22. The last x$\overline{\text{CAS}}$ edge to transition High.
23. Last falling x$\overline{\text{CAS}}$ edge to first rising x$\overline{\text{CAS}}$ edge.
24. Last rising x$\overline{\text{CAS}}$ edge to first rising x$\overline{\text{CAS}}$ edge.
25. Last rising $\overline{\text{CAS}}$ edge to next cycle's last rising x$\overline{\text{CAS}}$ edge.
26. Last x$\overline{\text{CAS}}$ to go Low.
27. A Hidden Refresh may also be performed after a Write cycle. In this case, $\overline{\text{WE}}$ is Low and $\overline{\text{OE}}$ is High.

GENERAL DESCRIPTION

The 1M x 16 is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x16 configuration. The Meg x 16 has both Byte Write and Word Write access cycles via two CAS pins (LCAS and UCAS).

These function like a single CAS found on other DRAMs in that either LCAS or UCAS will generate an internal CAS.

The CAS function and timing are determined by the first CAS (LCAS or UCAS) to transition Low and the last CAS to transition back High. Using only one of the two signals results in a byte Write cycle. LCAS transitioning Low selects an access cycle for the lower byte (I/O$_{0-7}$), and UCAS transitioning Low selects an access cycle for the upper byte (I/O$_{8-15}$).

Each bit is uniquely addressed through the 20 address bits during Read or Write cycles. These are entered 10 bits (A$_{0-9}$) at a time. RAS is used to latch the first 10 bits and CAS, the latter 10 bits. The CAS function also determines whether the cycle will be a refresh cycle (RAS only) or an active cycle (Read, Write or Read-Write) once RAS goes Low.

The LCAS and UCAS inputs internally generate a CAS signal that functions like the single CAS input on other DRAMs. The key difference is each CAS input (LCAS and UCAS) controls its corresponding eight I/O inputs during Write accesses. LCAS controls I/O$_{0-7}$, and UCAS controls I/O$_{8-15}$. The two CAS controls give the 1M x 16 both Byte Read and Byte Write cycle capabilities.

A logic High on WE dictates Read mode, while a logic Low on WE dictates Write mode. During a Write cycle, data-in (I) is latched by the falling edge of WE or CAS (LCAS or UCAS), whichever occurs last. An Early Write occurs when WE is taken Low prior to either CAS falling. A Late Write or Read-Modify-Write occurs when WE falls after CAS (LCAS or UCAS) was taken Low. During Early Write cycles, the data outputs (O) will remain High-Z, regardless of the state of OE. During Late Write or Read-Modify-Write is attempted while keeping OE Low, no write will occur, and the data outputs will drive read data from the accessed location.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE.

PAGE ACCESS

Page operations allow faster data operations (Read, Write or Read-Modify-Write) within a row address defined page boundary. The Page cycle is always initiated with a row address strobed-in by RAS, followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS Low and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS High terminates the Page Mode of operation.

EDO PAGE MODE

The 1M x 16 provides EDO Page Mode, which is an accelerated Fast Page Mode cycle. The primary advantage of EDO is the availability of data-out even after CAS returns High. EDO provides for CAS precharge time (t$_{CP}$) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline Reads.

Fast Page Mode DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO Page Mode DRAMs operate like Fast Page Mode DRAMs, except data will remain valid or become valid after CAS goes High during Reads, provided RAS and OE are held Low. If OE is pulsed while RAS and CAS are Low, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes High while RAS remains Low, data will transition to and remain High-Z. WE can also perform the function of disabling the output drivers under certain conditions.

BYTE ACCESS CYCLE

The Byte Writes and Byte Reads are determined by the use of LCAS and UCAS. Enabling LCAS selects a lower byte access (I/O$_{0-7}$). Enabling UCAS selects an upper byte access (I/O$_{8-15}$). Enabling both LCAS and UCAS selects a Word Write cycle.

The 1M x 16 may be viewed as two 1M x 8 DRAMs that have common input controls, with the exception of the CAS inputs.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an Early Write on one byte and a Late Write on the other byte are not allowed during the same cycle. However, an Early Write on one byte and a Late Write on the other byte, after a CAS precharge has been satisfied, are permissible.

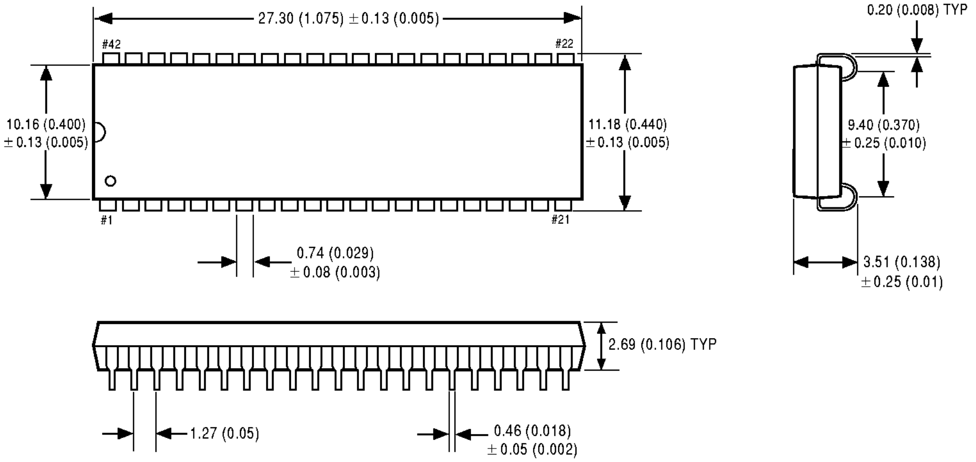
REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (Read, Write) or RAS refresh cycle (RAS-only, CBR or Hidden) so that all 1,024 combinations of RAS addresses are executed within t$_{REF}$ (max), regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic RAS addressing.

STANDBY

Returning RAS and CAS High terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS High time.

PACKAGE DIMENSION: 42 LEAD SOJ, (TJ)



TOLERANCES: ±0.13 (0.005) UNLESS OTHERWISE SPECIFIED
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P D E 1M 16 V X - 70 TJ X

DEVICE GRADE:

M =	Military Temperature	-55°C to +125°C
I =	Industrial Temperature	-40°C to +85°C

PACKAGE:
TJ = 42 Lead Plastic Surface Mount SOJ

ACCESS TIME (ns)

IMPROVEMENT MARK

B = Burn-in
T = Temperature Cycle
C = Burn-in and Temp Cycle

Low Voltage Supply 3.3V ±0.3V

ORGANIZATION, 1M x 16

Blank = Fast Page Mode (FPM)
E = Extended Data Out Mode (EDO)

DRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS