Signetics

FAST 74F30245,74F30640 Transceivers

FAST Products

'F30245 Octal 30Ω Transceiver Non-Inverting
(Open Collector With Enable + 3-State)
'F30640 Octal 30Ω Transceiver Inverting
(Open Collector With Enable + 3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30245	5.5ns	90mA
74F30640	5.0ns	85mA

FEATURES

- High impedance NPN base inputs for reduced loading
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- 'F30245 Non-Inverting
- 'F30640 Inverting
- Choice of outputs:
  Open collectors (B_0-B_7) and 3-states(A_0-A_7)
- Open-Collector outputs sink 160mA
- 160mA I_{OL} ideal for low-impedance applications and transmission line effects with impedance as low as 30Ω
- 3-state buffer outputs sink 24mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- Available in 24-pin standard slim DIP (300mil) plastic or CERDIP packages
- Flow through pinout structure facilitates PC board layout

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30245F, N74F30640F
24-Pin Plastic Slim DIP[1]	N74F30245N, N74F30640N

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

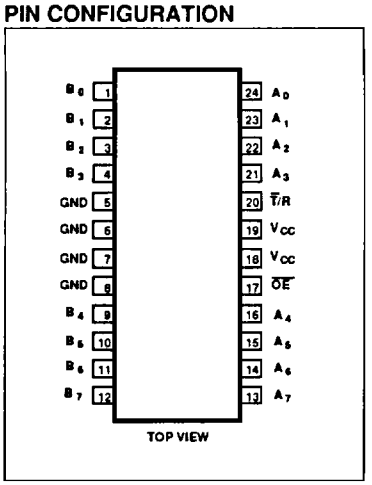
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Data inputs	3.5/0.1167	70μA/70μA
B_0- B_7	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	2.0/0.0667	40μA/40μA
T/R	Transmit/Receive input	2.0/0.0667	40μA/40μA
A_0- A_7	Data outputs (3-state)	150/40	3.0mA/24mA
B_0- B_7	Data outputs (OC)	OC/266.7	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

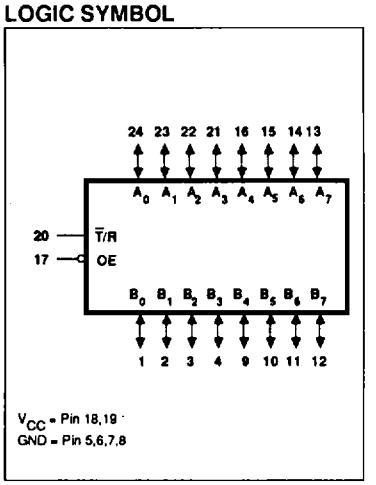
DESCRIPTION

The 74F30245/F30640 are high current octal transceivers. The 'F30245 has non-inverting data paths and the 'F30640 has inverting paths. The B outputs are open collector with 160mA I_{OL} while the A outputs are 3-state with 24mA I_{OL}. Both transceivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

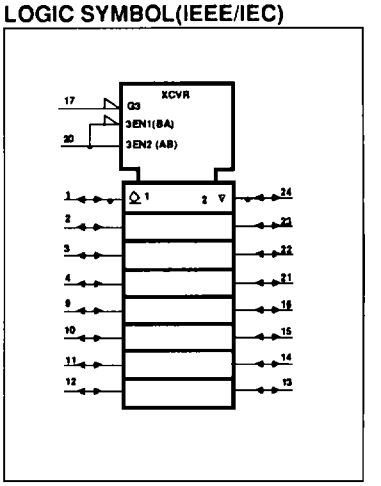
PIN CONFIGURATION



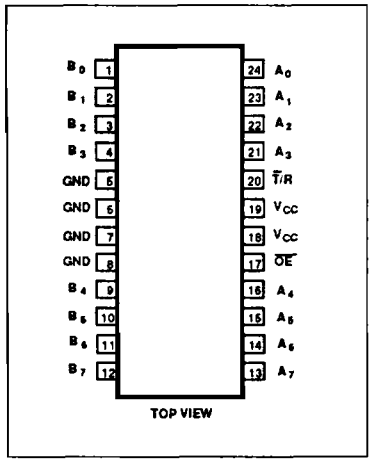
LOGIC SYMBOL



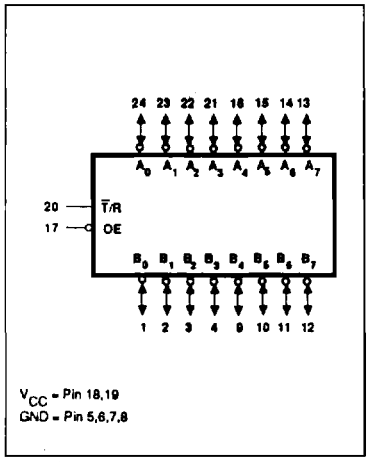
LOGIC SYMBOL(IEEE/IEC)



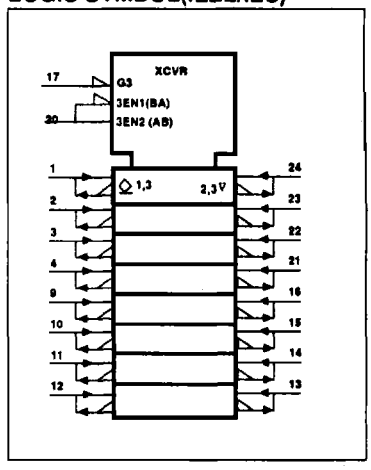
PIN CONFIGURATION



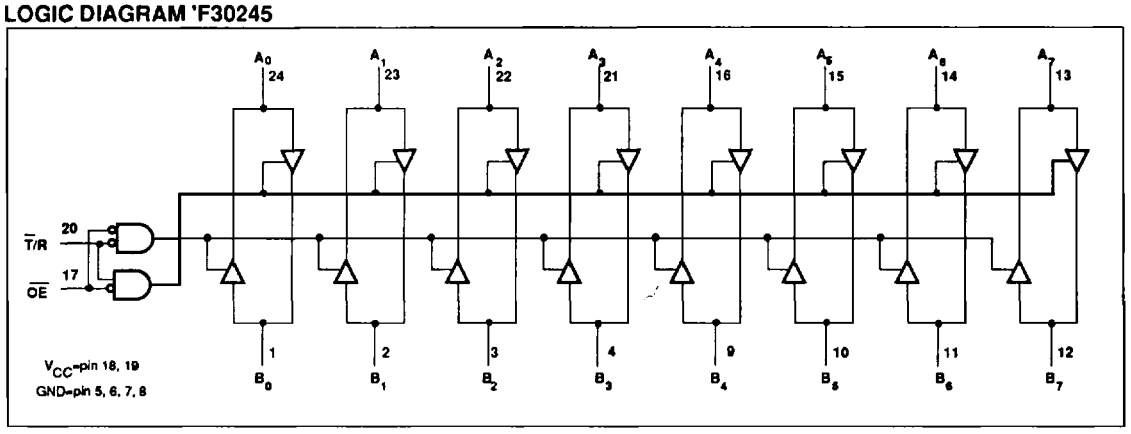
LOGIC SYMBOL



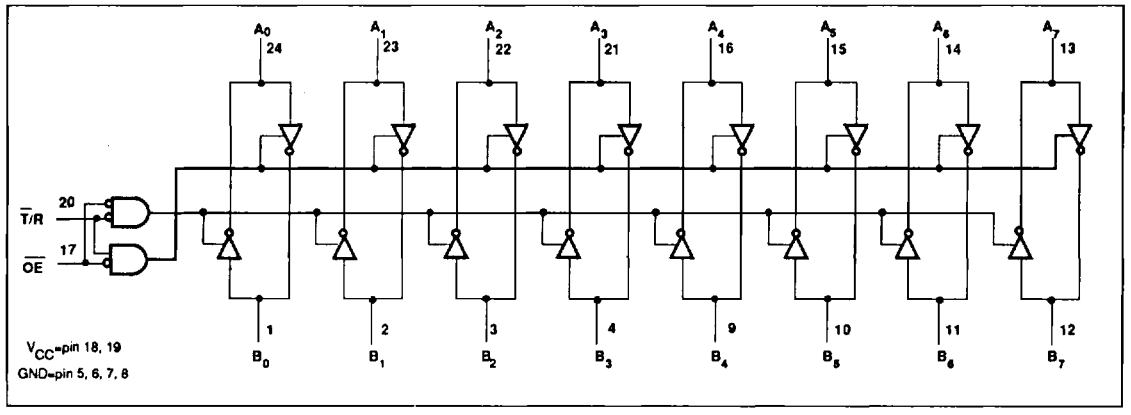
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM 'F30245



LOGIC DIAGRAM 'F30640



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS			
		'F30245		'F30640	
$\overline{OE}$	$\overline{T}$/R	A_n	B_n	A_n	B_n
L	H	A=B	Inputs	A=$\overline{B}$	Inputs
L	L	Inputs	B=A	Inputs	B=$\overline{A}$
H	X	Z	Z	Z	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	320	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	B_0-B_7			4.5	V
I_{OH}	High-level output current	A_0-A_7			-3	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			160	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current	B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=100mA	±10%V_{CC}		0.42	0.55	V
				I_{OL1}=160mA[4]	±5%V_{CC}			0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{T}$/R, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{T}$/R, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	µA
		B_0-B_7						20	µA
I_{IL}	Low-level input current	$\overline{T}$/R, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					-40	µA
		B_0-B_7						-600	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7	V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	'F30245	V_{CC} = MAX			50	80	mA
		I_{CCL}					100	145	mA
		I_{CCZ}					60	85	mA
		I_{CCH}	'F30640	V_{CC} = MAX			40	60	mA
		I_{CCL}					75	130	mA
		I_{CCZ}					45	65	mA

NOTES:

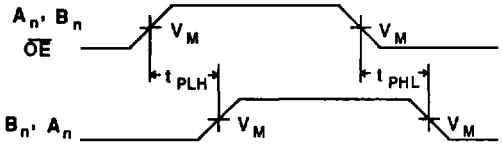
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

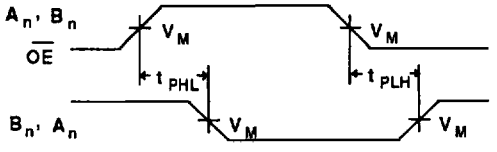
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH}* t_{PHL}	Propagation delay A_n to B_n	'F30245	Waveform 1,2	7.5 3.0	10.0 4.5	13.0 7.5	7.0 2.5	13.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1,2	2.0 2.0	3.5 3.5	6.5 6.0	1.5 1.5	7.0 6.5	ns
t_{PLH}* t_{PHL}	Propagation delay A_n to B_n	'F30640	Waveform 1,2	7.5 1.0	10.0 2.0	13.0 5.0	7.5 1.0	13.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1,2	1.0 1.0	2.5 2.0	5.5 5.0	1.0 1.0	6.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	B_n ouputs	Waveform 1,2	7.5 3.5	9.5 5.5	13.0 8.5	7.5 3.0	13.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	A_n ouputs	Waveform 3 Waveform 4	2.5 1.5	4.5 4.0	7.5 8.0	2.0 1.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	A_n ouputs	Waveform 3 Waveform 4	1.5 1.0	3.5 3.5	6.5 6.5	1.0 1.0	7.5 7.0	ns

* = See Figure A for Open Collector Output information

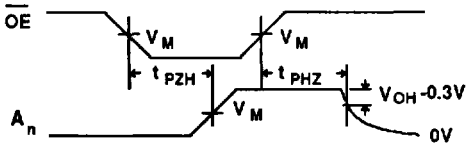
AC WAVEFORMS



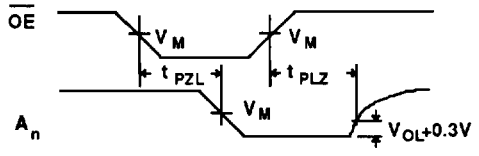
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



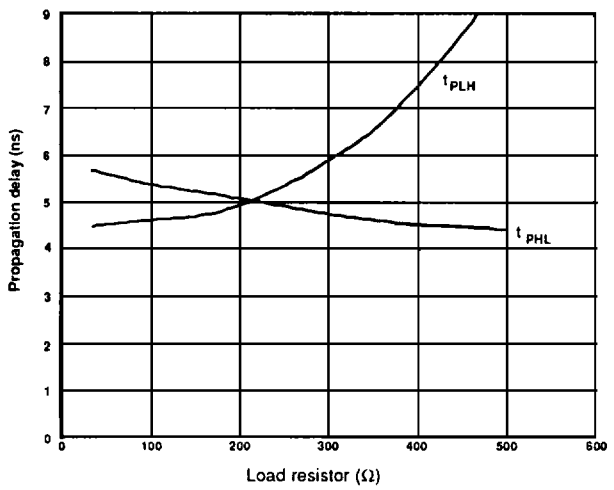
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

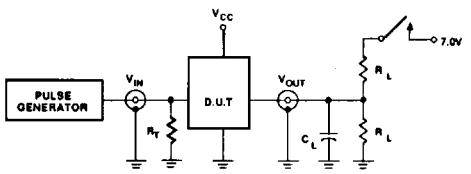
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

Figure A

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs and Open Collector (OC) outputs

SWITCH POSITION

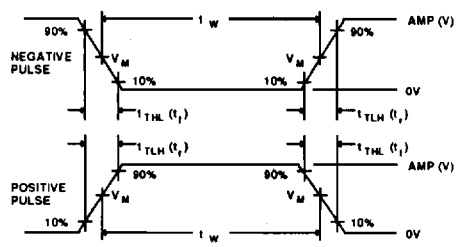
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns