Creation Date: 2/28/96
Revision: June 7, 1996

Aptos SEMICONDUCTOR

ADVANCED INFORMATION

AP9A104
AP9B104

5V and 3.3V, 64K x 16 CMOS Static RAM

Features

- Fast access times: 10, 12, 15, and 20 ns
- Fast output enable access time: 3, 3, 5, and 6 ns
- Multiple center power and ground pins for improved noise immunity
- High-performance, low-power, CMOS double-metal process
- Single 5V ±10% or 3.3V ± 10% supply
- Individual byte controls for both Read and Write cycles
- TTL-compatible I/O
- Packaged in 44-pin, 400-mil SOJ and 44-pin, 400-mil TSOP

Functional Description

The Aptos AP9A104-*(5V)* and AP9B104-*(3.3V)* are organized as a 64K x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Aptos static RAMs are fabricated using double-layer polysilicon technology.

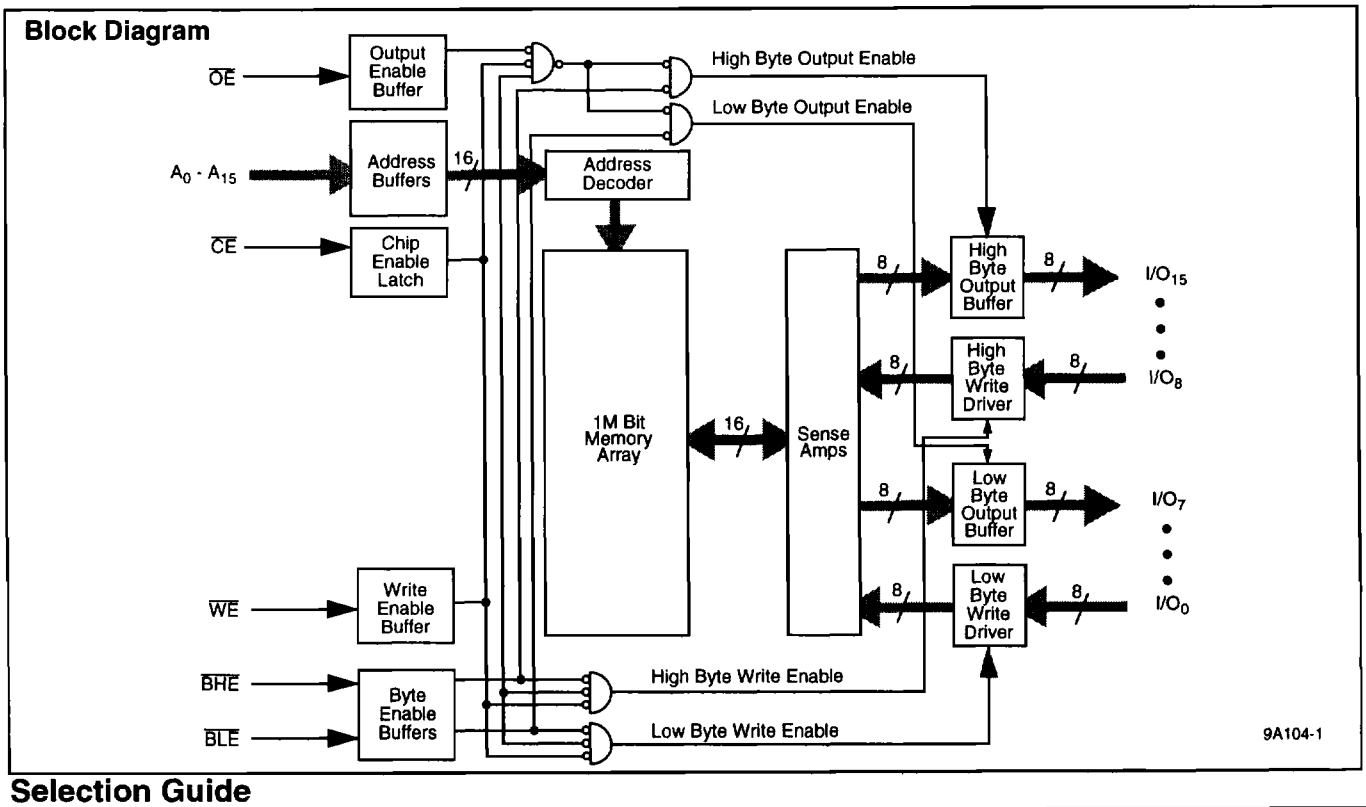
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Aptos offers Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) capabilities. This enhancement can place the output pin in High-Z for additional flexibility in system design.

The AP9A104/AP9B104 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW Chip Enable, separate upper and lower byte enables and a fast Output Enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls I/O_0 - I/O_7, the lower bits. $\overline{BHE}$ controls I/O_8 - I/O_{15}, the upper bits.

The AP9A104/AP9B104 operates from a single +5V/ +3.3V power supply and all inputs and outputs are fully TTL-compatible.

Block Diagram



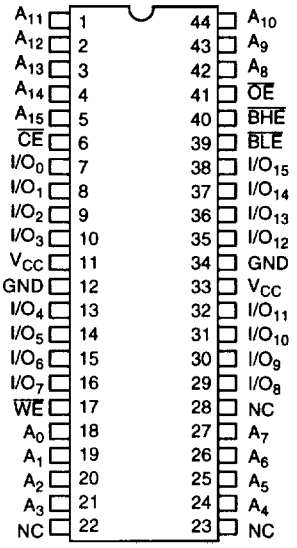
Selection Guide

	AP9A104-10 AP9B104-10	AP9A104-12 AP9B104-12	AP9A104-15 AP9B104-15	AP9A104-20 AP9B104-20
Maximum Access Time (ns)	10	12	15	20
Maximum Operating Current (mA)	230/140	220/130	200/120	190/100
Maximum Standby Current (mA)	5/2	5/2	5/2	5/2

Aptos Semiconductor • 3060 Tasman Drive, Santa Clara, CA 95054 • Phone: (408) 986-0188 FAX: (408) 986-0331

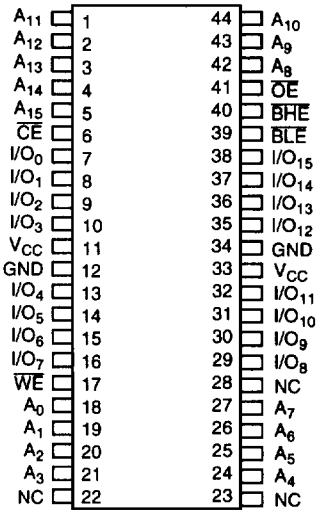
Pin Configurations

44-Pin SOJ
TOP VIEW



9A104-2

44-Pin TSOP
TOP VIEW



9A104-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....-55 °C to +150 ° C
V_{CC} Supply Relative to GND *(9A104)* .....-1.0 V to +7 V
V_{CC} Supply Relative to GND *(9B104)*.....-1.0 V to +5 V
Ambient Temperature.....-50 °C +125 °C
Short Circuit Output Current[1] ..... ± 50 mA
Voltage on any Pin Relative to GND.....-1.0 to V_{CC} +1.0 V
Power Dissipation.....1.0 W

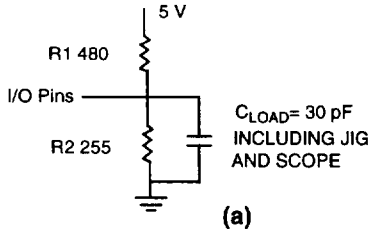
Electrical Characteristics ($0°C \le T_A \le 70°$ C, V_{CC} = 5V ± 10%, V_{CC} = 3.3V ± 10% *-AP9B104*)

Symbol	Parameter	Test Conditions	9A104-10 9B104-10		9A104-12 9B104-12		9A104-15 9B104-15		9A104-20 9B104-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE} = V_{IL}$, f = fmax		230/ 140		220/ 130		200/ 120		190/ 100	mA
I_{CC2}	Static Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE} = V_{IL}$, f = 0		120/ 50		120/ 50		120/ 50		120/ 50	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \ge V_{IH}$, f = Max.		5/2		5/2		5/2		5/2	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE} \ge V_{CC}$ -0.2V, $V_{IN} \ge V_{CC}$ -0.2V or $V_{IN} \le 0.2V$, f = 0		2/1		2/1		2/1		2/1	mA
I_{LI}	Input Leakage Current	GND ≤ $V_{IN} \le V_{CC}$	-1	1	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ $V_{OUT} \le V_{CC}$, Output Disabled	-1	1	-1	1	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

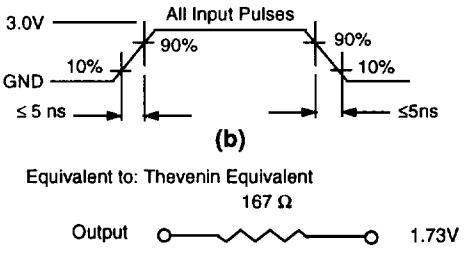
Capacitance

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{OUT}	I/O Capacitance	5	pF

AC Test Loads and Waveforms



(a)



(b)

Equivalent to: Thevenin Equivalent
167 Ω
Output
1.73V

Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. Negative undershoot of up to 3.0 V is permitted once per cycle.
4. Capacitances are maximum values at 25 °C measured at 1 MHz with V_{CC} = 5.0V.
5. Guaranteed but not tested.

Switching Characteristics Over the Operating Range[1]

Parameter	Description	9A104-10 9B104-10		9A104-12 9B104-12		9A104-15 9B104-15		9A104-20 9B104-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address Access Time		10		12		15		20	ns
t_{OHA}	Output Hold Time	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ Access Time		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ Access Time		3		3		5		6	ns
t_{LZOE}	$\overline{OE}$ to Low-Z Output	0		0		0		0		ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output		3		3		5		6	ns
t_{LZCE}	$\overline{CE}$ to Low-Z Output	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ to High-Z Output		5		6		8		9	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		10		12		15		20	ns
t_{ABE}	Byte Enable Access Time		3		3		5		6	ns
t_{LZBE}	Byte Enable to Output Low-Z	0		0		0		0		ns
t_{HZBE}	Byte Enable to Output High-Z		3		3		5		6	ns
Write Cycle[3]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ to Write End	7		8		10		12		ns
t_{AW}	Address to Set-up Time to Write End	7		8		10		12		ns
t_{HA}	Address Hold to Write End	0		0		0		0		ns
t_{SA}	Address Set-up Time	0		0		0		0		ns
t_{PWE1}[4]	$\overline{WE}$ Pulse Width ($\overline{OE}$ =HIGH)	7		8		10		12		ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =LOW)	10		12		12		15		ns
t_{SD}	Data Set-up to Write End	6		6		7		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output		5		6		7		9	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	2		2		2		2		ns
t_{BW}	Byte Enable to End of Write	7		8		10		12		ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 - 3 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*.
2. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ±500mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW and byte enable LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Set-up and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ High.
5. $\overline{WE}$ is HIGH for a Read Cycle.
6. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
7. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.
8. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.
9. $\overline{BHE}$ and $\overline{BLE}$ are held in their asserted state (LOW).
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZBE} is less than t_{LZBE}.

Pin Descriptions

A_0 - A_{15}: Address Inputs

These 16 address inputs select one of the 16-bit words in the RAM.

$\overline{CE}$: Chip Enable Input

$\overline{CE}$ is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while $\overline{CE}$ is asserted (LOW) and $\overline{WE}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is deasserted.

$\overline{WE}$: Write Enable Input

The Write Enable input is asserted LOW and controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

$\overline{BHE}$, $\overline{BLE}$: Byte Enables

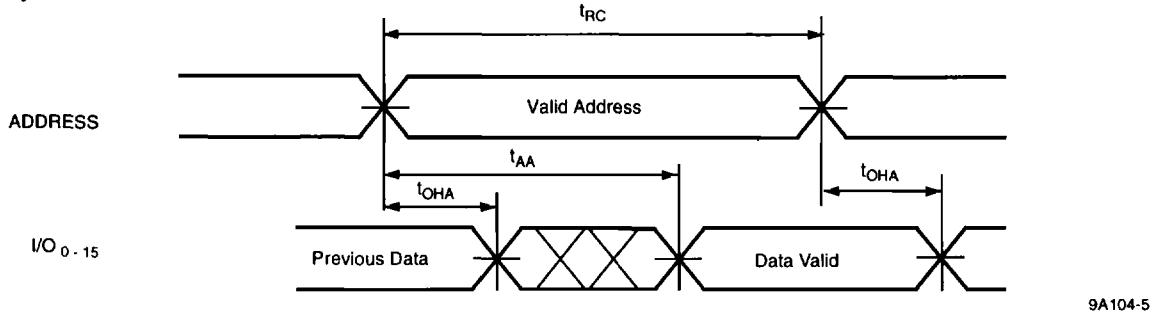
These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte (I/O_0 - I/O_7). When $\overline{BHE}$ is LOW, data is written or read to the upper byte (I/O_8 - I/O_{15}).

I/O_0 - I/O_{15}: Common Input/Output Pins

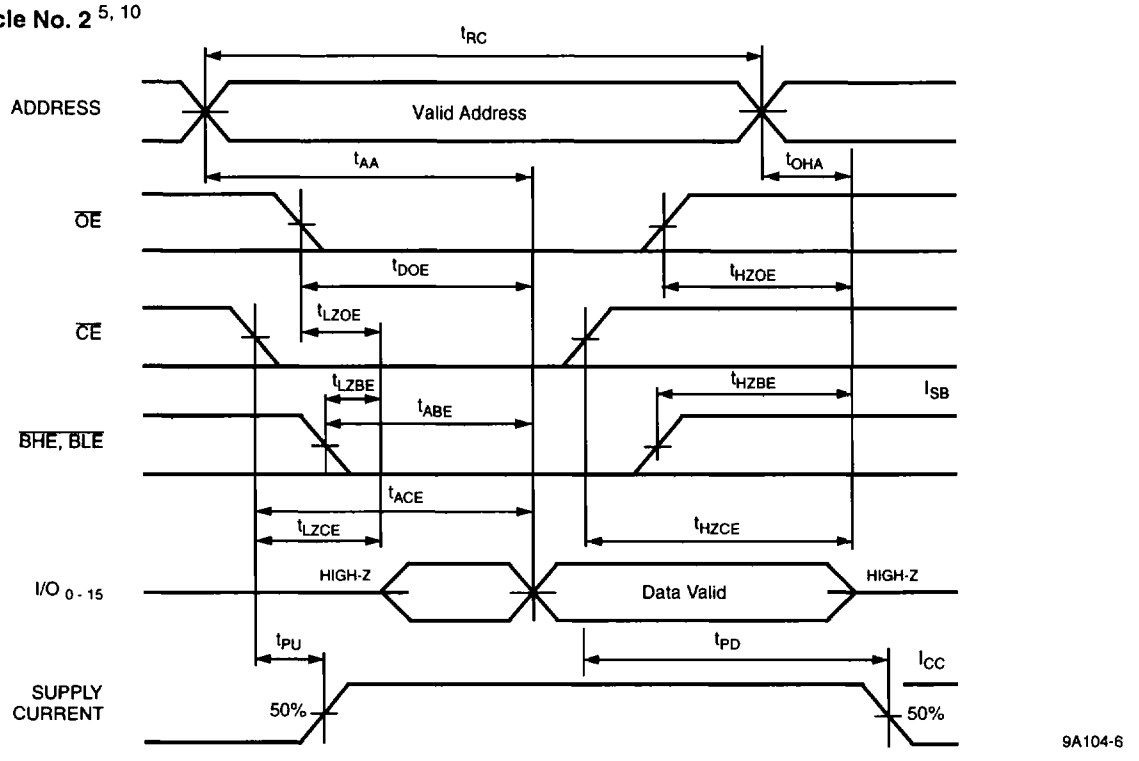
GND: Ground

Switching Waveforms

Read Cycle No. 1 [5, 6, 9]

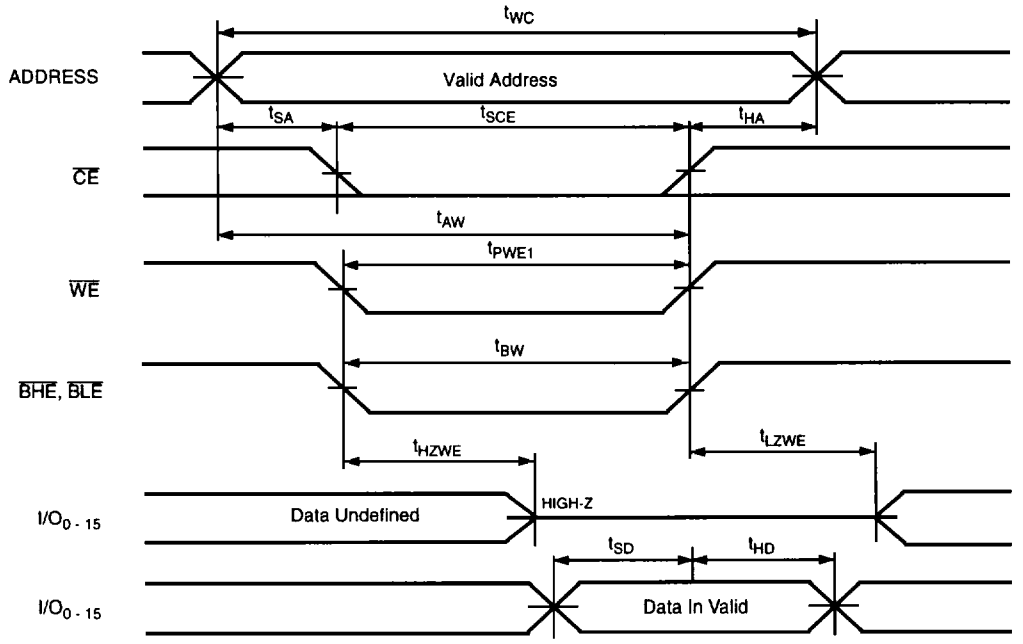


Read Cycle No. 2 [5, 10]

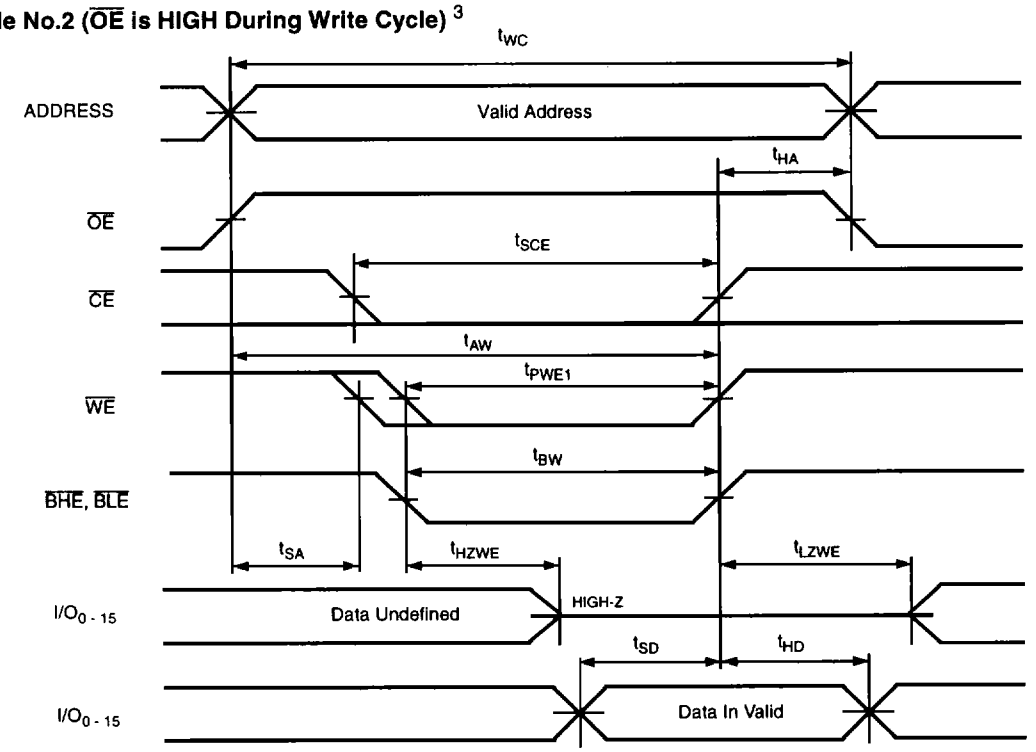


Switching Waveforms (continued)

Write Cycle No.1 ($\overline{CE}$ controlled, $\overline{OE}$ is HIGH or LOW) [3]

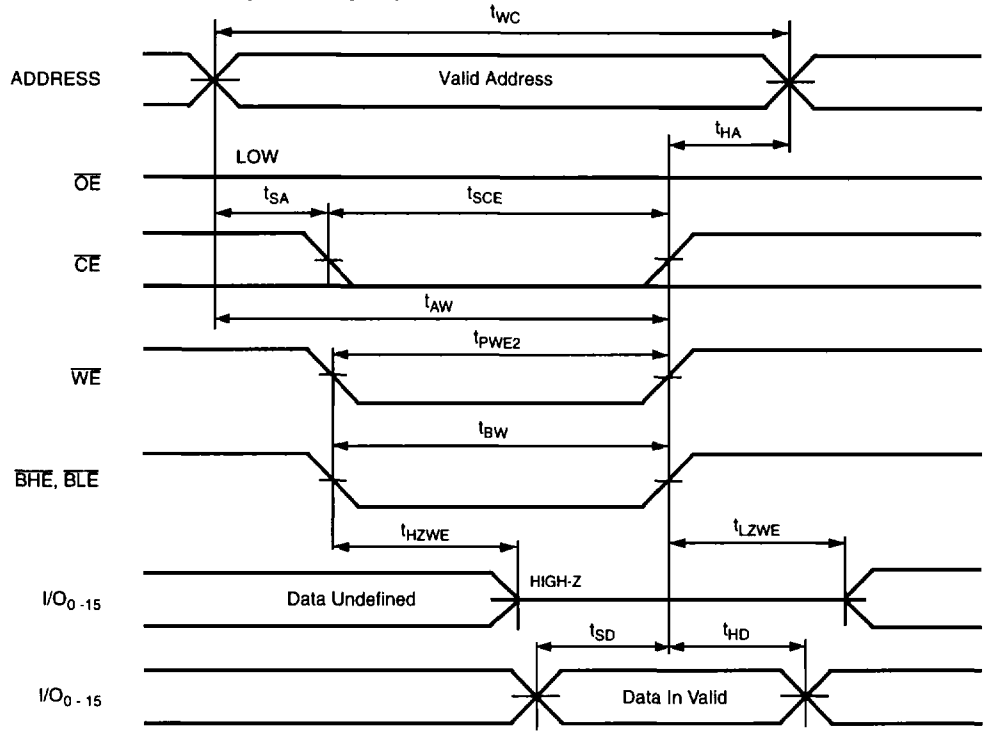


Write Cycle No.2 ($\overline{OE}$ is HIGH During Write Cycle) [3]



Switching Waveforms (continued)

Write Cycle No.3 ($\overline{OE}$ is LOW During Write Cycle) [3]



Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0 - I/O_7	I/O_8 - I/O_{15}	Power
Standby	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Low Byte Read (I/O_0 - I/O_8)	L	L	H	L	H	I_{OUT}	High-Z	I_{CC1}, I_{CC2}
High Byte Read (I/O_9 - I/O_{15})	L	L	H	H	L	High-Z	I_{OUT}	I_{CC1}, I_{CC2}
Word Read (I/O_0 - I/O_{15})	L	L	H	L	L	I_{OUT}	I_{OUT}	I_{CC1}, I_{CC2}
Word Write (I/O_0 - I/O_{15})	L	X	L	L	L	I_{IN}	I_{IN}	I_{CC1}, I_{CC2}
Low Byte Write (I/O_0 - I/O_8)	L	X	L	L	H	I_{IN}	High-Z	I_{CC1}, I_{CC2}
High Byte Write (I/O_9 - I/O_{15})	L	X	L	H	L	High-Z	I_{IN}	I_{CC1}, I_{CC2}
Output Disable	L	H	H	X	X	High-Z	High-Z	I_{CC1}, I_{CC2}
	L	X	X	H	H	High-Z	High-Z	I_{CC1}, I_{CC2}

Ordering Information

5V

Speed	Part Number	Package Name	Package Type	Temperature Range
10	AP9A104-10VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-10TC	T44.1	44-Pin Thin Small Outline Package	Commercial
12	AP9A104-12VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-12TC	T44.1	44-Pin Thin Small Outline Package	Commercial
15	AP9A104-15VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-15TC	T44.1	44-Pin Thin Small Outline Package	Commercial
20	AP9A104-20VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-20TC	T44.1	44-Pin Thin Small Outline Package	Commercial

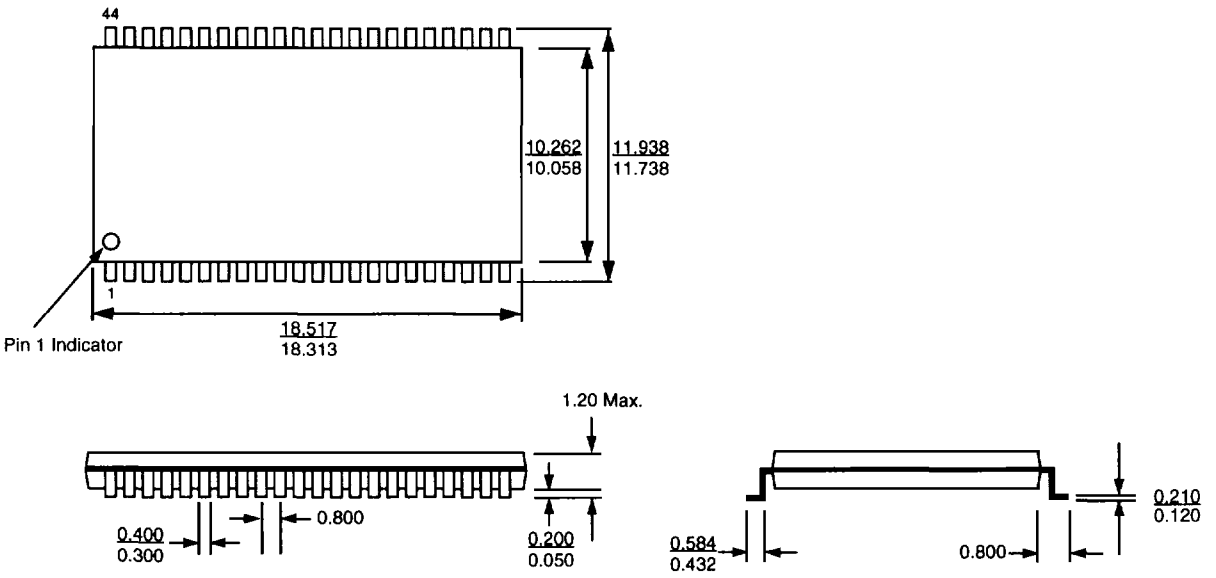
3.3V

Speed	Part Number	Package Name	Package Type	Temperature Range
10	AP9B104-10VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9B104-10TC	T44.1	44-Pin Thin Small Outline Package	Commercial
12	AP9B104-12VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9B104-12TC	T44.1	44-Pin Thin Small Outline Package	Commercial
15	AP9B104-15VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9B104-15TC	T44.1	44-Pin Thin Small Outline Package	Commercial
20	AP9B104-20VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9B104-20TC	T44.1	44-Pin Thin Small Outline Package	Commercial

Document # DS-00008-Rev A

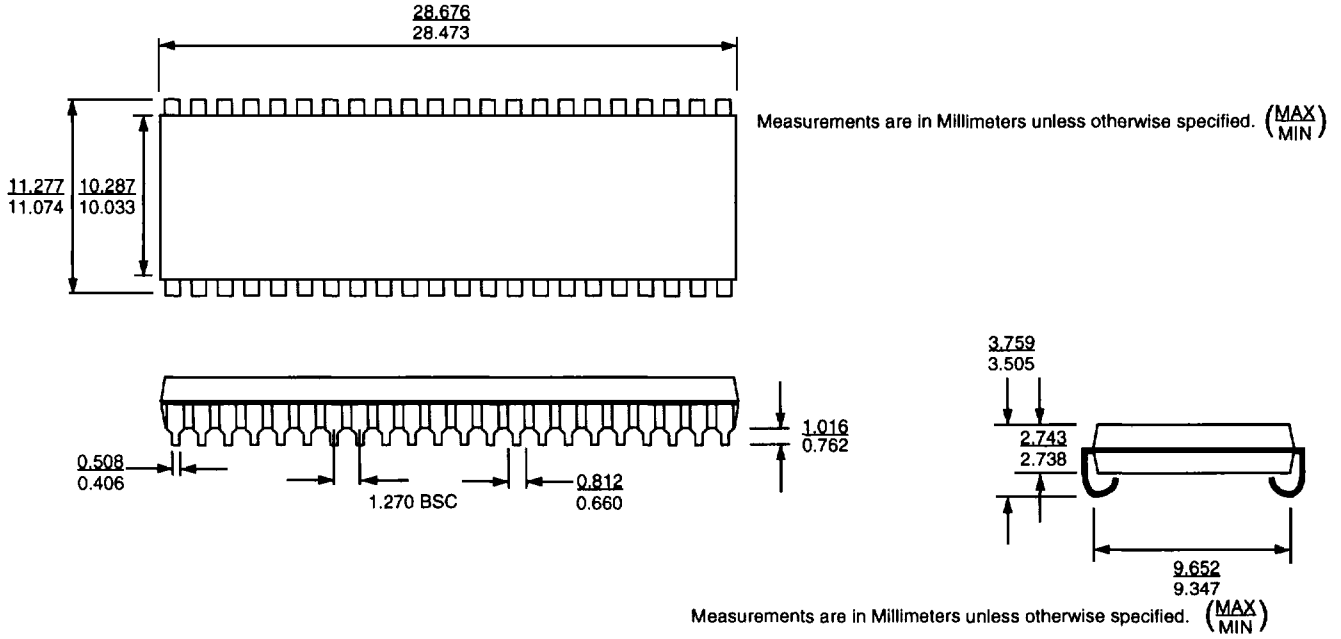
Package Diagrams

T44.1 - 44-Pin (400-Mil) Thin Small Outline Package (TSOP)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)

V44.1 - 44-Pin (400-Mil) Small Outline J-Bend (SOJ)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)