- **Pin and functional compatibility with the industry standard 8255A**
- **Supports 8086/8088 and 80186/188 microprocessors**
- **Very high speed - 10, 8 and 5 MHz *zero wait state* operation**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **24 programmable I/O pins**
- **Direct bit set/reset capability**
- **Bi-directional bus operation**
- **Enhanced control word read capability**
- **Bus-hold circuitry on all I/O ports eliminates the need for external pull-up resistors**

The CA82C55A Programmable Peripheral Interface is a high performance CMOS device offering pin for pin functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. Bus hold circuitry on all I/O ports together with TTL compatibility over the full temperature range eliminates the need for pull-up resistors.

The CA82C55A is a general purpose programmable I/O device designed for use with several different microprocessors. Its high speed and high performance make it ideally suited for aerospace and defense applications, while the low power consumption suits it to portable systems and systems with low power standby modes.

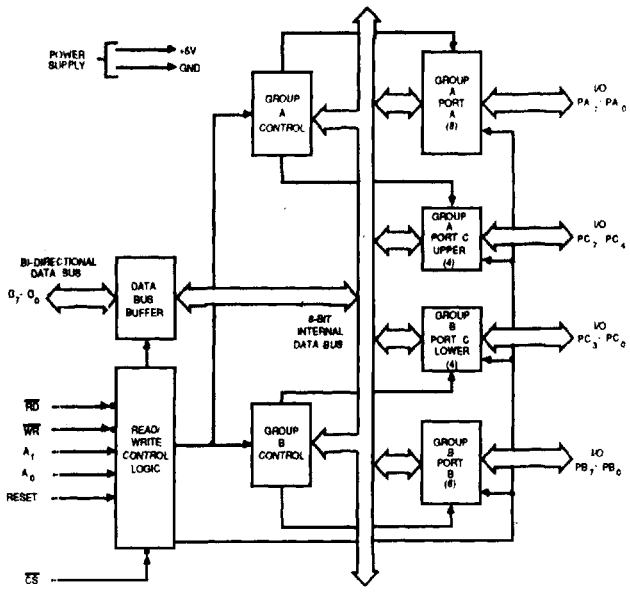


Figure 1 : CA82C55A BLOCK DIAGRAM

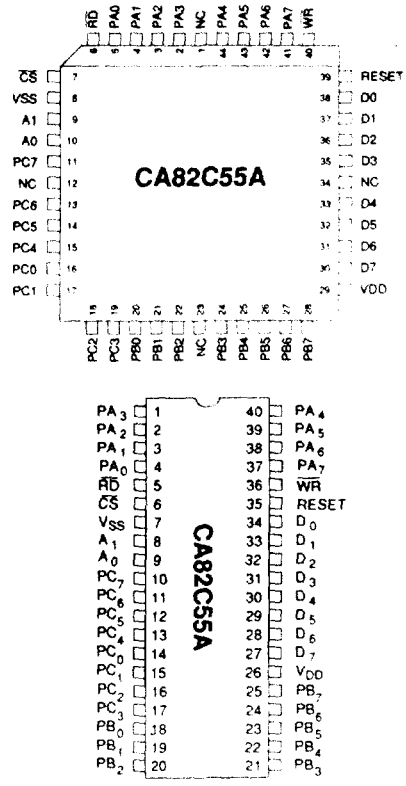


Figure 2 : PLCC and DIP PIN CONFIGURATIONS

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s) PLCC	Pin(s) PDIP	Type	Name and Function
A_1, A_0	9, 10	8, 9	I	**Address:** These input signals, in conjunction with RD and WR, control the selection of one of the three ports or the control word registers.
CS	7	6	I	**Chip Select:** A low on this input enables the CA82C55A to respond to RD and WR signals. RD and WR are ignored otherwise.
D_{0-7}	38-30	34-27	I/O	**Data Bus:** Bi-directional, tri-state data bus lines, connected to system data bus.
PA_{0-7}	5-2 44-41	4-1 40-37	I/O	**Port A, Pins 0-7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
PB_{0-7}	20-28	18-25	I/O	**Port B, Pins 0-7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
PC_{0-3}	16-19	14-17	I/O	**Port C, Pins 0-3:** Lower nibble of an 8-bit data output latch/buffer an an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{4-7}	15-13,11	13-10	I/O	**Port C, Pins 4-7:** Upper nibble of Port C.
RD	6	5	I	**Read Control:** This input is low during CPU read operations.
RESET	39	35	I	**Reset:** A high on this input clears the control register and all ports are set to the input mode.
V_{DD}	29	26		**Power:** 5 V ± 10% DC Supply
V_{SS}	8	7		**Ground:** 0 V
WR	40	36	I	**Write Control:** This input is low during CPU write operations.

A_1	A_0	RD	WR	CS	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus

A_1	A_0	RD	WR	CS	Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control

A_1	A_0	RD	WR	CS	Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

FUNCTIONAL DESCRIPTION

General

The CA82C55A is a programmable peripheral interface device designed for use in high speed, low power microcomputer systems. It is a general purpose I/O component which functions to interface peripheral equipment to the microcomputer system bus. The functional configuration of the CA82C55A is programmed by the system software such that no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bi-directional 8-bit buffer is used to interface the CA82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. The data bus buffer also transfers control words and status information.

Read/Write and Control Logic

This block manages all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control buses and issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. The CPU *outputs* a control word to the CA82C55A. The control word contains information such as *mode, bit set, bit reset,* etc., that initializes the functional configuration of the CA82C55A.

Each of the Control blocks (Group A and Group B) accepts *commands* from the Read/Write Control Logic, receives *control words* from the internal data bus and issues the proper commands to its associated ports.

- Control Group A - Port A and Port C upper (C_7 - C_4)
- Control Group B - Port B and Port C lower (C_3 - C_0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions (Table 1). The control word format for both Read and Write operations is shown in Figure 8. Bit D_7 will always be a logic ONE when the control word is read, as this implies control word mode information.

Ports A, B and C

The CA82C55A contains three 8-bit ports (A, B and C). All can be configured in a wide variety of functional characteristics by the system software, but each also has its own special features.

Port A: One 8-bit data output latch/buffer and one 8-bit input latch. Both *pull-up* and *pull-down* bus hold devices are present on Port A.

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer. Only *pull-up* bus hold devices are present on Port B.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only *pull-up* bus hold devices are present on Port C.

See Figure 3 for the bus-hold circuit configuration for Ports A, B and C.

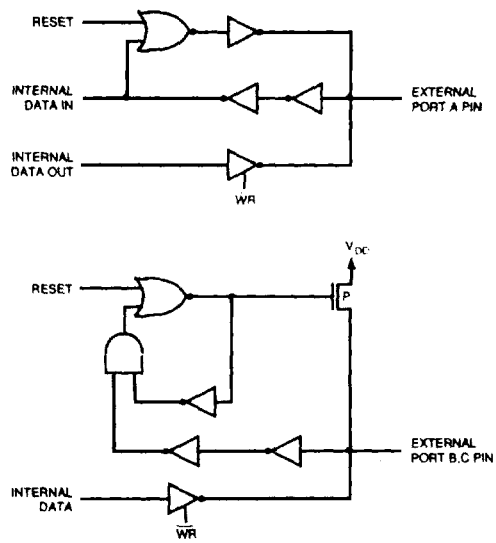


Figure 3 : PORTs A, B & C BUS-HOLD CONFIGURATION

Table 2 : AC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

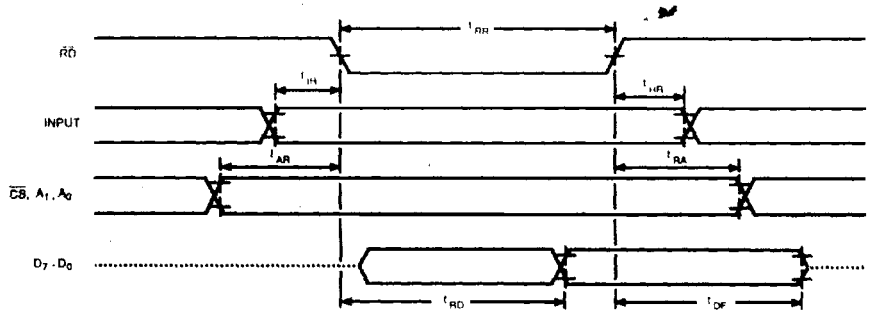
Symbol	Parameter	Test Conditions	Limits (5 MHz) Min	Limits (5 MHz) Max	Limits (8 MHz) Min	Limits (8 MHz) Max	Limits (10 MHz) Min	Limits (10 MHz) Max	Units
t_{AD}	$\overline{ACK}$ = 0 to Output			300		175		125	ns
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1			350		150		100	ns
t_{AK}	$\overline{ACK}$ Pulse Width		300		200		100		ns
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1			350		150		100	ns
t_{AR}	Address Stable Before $\overline{RD}$ ↓		20		0		0		ns
t_{AW}	Address Stable Before $\overline{WR}$ ↓		0		0		0		ns
t_{DF}	$\overline{RD}$ ≠ Data Floating $\overline{RD}$ ↑ to Data Floating		10	100	10	75	10	75	ns
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑		100		100		50		ns
t_{HR}	Peripheral Data After $\overline{RD}$		20		0		0		ns
t_{IR}	Peripheral Data Before $\overline{RD}$		20		0		0		ns
t_{KD}	$\overline{ACK}$ = 1 to Output Float		20	250	20	250	20	175	ns
t_{PH}	Peripheral Data After STB High		180		50		40		ns
t_{PS}	Peripheral Data Before STB High		20		20		20		ns
t_{RA}	Address Hold Time After $\overline{RD}$ ↑		20		0		0		ns
t_{RD}	Data Delay from $\overline{RD}$ ↓			200		120		95	ns
t_{RES}	Reset Pulse Width	See Note 2	500		500		400		ns
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0			300		150		120	ns
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0			400		200		160	ns
t_{RR}	$\overline{RD}$ Pulse Width		300		150		100		ns
t_{RV}	Recovery Time between $\overline{RD}$/$\overline{WR}$		850		200		100		ns
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1			300		150		100	ns
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1			300		150		100	ns
t_{ST}	$\overline{STB}$ Pulse Width		300		100		50		ns
t_{WA}	Address Hold Time After $\overline{WR}$ ↑	Ports A & B Port C	30 30		20 20		10 10		ns ns
t_{WB}	$\overline{WR}$ = 1 to Output			350		350		150	ns
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	Ports A & B Port C	40 40		30 30		20 20		ns ns
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	See Note 1		850		200		160	ns
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0			650		150		120	ns
t_{WW}	$\overline{WR}$ Pulse Width		300		100		70		ns

Notes: 1. INTR ↑ may occur as early as $\overline{WR}$ ↓.

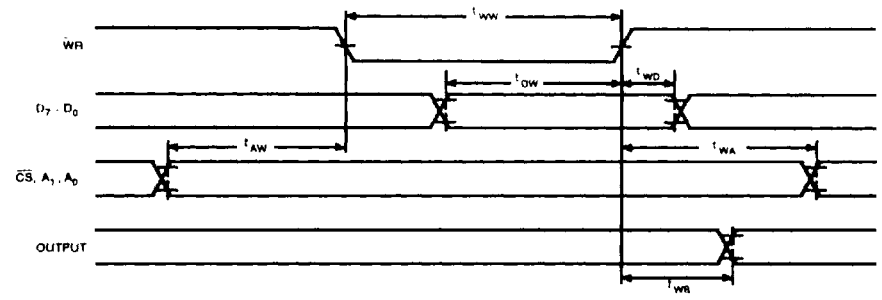
2. Width of initial Reset pulse after power on must be at least 50 µSec. Subsequent Reset pulses may be 500 ns minimum.

Figure 4 : TIMING DIAGRAMS

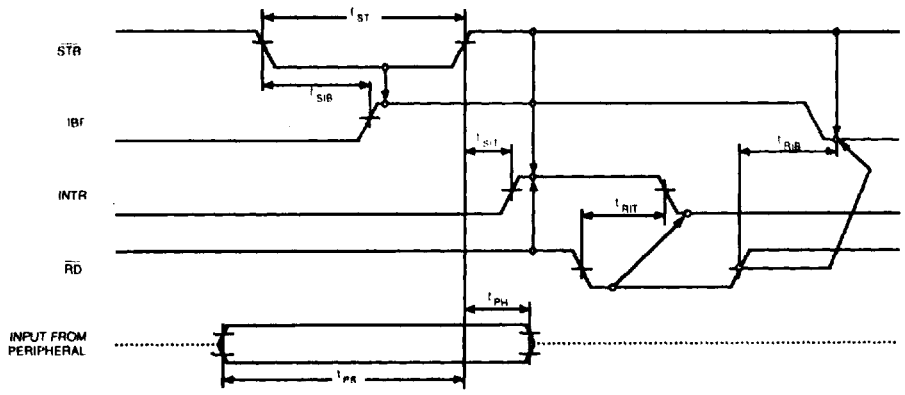
a) Mode 0 (Basic Input)



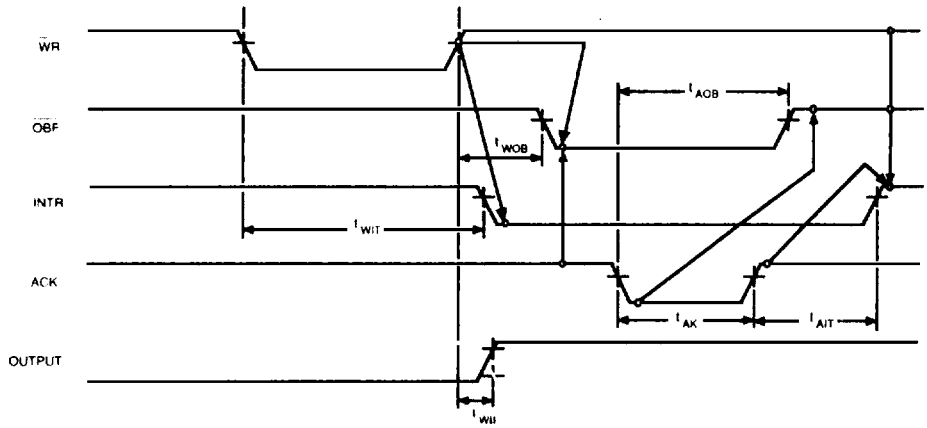
b) Mode 0 (Basic Output)



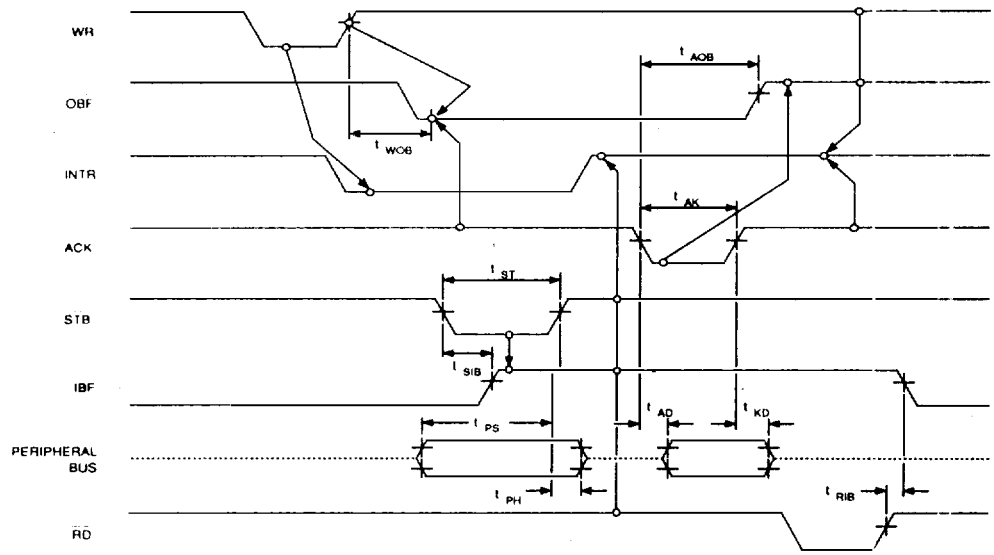
c) Mode 1 (Strobed Input)



d) Mode 1 (Strobed Output)

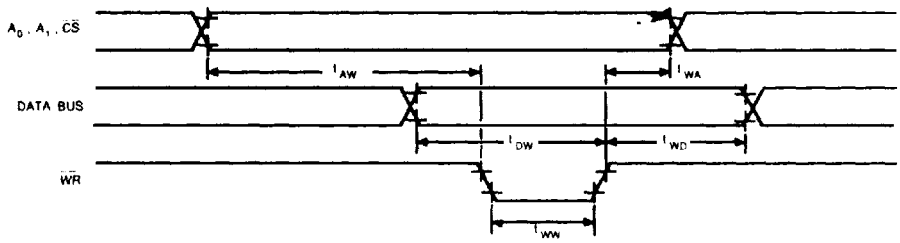


e) Mode 2 (Bi-directional)

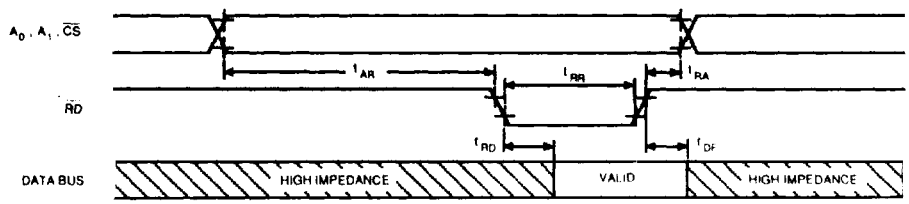


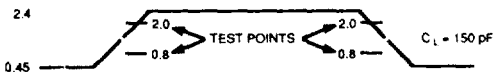
Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$, is permissible (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$).

f) Write Timing



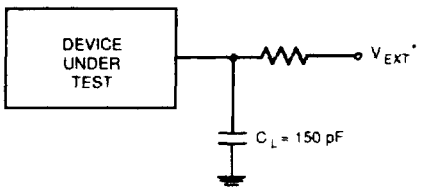
g) Read Timing





A.C. Testing Inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

Figure 5 : AC TESTING I/O WAVEFORM



* V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance.

Figure 6 : AC TESTING LOAD CIRCUIT

Table 3 : DC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	V_{DD} Supply Current	(Note 3)	-	10	mA
I_{DDSB}	V_{DD} Supply Current-Standby	V_{DD} = 5.5 V V_{IN} = V_{DD} or V_{SS} *Port Conditions:* If I/P = Open/High O/P = Open Only Data Bus = High/Low CS = High Reset = Low Pure Inputs = Low/High	-	10	µA
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} to 0V (Note 1)	-	±1	µA
I_{OFL}	Output Float Leakage Current	V_{IN} = V_{DD} to 0V (Note 2)	-	±10	µA
I_{PHH}	Port Hold High Leakage Current	V_{OUT} = 3.0 V Ports A, B and C	–50	–350	µA
I_{PHL}	Port Hold Low Leakage Current	V_{OUT} = 1.0 V Port A only	+50	+350	µA
V_{IH}	Input High Voltage		2.0	V_{DD}	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = –2.5 mA	3.0	-	V
		I_{OH} = –100 µA	V_{DD} – 0.4	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.5 mA	-	0.4	V

Notes: 1. Pins A_1, A_0, CS, WR, RD, Reset.
2. Data Bus; Ports B, C.
3. Outputs Open

Table 4 : CAPACITANCE (T_A = 25 °C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
C_{IN}	Input Capacitance	Unmeasured Pins		10	pF
$C_{I/O}$	I/O Capacitance	Returned to V_{SS}		20	pF

Table 5 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage		+4 V to +6 V
Operating Temperature Range	Commercial	0°C to 70 °C
	Industrial	–40°C to +85°C
	Military	–55°C to +125°C

3

Table 6 : ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	+7.0 V
Input, Output or I/O Voltage Applied	V_{SS} – 0.5 V to V_{CC} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Maximum Package Power Dissipation	1 W

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic input/output
- Mode 1 - Strobed input/output
- Mode 2 - Bi-directional Bus

When the Reset input goes *high* all ports will be set to the input mode with all 24 port lines held at a logic one level by the internal bus hold devices. After the reset is removed, no additional initialization is required for the CA82C55A to remain in the input mode. No pullup or pulldown devices are required. During the execution of the system program, any of the other modes may be deleted by using a single output instruction. This allows a single CA82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined such that their functional definition can be tailored to almost any I/O structure. For example, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, and Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

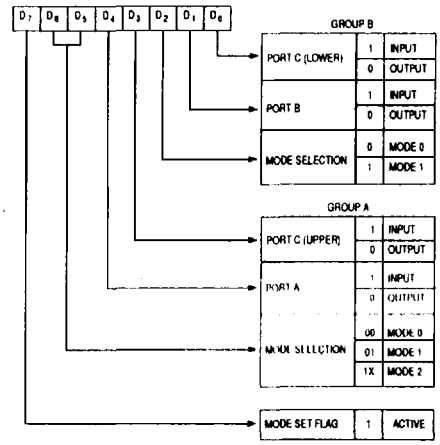


Figure 8 : MODE DEFINITION FORMAT

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces the software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation as if they were data output ports.

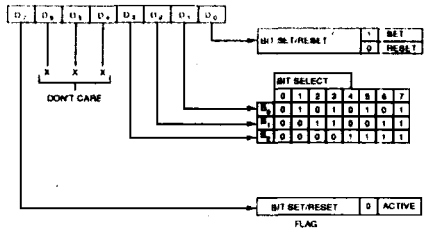


Figure 9 : BIT SET/RESET FORMAT

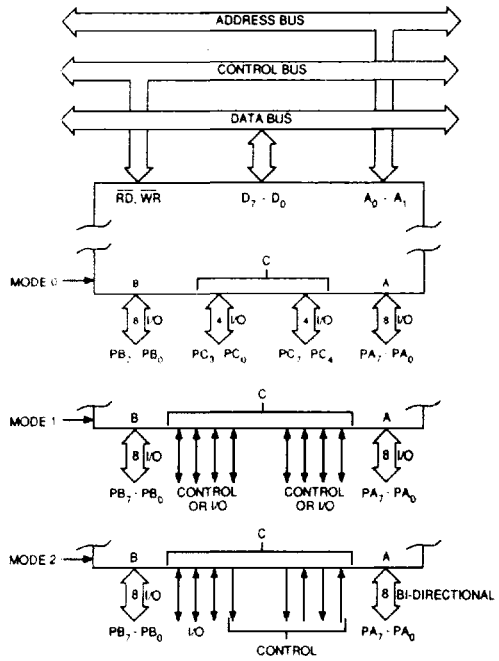


Figure 7 : MODE DEFINITIONS and BUS INTERFACE

Interrupt Control Functions

When the CA82C55A is operating in Mode 1 or Mode 2, control signals are provided for use as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the bit set/reset function of Port C.

This function allows the Programmer to allow or disallow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable

(BIT-RESET) - INTE is RESET - Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output)

This mode provides simple input and output operations for each of the three ports. No *handshaking* is required. Data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this mode.

Table 7 : MODE 0 PORT DEFINITION

Control Word #	Control Word Bits								Port Direction			
	GROUP A					GROUP B			GROUP A		GROUP B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	PA_7-PA_0	PC_7-PC_4	PC_3-PC_0	PB_7-PB_0
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	INPUT	OUTPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	OUTPUT	INPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	INPUT	OUTPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	OUTPUT	INPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	INPUT	OUTPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	OUTPUT	INPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	INPUT	OUTPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	OUTPUT	INPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT

Refer to Figure 10 for an example of a Mode 0 Configuration

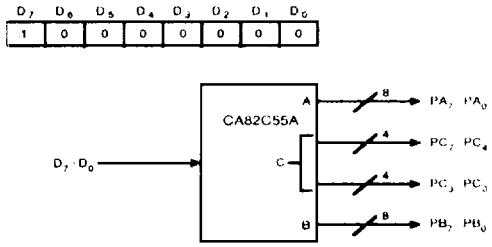


Figure 10 : MODE 0 CONFIGURATION

Mode 1 (Strobed Input/Output)

This mode transfers I/O data to or from a specified port in conjunction with strobes or *handshaking* signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these *handshaking* signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definitions

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that the data has been loaded into the input latch. IBF is set by the $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ being a ONE, IBF is a ONE and INTE is a ONE. It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A
Controlled by bit set/reset of PC_4.

INTE B
Controlled by bit set/reset of PC_2

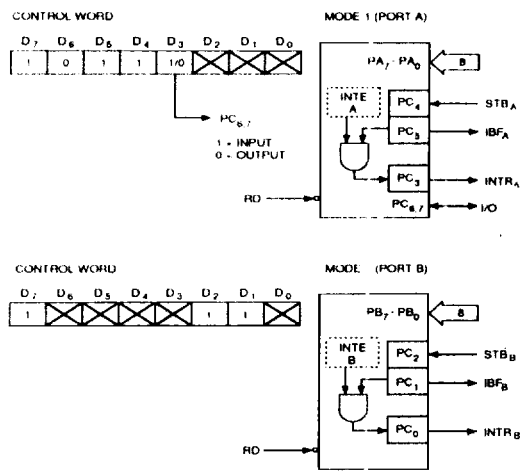


Figure 11 : MODE 1 INPUT

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F): The $\overline{OBF}$ output will go LOW to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by the $\overline{ACK}$ Input being low.

ACK (Acknowledge Input): A LOW on this input informs the CA82C55A that the data from Port A or Port B has been accepted. (i.e. a response from the peripheral device indicating that it has received the data output by the CPU).

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a ONE, $\overline{OBF}$ is a ONE and INTE is a ONE. It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

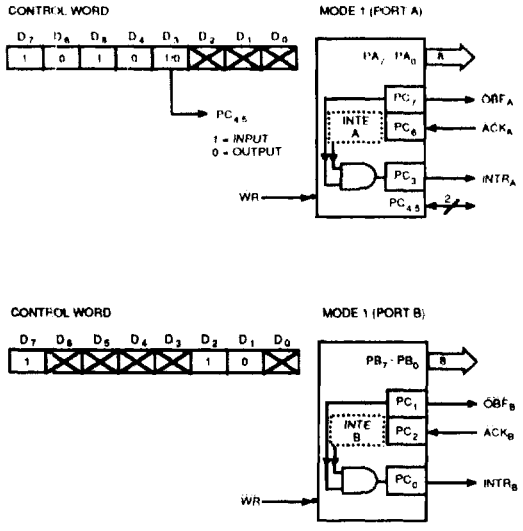


Figure 12 : MODE 1 OUTPUT

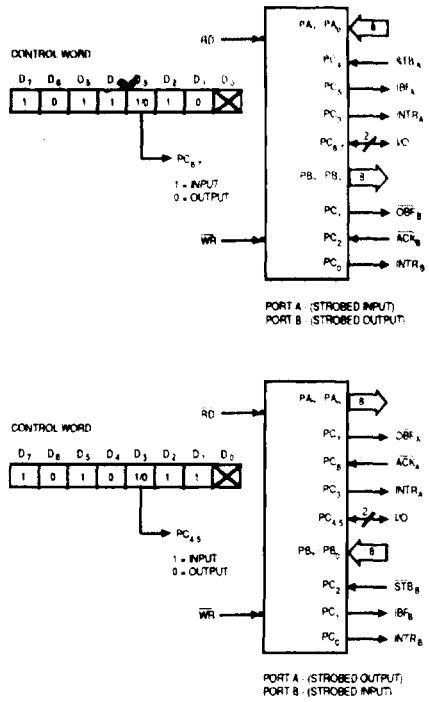


Figure 13 : COMBINATIONS OF MODE 1

Mode 2 (Strobed Bi-directional Bus I/O)

This mode provides a means for communicating with a peripheral device or a structure on a single 8-bit bus to facilitate both the transmitting and the receiving of data (bi-directional bus I/O). *Handshaking* signals maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status of the 8-bit, bi-directional bus port (Port A).

Bi-directional Bus I/O Control Signal Definition

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full): The $\overline{OBF}$ output will go LOW to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge): A LOW on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$): Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF): Controlled by bit set/reset of PC_4.

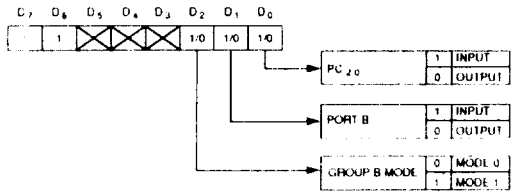


Figure 14 : MODE CONTROL WORD

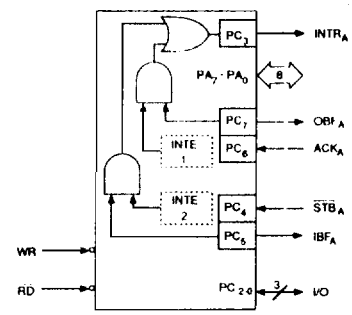


Figure 15 : MODE 2

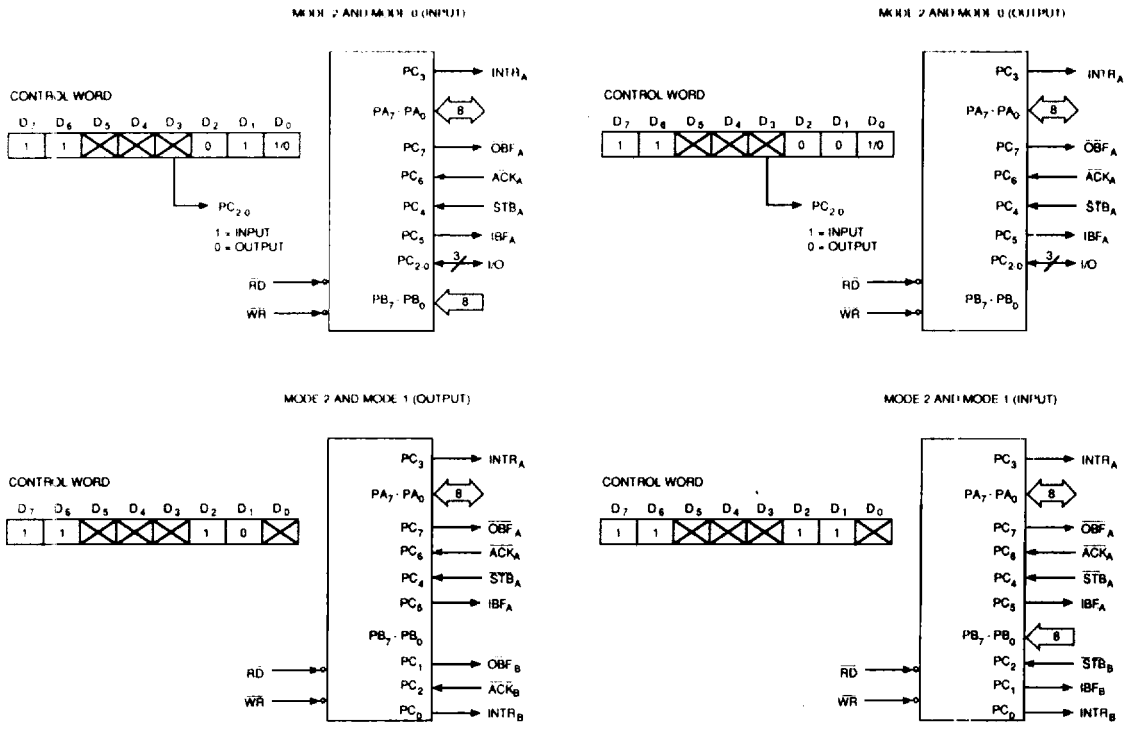


Figure 16 : MODE 1/4 COMBINATIONS

Table 8 : MODE DEFINITION SUMMARY

PORT		MODE 0	MODE 1				MODE 2
PORT A	PA_0 PA_1 PA_2 PA_3 PA_4 PA_5 PA_6 PA_7	All IN or All OUT	All IN or All OUT				All BI-DIRECTIONAL
PORT B	PB_0 PB_1 PB_2 PB_3 PB_4 PB_5 PB_6 PB_7	All IN or All OUT	All IN or All OUT				Not Used in MODE 2
			A IN, B IN	A IN, B OUT	A OUT, B IN	A OUT, B OUT	
PORT C	PC_0	All IN	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$	I/O
	PC_1	or	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$	I/O
	PC_2	All OUT	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
	PC_3		$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
	PC_4	All IN	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O	$\overline{STB}_A$
	PC_5	or	IBF_A	IBF_A	I/O	I/O	IBF_A
	PC_6	All OUT	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	$\overline{ACK}_A$
	PC_7		I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	$\overline{OBF}_A$

3

Special Mode Combination Considerations

Several combinations of modes are possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a *Set Mode* command.

The state of all the Port C lines, except the ACK and STB lines, will be placed on the data bus during a read of Port C. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4, and PC_6 bit positions as shown in Table 9.

Through a *Write Port C* command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a *Write Port C* command, and the interrupt enable flags cannot be accessed. *The Set/Reset Port C Bit* command must be used to write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag.

With a *Set/Reset Port C Bit* command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be set or reset. Port C lines programmed as inputs, including ACK and STB lines, are not affected by a *Set/Reset Port C Bit* command. Writing to the corresponding Port C bit positions of the ACK and $\overline{STB}$ lines with the *Set/Reset Port C Bit* command will affect the Group A and Group B interrupt enable flags (see Table 9).

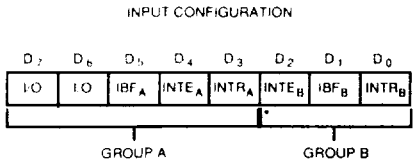
Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. Thus the CA82C55A can directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the CA82C55A is in Modes 1 or 2, Port C generates or accepts *handshaking* signals with the peripheral device. Reading Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. This function is performed by executing a normal read operation of Port C.



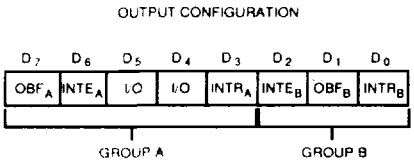
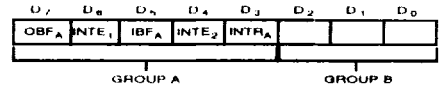


Figure 17 : MODE 1 STATUS WORD FORMAT



(Defined by Mode 0 or Mode 1 Selection)

Figure 18 : MODE 2 STATUS WORD FORMAT

Table 9 : INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
$INTE_B$	PC_2	ACK_B (Output Mode 1) or STB_B (Input Mode 1)
$INTE_{A2}$	PC_4	STB_A (Input Mode 1 or Mode 2)
$INTE_{A1}$	PC_6	ACK_A (Output Mode 1 or Mode 2)

APPLICATIONS

The CA82C55A is a very powerful device for interfacing peripheral equipment to the microcomputer system. It is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a *service routine* associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the CA82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the interface characteristics of the I/O device for both data transfer and timing, and matching this information to the examples and tables in the *Operational Description*, a control word can easily be developed to initialize the CA82C55A to exactly *fit* the application. Figures 19 through 25 illustrate a few examples of typical CA82C55A applications.

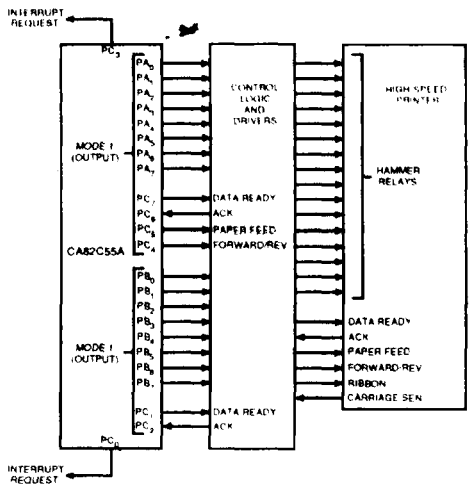


Figure 19 : PRINTER INTERFACE

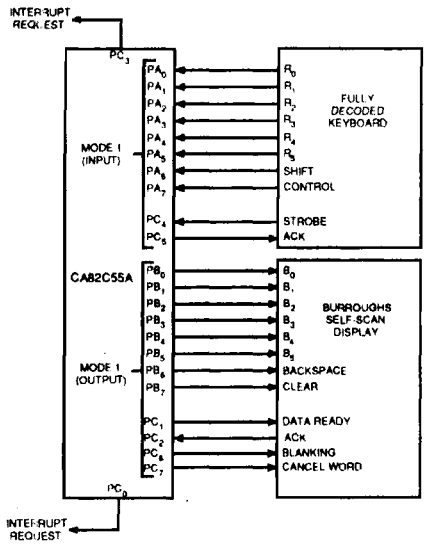


Figure 20 : KEYBOARD and DISPLAY INTERFACE

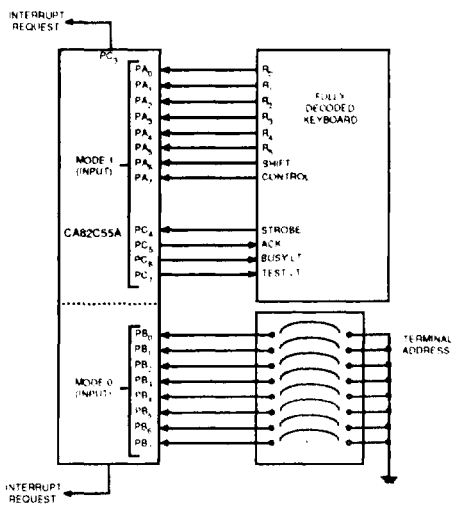


Figure 21 : KEYBOARD and TERMINAL ADDRESS INTERFACE

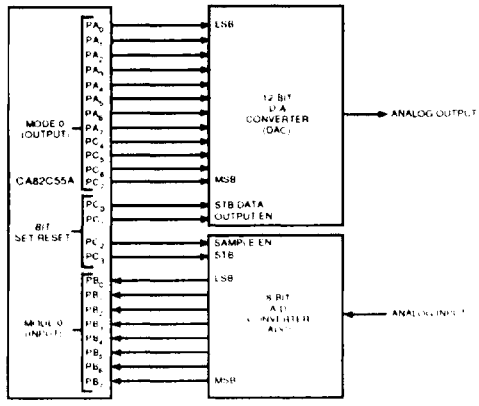


Figure 22 : DIGITAL TO ANALOG, ANALOG TO DIGITAL

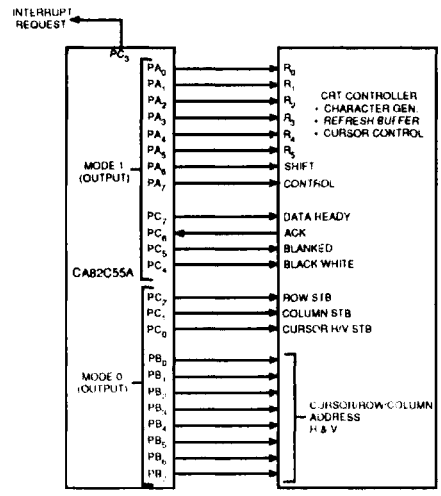


Figure 24 : BASIC FLOPPY DISC INTERFACE

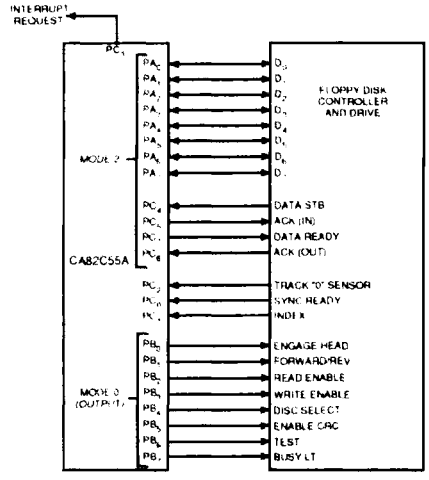


Figure 23 : BASIC CRT CONTROLLER INTERFACE

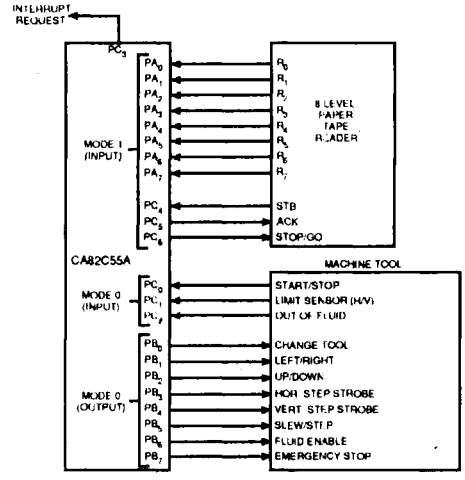


Figure 25 : MACHINE TOOL CONTROLLER INTERFACE