

1 Megabit CMOS Boot Block Flash Memory

- Fast Read Access Time: 90/120/150 ns
- On-Chip Address, Data Latches, Programming and Erase Algorithms
- Blocked Architecture:
 - One 8 KB Boot Block w/ Lock Out
 - Two 4 KB Parameter Blocks
 - One 112 KB Main Block
- Low Power CMOS Operation
- 12.0V $\pm$ 5% Programming and Erase Voltage
- Embedded Algorithms Program & Erase
- High Speed Programming
- Deep Powerdown Mode
 - 0.05 μ A I_{CC} Typical
 - 0.8 μ A I_{PP} Typical
- Electronic Signature
- 100,000 Program/Erase Cycles and 10 Year Data Retention
- JEDEC Standard Pinouts:
 - 32 pin DIP
 - 32 pin PLCC
 - 32 pin TSOP
- Commercial and Industrial Temperature Ranges

