Enhanced Video Dot Clock Generator

Features

- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Provision for external frequency input
- Excellent power supply rejection
- Small footprint - 20-pin DIP or SOIC

Applications

- Higher Frequency applications
- EGA - VGA - Super VGA-XGA video adapters
- High resolution MAC II displays
- Workstations
- LCD and other flat panel display systems
- 8514A - TMS 34010 - TMS 34020
- Motherboard - PS2™ display systems

Description

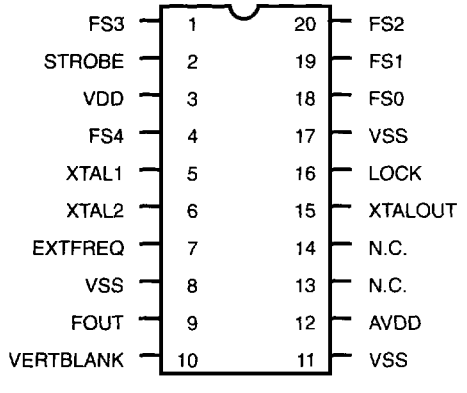
The **ICS1494** Dot Clock Generator is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS1494** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Outputs are compatible with **VGA, EGA, XGA, MCGA, CGA, MDA,** as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single-level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 32 clock rates, the **ICS1494** has provisions to multiplex an externally-generated signal source into the **FOUT** signal path. The **ICS1494** can also be programmed to select the crystal oscillator signal as the **FOUT** output. Internal phase-locked frequencies continue to remain locked at their preset values when these modes are selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes, as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire graphics system.

Features

- 135 MHz Guaranteed Performance
- Fast acquisition of selected frequencies
- Internal loop filter eliminates noise pickup
- Advanced PLL for low phase-jitter
- Improved loop stability over entire frequency range
- Frequency change synchronized to vertical retrace
- Frequency change-detection circuitry enhances new frequency acquisition
- Lock Detect Output
- Buffered XTAL Out

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Notes:

1. In applications where the external frequency input is not specified. EXTFREQ must be tied to VDD.
2. ICS1494M(SOIC) pinout is identical to ICS1494N(DIP).

Circuit and Application Options

The **ICS1494** will typically derive its frequency reference from a series-resonant crystal connected between pins 5 and 6. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into XTAL1. Pin 6 must be left open.

The **ICS1494** is capable of multiplexing an externally generated frequency source of **FOUT** via a mask option, in addition to its internally generated clock.

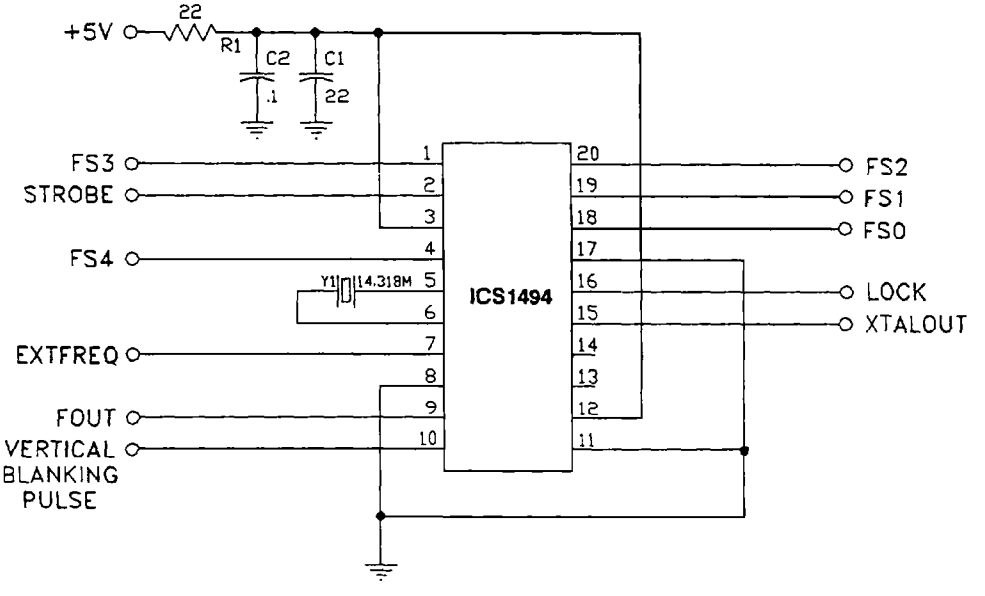
This is input via **EXTFREQ (7)**. When an external source is selected the PLL remains locked to the value specified in the selected address. This provision facilitates the ability to rapidly change frequencies. When this option is not specified in the ROM pattern, pin 7 is internally tied to V_{DD} and should be connected to V_{DD} on the PCB.

Power Supply Conditioning

The **ICS1494** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component. The cost of the discretes used in Figure 2 is less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all V_{DD}s may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS minimized the effect of packaging and minimized the interaction of the digital and analog supply currents.

Figure 1



Applications

Layout Considerations

Utilizing the **ICS1494** in video graphics adapter cards or on PS2 motherboards is simple but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS1494** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital Vss and Vdd connections to permit extended frequency **VCLK** operation to 135 MHz. However, in all cases, all V_{SS} and V_{DD} pins should be connected.

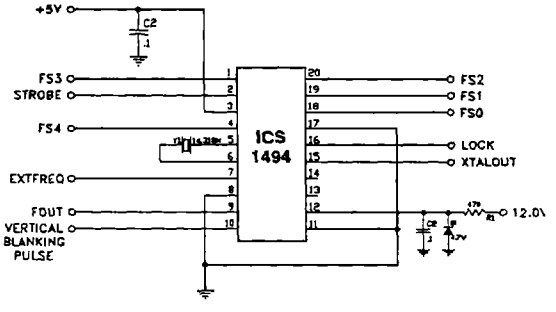


Figure 2

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (5)** and **XTAL2 (6)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10MHz and 25MHz have been tested. Maintain short lead lengths between the crystal and the **ICS1494**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (5)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (5)**, and keep the lead length of the capacitor to **XTAL1 (5)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1494** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (6)** must be left open in this configuration.

LOCK

LOCK(16) is an output signal which may be monitored to indicate when the **ICS1494** has achieved phase lock after a change in frequency has been selected. In systems where it is used, it is tied to an interrupt input to the microprocessor. When high, it indicates phase lock has been achieved.

Buffered XTALOUT

In motherboard applications, it may be desirable to have the **ICS1494** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (15)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **FOUT(9)** and other components in the system should be kept as short as possible. The **ICS1494** outputs have been designed to minimize overshoot. In addition it may be helpful to place a ferrite bead in this signal path to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS1494**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ (7), on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled, signals driving the input will appear at **FOUT(9)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code. **If this option is not specified, pin (7) is connected to VDD internally, and MUST be connected to VDD or left open, not grounded!**

Digital Inputs

FS0 (18), FS1 (19), FS2 (20),FS3(1), and **FS4 (4)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (2)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **VERTBLANK (10)**, when low, inhibits the transfer of new frequency select information. Enabling this pin during the vertical blanking interval causes the change in frequency to happen at this time and prevents any visible glitch when a new frequency is selected. If this feature is not required, this pin may be left open.

Absolute Maximum Ratings

Supply Voltage ..... V_{DD} ..... -0.5V to +7V
Input Voltage..... V_{IN}..... -0.5V to V_{DD}+0.5V
Output Voltage ..... V_{OUT} ..... -0.5V to V_{DD}+0.5V
Clamp Diode Current ..... V_{IK} & I_{OK} . ±30mA
Output Current per Pin ..... I_{OUT} ..... ±50mA
Operating Temperature..... T_o..... 0 °C to 70 °C
Storage Temperature..... T_S..... -85 °C to +150 °C
Power Dissipation..... P_D..... 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0 °C to 70 °C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{dd}	Operating Voltage Range	4.0	5.5	V	
V_{il}	Input Low Voltage	V_{ss}	0.8	V	V_{dd} = 5V
V_{ih}	Input High Voltage	2.0	V_{dd}	V	V_{dd} = 5V
I_{lh}	Input Leakage Current	-	10	uA	V_{in} = V_{cc}
V_{ol}	Output Low Voltage	-	0.4	V	I_{ol} = 4.0 mA
V_{oh}	Output High Voltage	2.4	-	V	I_{oh} = 4.0 mA
I_{dda}	Analog Supply Current	-	5	mA	V_{dd} = 5.0V, FOUT = 25 MHz
I_{dda}	Analog Supply Current	-	7	mA	V_{dd} = 5.0V, FOUT = 110 MHz
I_{ddd}	Digital Supply Current	-	12	mA	V_{dd} = 5.0V, FOUT = 25 MHz
I_{ddd}	Digital Supply Current	-	25	mA	V_{dd} = 5.0V, FOUT = 110 MHz
R_{up} *	Internal Pull-up Resistors	50	200	K Ohm	V_{dd} = 5V, V_{in} = 0V
C_{in}	Input Pin Capacitance	-	8	pF	F_c = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_c = 1 MHz

* The following inputs have pull-ups: FS0-4, STROBE, EXTFREQ, VERTBLANK.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V.
6. Supply Voltage Range = 4.75 to 5.25 Volts
7. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	FOUT TIMING			
Tr	Rise Time	-	3	
Tf	Fall Time	-	3	
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns
	Duty Cycle	40%	60%	110 MHz or less

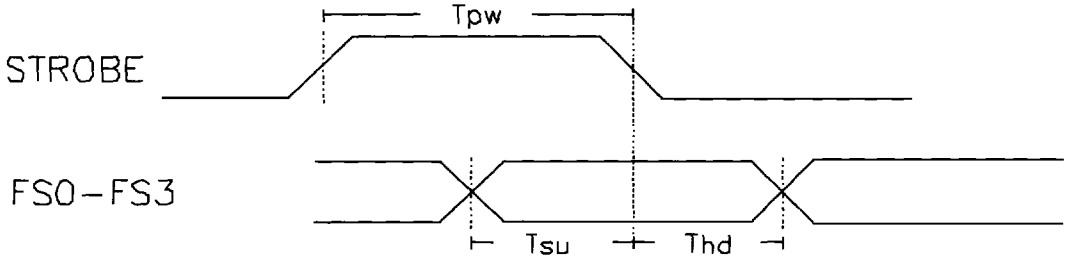


Figure 3

Ordering Information

ICS1494AN-XXX or ICS1494AM-XXX

Example: