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Mosaic
Semiconductor
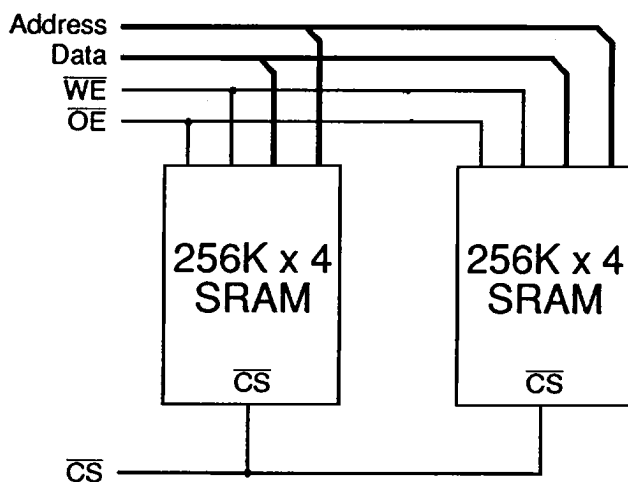Inc.

262,144 x 8 CMOS High Speed Static RAM

Features
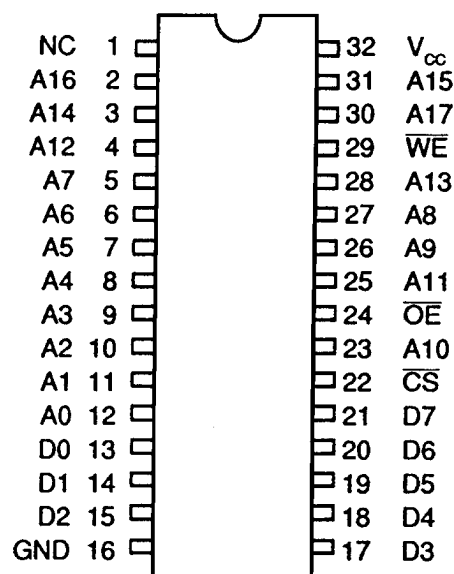
Very Fast Access Times of 25/35/45/55 ns
(25 ns Under Development)
JEDEC Standard 32 pin Footprint
VIL™ High Density Package
Operating Power   1705mW(max.)
Low Power Standby 1.1mW (typ.)-L Version
2.0V Data Retention Mode
Completely Static Operation
Equal Access and Cycle Times
Battery Back-up Capability
Directly TTL Compatible
May be Processed to MIL-STD-883 Method 5004,
non-compliant

Block Diagram

Pin Definition

Package Type - 'V'

NC	1		32	V_{cc}
A16	2		31	A15
A14	3		30	A17
A12	4		29	$\overline{WE}$
A7	5		28	A13
A6	6		27	A8
A5	7		26	A9
A4	8		25	A11
A3	9		24	$\overline{OE}$
A2	10		23	A10
A1	11		22	$\overline{CS}$
A0	12		21	D7
D0	13		20	D6
D1	14		19	D5
D2	15		18	D4
GND	16		17	D3

Pin Functions

A0-A17	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
32	0.1" Vertical-in-LIne (VIL™)	V	Ceramic	JEDEC

Package dimensions and outline are displayed on page 6
VIL is a trademark for Mosaic Semiconductor Inc., US Patent number D316251.

Absolute Maximum Ratings [1]

Voltage on any pin relative to V_{SS} [2]	V_T	-0.5 to +7	V
Power Dissipation	P_T	1.0	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 2.0V for less than 10ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (8256I)
	T_{AM}	-55	-	125	°C (8256M, 8256MB)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-10	-	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	-5	-	5	μA
Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL},$I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	-	310	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}, I/P's static	-	-	80	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	-	20	mA
-L Version	I_{SB2}	As above	-	-	1	mA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	C_{IN}	V_{IN}=0V	-	20	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	20	pF

Note: These parameters are sampled and not 100% tested.

AC Test Conditions　　　　　　　　　　　　Output Load Circuit

* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Diagram
* V_{CC}=5V±10%

I/O Pin

V_{CC}

480Ω

255Ω

30 pF*

* Including scope and jig

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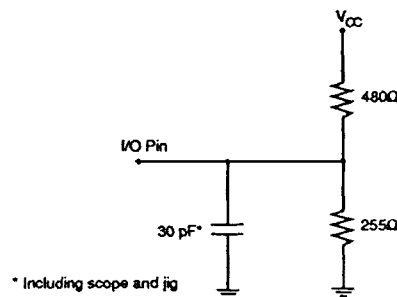
Read Cycle Timing

| Parameter	Symbol	-25 [10] min	max	-35 min	max	-45 min	max	-55 min	max	Unit	Note
Read Cycle Time	t_{RC}	25	-	35	-	45	-	55	-	ns	
Address Access Time	t_{AA}	-	25	-	35	-	45	-	55	ns	
Chip Select Access Time	t_{ACS}	-	25	-	35	-	45	-	55	ns	
Output Enable to Output Valid	t_{OE}	-	12	-	15	-	18	-	15	ns	
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	5	-	ns	1
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	15	0	20	0	18	ns	1
Output Disable to Output in High Z	t_{OHZ}	0	10	0	12	0	18	0	15	ns	1

Read Cycle No. 1 Timing Waveform [1,2]
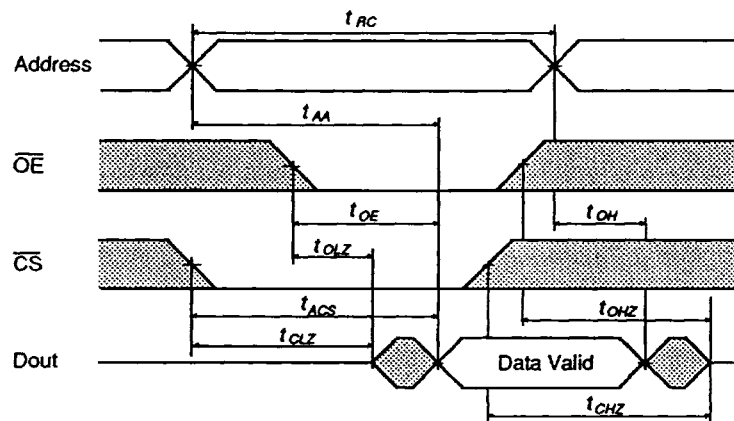
Read Cycle No. 2 Timing Waveform [1,2,3,5]
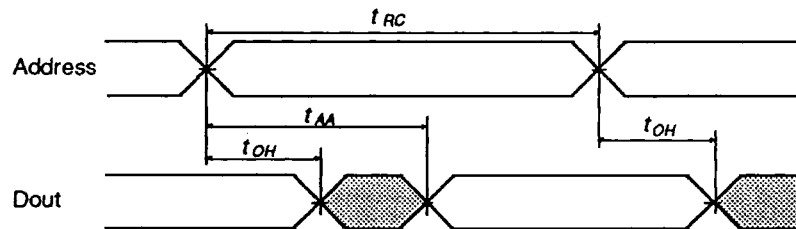
Read Cycle No. 3 Timing Waveform [1,2,4,5]
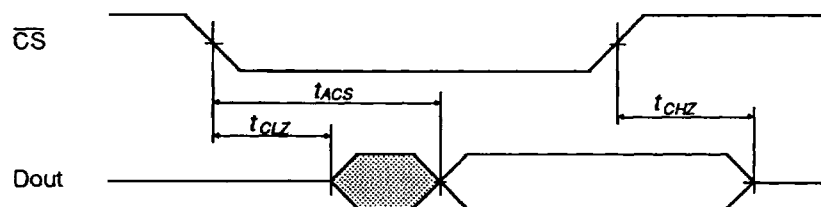
Notes: (1) Transition is measured ±200mV from steady voltage with Load B. This parameter is sampled and not 100% tested.

(2) $\overline{WE}$ is High for Read Cycle.

(3) Device is continuously selected, $\overline{CS}=V_{IL}$.

(4) Address valid prior to or coincident with $\overline{CS}$ transition Low.

(5) $\overline{OE}=V_{IL}$.

(6) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle Timing

Parameter	Symbol	-25 [10] min	-25 [10] max	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit	Notes
Write Cycle Time	t_{WC}	25	-	35	-	45	-	55	-	ns	
Chip Selection to End of Write	t_{CW}	17	-	25	-	25	-	30	-	ns	
Address Valid to End of Write	t_{AW}	20	-	30	-	30	-	30	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	17	-	25	-	25	-	30	-	ns	
Write Recovery Time	t_{WR}	3	-	3	-	3	-	3	-	ns	
Write to Output in High Z	t_{WHZ}	0	15	0	20	0	20	0	20	ns	9
Data to Write Time Overlap	t_{DW}	15	-	20	-	20	-	20	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns	
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	0	10	0	10	ns	9
Output Active from End of Write	t_{OW}	0	-	0	-	0	-	0	-	ns	9

Write Cycle No.1 Timing Waveform
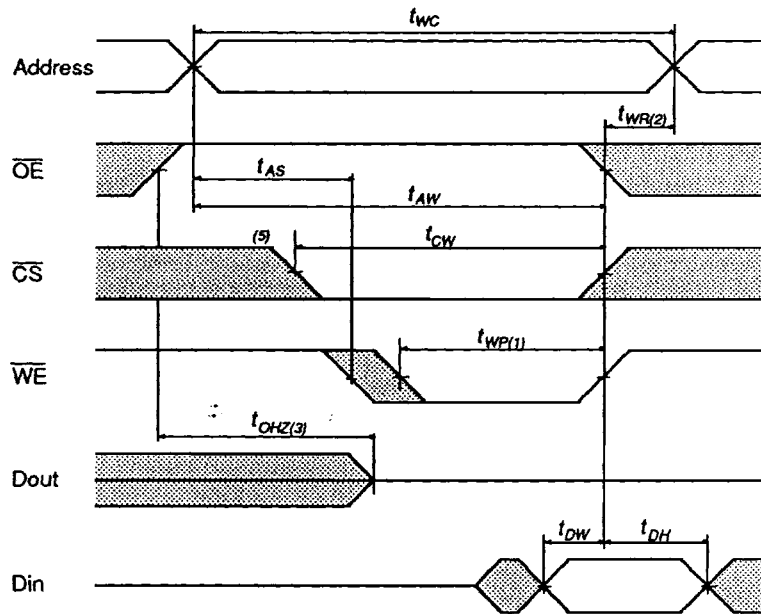
Write Cycle No.2 Timing Waveform [5]
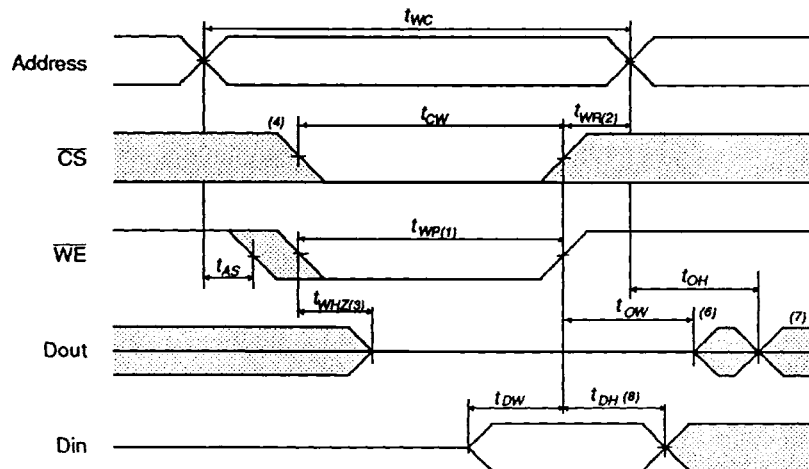
AC Characteristics Notes

Note: (1)   A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3)   During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4)   If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, O/P's remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
(6)   Dout is in the same phase as written data of this write cycle.
(7)   Dout is the read data of next address.
(8)   If $\overline{CS}$ is low during this period, I/O pins are in the output state. I/P signals out of phase must not be applied to I/O pins.
(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
(10)   Under development.

Low V_{cc} Data Retention Characteristics - L Version Only (T_A= -55°C to +125°C)

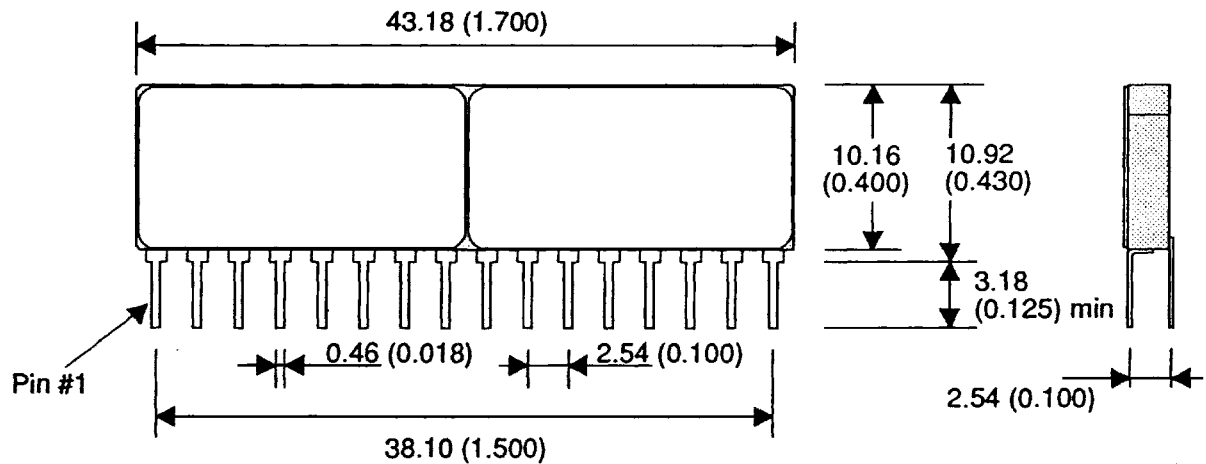| Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{cc} for Data Retention	V_{DR}	$\overline{CS} \geq V_{cc}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{cc}=3.0V, $\overline{CS} \geq V_{cc}$-0.2	-	-	750[2]	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}[1]	-	-	ns

Notes: (1) t_{RC}=Read Cycle Time
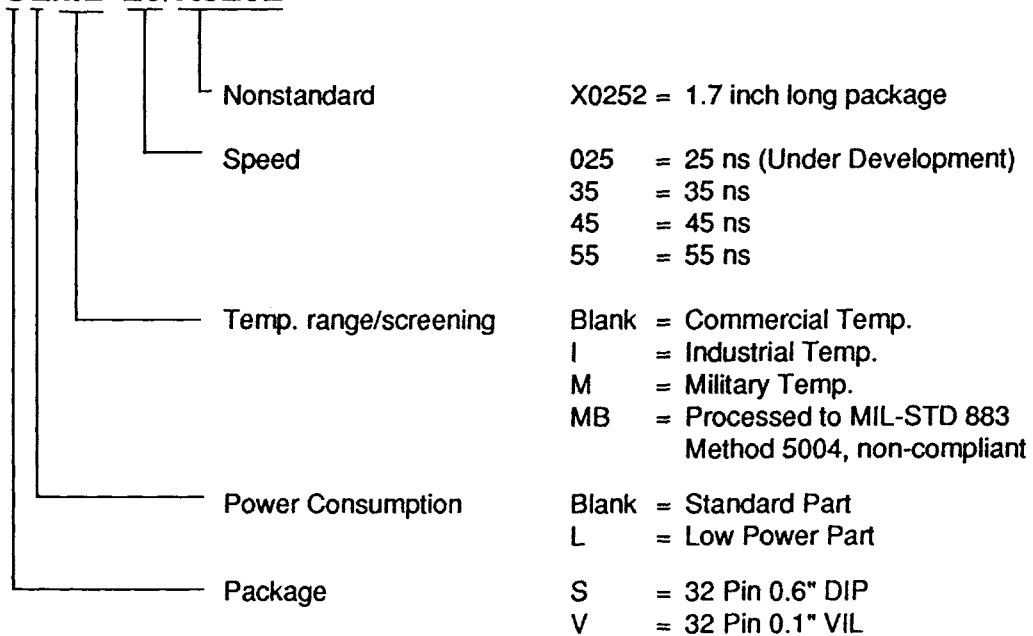(2) V_{cc}=3.0V

Low V_{cc} Data Retention Timing Waveform
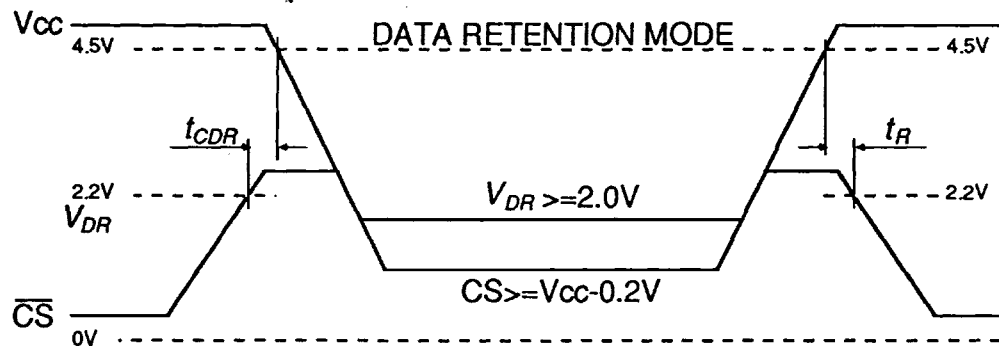
Package Details Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.010)

32 Pin 0.1" Vertical-In-Line (VIL) - ('V' Package)

Ordering Information

MSM8256SLMB-25/X0252

Nonstandard	X0252 = 1.7 inch long package
Speed	025 = 25 ns (Under Development)
	35 = 35 ns
	45 = 45 ns
	55 = 55 ns
Temp. range/screening	Blank = Commercial Temp.
	I = Industrial Temp.
	M = Military Temp.
	MB = Processed to MIL-STD 883 Method 5004, non-compliant
Power Consumption	Blank = Standard Part
	L = Low Power Part
Package	S = 32 Pin 0.6" DIP
	V = 32 Pin 0.1" VIL

Note: For more information regarding screening levels, contact Mosaic Semiconductor Inc. for the 'Screening Level Applications Note.'Ordering Information