2048 x 18: PDM42235
4096 x 18: PDM42245

CMOS High Speed Synchronous FIFOs 2048 x 18-Bit to 4096 x 18-Bit

Features

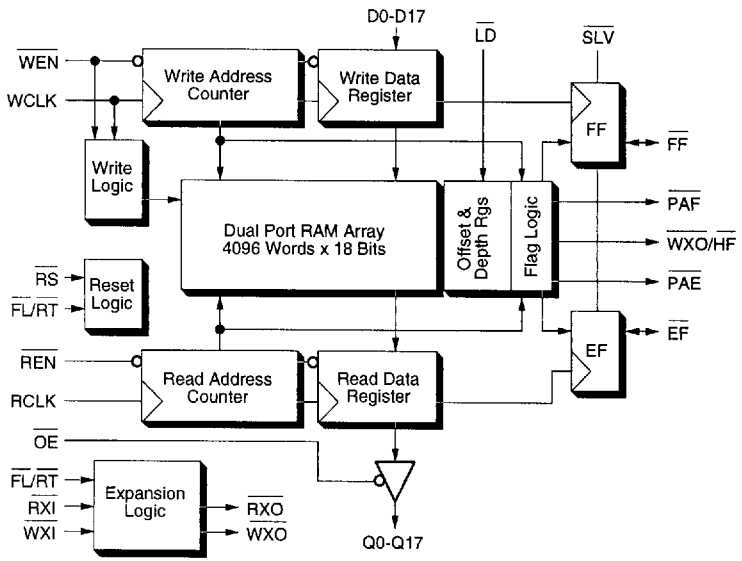
- High speed access times
  Com'l: 10, 15, 20, 25, 30, 35, 50 ns
  Ind: 15, 20, 25, 30, 50 ns
- Clock synchronous interface for high speed
- Independent read and write clocks
- High current outputs for direct bus drive
- Resistor noise damping for clean signals
- Synchronous empty and full flags
- Master/slave controls for expansion
- Synchronous retransmit capability
- Expandable in width and depth
- 10 ns read and write cycle times
- Plug compatible with IDT 72235LB/72245LB

Description

The PDM42235 and PDM42245 are high speed First In First Out (FIFO) buffer memories with clocked read and write interfaces. The PDM42235 and PDM42245 are 2048, 4096 word by 18-bit FIFOs, respectively. The 422X5 series of FIFOs have clocked synchronous (register like) interfaces controlled by read and write enables. Clocked interfaces allow clock cycle times down to 10 ns, much faster than conventional FIFOs, while simplifying designs and improving margins. High current data outputs with noise damping resistors allow direct bus drive with low noise. Synchronous flags solve metastability problems. Programmable Almost Empty ($\overline{PAE}$) and Almost Full ($\overline{PAF}$) flags simplify system designs. Master/slave controls allow width and depth expansion without timing problems or added logic.

The PDM 422x5 is available in a 68 pin PLCC, a 68 pin ceramic and plastic Pin Grid Array (PGA) packages.

Functional Block Diagram



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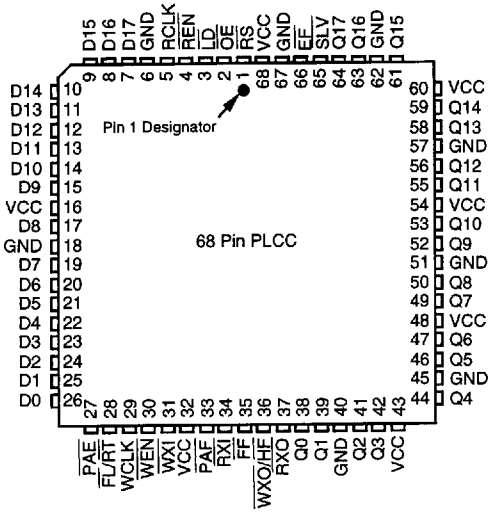
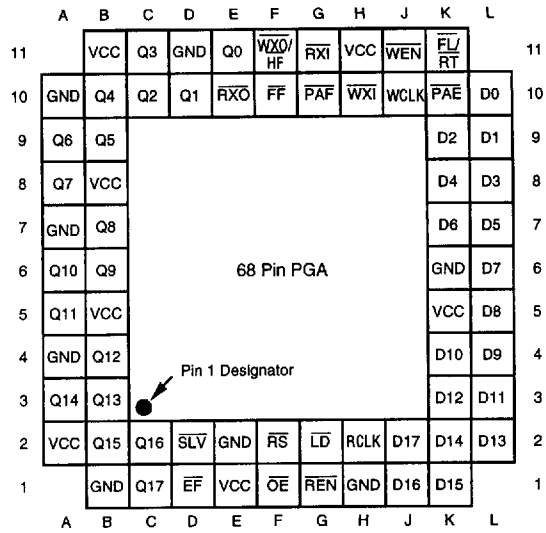
Pin Configuration





Pin Descriptions

Symbol	Name	I/O	Description
D0–D17	Data Inputs	I	Data inputs for a 18 bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{PAF}$ go high. and $\overline{PAE}$ and EF go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when Write Enable $\overline{WEN}$ is asserted (LOW).
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when Read Enable $\overline{REN}$ is asserted (LOW).
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is low, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{WEN}$ and $\overline{LD}$ are LOW, data on the inputs D0-D15 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK. When $\overline{LD}$ and $\overline{REN}$ are LOW, data on the outputs Q0-Q15 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK.
$\overline{FL}$/$\overline{RT}$	First Load/Retransmit	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first devic e (first load device) and set to HIGH for all other devices in the daisy chain. To use the retransmit feature, $\overline{FL}$/$\overline{RT}$ must be HIGH during reset. Retransmit is initiated by taking $\overline{FL}$/$\overline{RT}$ LOW before the rising edge of the read clock and held for one clock edge.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into FIFO. The default offset at reset is 1/8 full.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into FIFO. The default offset at reset is 7/8 full.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
WXO/$\overline{HF}$	Write Expansion Out/ Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to WXI of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from the $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q0-Q17	Data Outputs	O	Data outputs for a 18-bit bus.
VCC	Power		Seven +5 volt power supply pins.
GND	Ground		Eight 0 volt ground pins.

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FIFO Status Flags

Words in FIFO	FF	EF	HF	PAE	PAF
0	H	L	H	L	H
1	H	H	H	L	H
n	H	H	H	L	H
n+1	H	H	H	H	H
N/2	H	H	H	H	H
N/2+1	H	H	L	H	H
N-m-1	H	H	L	H	H
N-m	H	H	L	H	L
N-1	H	H	L	H	L
N	L	H	L	H	L

NOTE: 1. n = Empty Offset Register Value
2. m = Full Offset Register Value
3. N = FIFO Depth: See Table

FIFO Depth & Defaults

FIFO P/N	N	n	m
42235	2048	127	127
42245	4096	127	127

Register Formats

Register	Bit Format		
	17, 16	15-6	5-0
Empty Offset	XX	Offset, n	
Full Offset	XX	Offset, m	
Depth	XX	XXXX	Depth

Register Programming

LD	WEN	REN	WCLK	RCLK	SELECTION
L	L	H	↑	X	Write Register & Advance Reg Counter: 0: Empty Offset 1: Full Offset 2: Depth
L	H	H			Advance Register Counter Only
H	L	H			Write into FIFO
H	H	H			No Operation
L	H	L	X	↑	Read Register & Advance Reg Counter: 0: Empty Offset 1: Full Offset 2: Depth
L	H	H			No Operation
H	H	L			Read from FIFO
H	H	H			No Operation

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-55 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Military	Ambient Temperature	-55	25	125	°C
Commercial	Ambient Temperature	-0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±10%, All Temperature Ranges)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}		-10	10	µA
I_{LO}	Output Leakage Current	V_{CC}= MAX., V_{OUT} = GND to V_{CC}		-10	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		0.4	—	V
V_{OH}	Output High Voltage	I_{OH} = -12mA, V_{CC} = Min.		2.4	—	V
V_{IH}	Input High Voltage		Ind. Com'l.	2.2 2.0	— —	V
V_{IL}	Input Low Voltage[2]			—	0.8	V
I_{OR}	Output Low Drive Current	V_{CC} = Min., V_{OL} = 2.0 Volts		50	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[1]		-60		mA
R_{OUT}	Output Resistance	$\Delta V_{OL}/\Delta I_{OL}$ @ I_O = 12mA	Ind. Com'l.	21 24	38 35	Ω Ω
I_{CC1}	Active Supply Current: Outputs Open	V_{CC}= MAX., f2 = 20 MHz on RCLK & WCLK	Ind. Com'l.	— —	240 190	mA mA
I_{CC2}	Standby Current: Inputs @ V_{CC}-0.2V	V_{CC}= MAX., f2 = 20 MHz on RCLK & WCLK	Ind. Com'l.	— —	75 70	mA mA

NOTE: 1. Not more than one output should be shorted and the duration is ≤ second
2. Undershoots to -1.5V 10 ns are allowed once per cycle

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Capacitance[1] (T_A = +25°C, f=1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	6	pf
C_{OUT}[2]	Output Leakage Current	8	pf

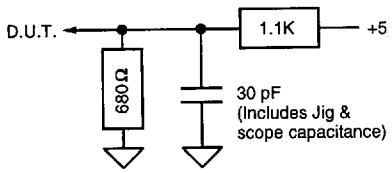
NOTE: 1. Characterized values, not currently tested.
2. With output deselected.

AC Electrical Characteristics (VCC = 5V ± 10%, All temperature Ranges)

Parameter	Symbol	-10	-15	-20	-25	-30	-50	Type	Units
Clock Cycle	t_C	10	15	20	25	30	50	Min	ns
Clock Frequency	f_C	100	66	50	40	33	20	Max	MHz
Clock High/Low	t_W	4	6	8	10	12	20	Min	ns
Clock Data	t_{CD}	2	2	2	2	2	2	Min	ns
		8	9	11	13	15	17	Max	ns
Clock to $\overline{EF}$, $\overline{FF}$	t_{CF}	7	9	11	13	15	17	Max	ns
Clock to $\overline{PAE}$, $\overline{PAF}$	t_{PF}	22	24	25	26	28	30	Max	ns
Clock to $\overline{HF}$	t_{HF}	22	24	25	26	28	30	Max	ns
Output Enable	t_{OE}	7	8	9	12	15	20	Max	ns
$\overline{OE}$ to Output Low Z[1]	t_{LZ}	0	0	0	0	0	0	Min	ns
$\overline{OE}$ to Output Hi Z[1]	t_{HZ}	6	7	8	11	14	19	Max	ns
Setup Time	t_S	3	4	5	5	6	7	Min	ns
Hold Time	t_H	1	1	1	1	1	1	Min	ns
Flag Setup Time (Slave)	t_{FS}	4	5	6	6	7	8	Min	ns
Flag Hold Time (Slave)	t_{FH}	1	1	1	1	1	1	Min	ns
Reset Pulse Width	t_{RS}	10	15	20	25	30	50	Min	ns
Reset Setup	t_{RSS}	7	10	12	15	18	30	Min	ns
Reset Recovery	t_{RSR}	7	10	12	15	18	30	Min	ns
Reset to Flags	t_{RF}	13	15	20	25	30	50	Max	ns
Retransmit to Prog Flags	t_{RTF}	40	45	50	55	60	65	Max	ns
Clock to Expand Out	t_{XO}	6.5	9	12	15	18	30	Max	ns
Exp. In Pulse Width	t_{XI}	3.5	6	8	10	12	20	Min	ns
Exp. In Setup Time	t_{XIS}	4	5	8	10	12	20	Min	ns
Skew to $\overline{FF}$	t_{SK1}	9	10	14	16	18	20	Min	ns
Skew to $\overline{EF}$	t_{SK2}	9	10	14	16	18	20	Min	ns

Notes: 1. Values characterized and guaranteed by design, not currently tested

Output Load



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V

Operational Description

Data is written into the FIFO when write enable ($\overline{WEN}$) is active. On the rising edge of write clock (WCLK), data is clocked into the write data register, an internal write pulse is generated and sent to RAM, data is written into the word selected by the contents of the write address counter, and the write address counter is incremented. The write address counter always points to the next RAM word to be written. A latch is used to hold the write address stable during the write pulse while the write counter is incrementing to the next address.

Internal write pulse generation is called self-timed write, meaning that the write pulse is generated by the chip rather than by external logic. Self-timed write is a significant benefit of synchronous FIFOs because generating short, precise write pulses is difficult in high speed systems.

Data is read from the FIFO when read enable ($\overline{REN}$) is active. On the rising edge of read clock (RCLK) , data from the RAM word selected by the contents of the read address counter is clocked into the read data register, and the read address counter is incremented. The read address counter always points to the next word to be read.

The FIFO is initialized by a reset pulse ($\overline{RS}$) which resets the read and write address counters, sets the Empty flag flip flop and resets the Full flag flip flop.

The flag logic compares the contents of the read and write address counters in conjunction with the read and write enables to generate the empty and full flags. If there is only one unread word in the FIFO and read enable is active, the next read clock will set the Empty flag flip flop ($\overline{EF}$). If there is only one unwritten word in the FIFO and write enable is active, the next write clock will set the Full flag flip flop ($\overline{FF}$).

The Empty flag going invalid indicates that data is available in the FIFO. The read data is brought to the outputs (Q0 - Q17) by activating the read enable line ($\overline{REN}$) and providing a rising edge to the read clock input (RCLK).

The Empty and Full flag flip-flops synchronize the Empty and Full flag outputs to the read and write clocks, respectively. Read data, read enable and the Empty flip flop all change state relative to the rising edge of read clock. Write data, write enable and the Full flag all change state relative to the rising edge of write clock. This provides a clocked (synchronous) interface to the user.

Bus Drive Capability

The 422X5 FIFOs are designed to directly drive high speed buses. The FIFO read outputs are always valid, and the Output Enable ($\overline{OE}$) signal allows read data to be gated onto a data bus. The output drivers have high current drive capability consistent with high speed. Many Vcc and ground pins are used to insure quiet, stable output signal levels.

The FIFO outputs also have built-in 25 ohm noise suppression resistors, allowing these outputs to drive even high capacitance buses at high speeds and with minimum noise. The noise damping resistors suppress both ground bounce and reflection noise, combining the benefits of high speed with clean signals.

Resistor outputs have additional specifications when compared to the older style TTL outputs. Resistor outputs have DC Vol specified at 8 mA at 0.4 volt for the 422X5 series, the same as other vendors' non resistor parts. A new specification, Ior, insures that the outputs have sufficient drive to handle high capacitance loads. It is specified at 50 mA minimum at 2.0 volts for the 422X5 series. It is intended to insure that the outputs consist of a high current driver and a discrete resistor rather than a weak driver. A high current driver with a resistor will handle high capacitance loads with minimal degradation. A weak driver, however, will current limit and slow down significantly under capacitance loading.

Retransmit

The 422X5 FIFOs have a retransmit feature. Retransmit resets the read address counter to zero, allowing a block of data to be reread. Retransmit is initiated by taking the $\overline{FL}/\overline{RT}$ pin low before the rising edge of the read clock and holding it low for one clock edge. The read counter will be reset in the next cycle following the rising edge of the clock, and the flags and data will be valid for address zero at the next read clock edge. The read counter and flags will be valid after the second read clock rising edge.

To use the retransmit feature, the FL/RT pin must be high during reset. This enables the retransmit logic. This allows the FL/RT pin to be tied to ground in systems which do not use the retransmit feature without performing continuous retransmit resets. It also maintains compatibility with other vendors' equivalent FIFOs.

Note that retransmit is not available in the depth expanded mode because the FL/RT pin is used to identify the first device in the depth expansion chain.

Programmable Flags

The 422X5 series synchronous FIFOs have additional flags: Half Full (HF), Programmable Almost Empty (PAE) and Programmable Almost Full (PAF). The HF flag indicates that the FIFO is half full. The PAE and PAF flags indicate that the FIFO is almost empty or almost full, respectively. The PAE flag can be used to indicate that a complete message or data block has been received. The PAF flag can be used to indicate that there is enough room to store one more message or data block. The PAE and PAF flags can simplify the design of a system by providing information about messages or blocks of data being transferred. They can replace logic which would be required to track message word counts.

The PAE and PAF flags use offset values which are programmed into internal registers. The offset values determine when the flags are active. The PAE flag is active when there are N unread words in the FIFO. The value of N is supplied by the Empty Offset register. The PAF flag is active when there are M unwritten words available in the FIFO. The value of M is supplied by the Full Offset register. The offset registers are programmed by writing data into the FIFO through the write port while activating the LD pin. These registers are set to their default to values listed in the depth default tables by the reset pulse.

The HF, PAE and PAF flags are unsynchronized outputs. This allows these outputs to be synchronized to either the read or write clocks, depending on the application. Although the PAE and PAF flags are nominally used to indicate almost empty and almost full, respectively, they could both be programmed to give different levels of almost full or different levels of almost empty, depending on the application.

Operating Configurations

Width Expansion

The 422X5 series FIFOs are easily expanded in width, as shown in the Width Expansion Block Diagram. In this figure, two FIFOs are used to buffer a 36-bit bus. The read and write clocks and read and write enables are paralleled on both FIFOs so that a 36-bit word is written and read.

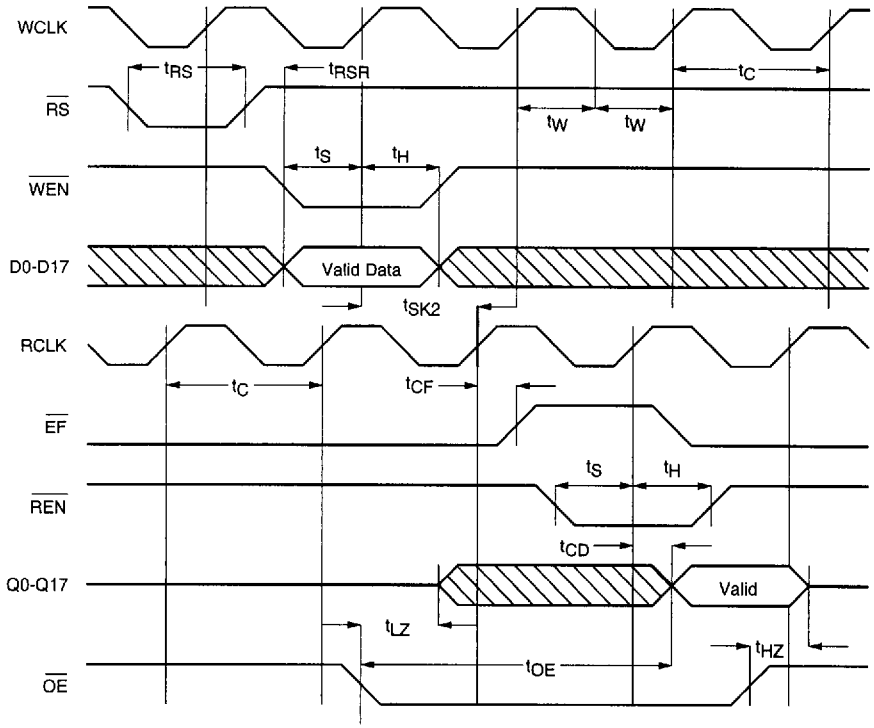
The 422X5 FIFOs solve a potential problem with the Empty and Full flags in width expansion. When a FIFO goes from empty to non-empty, the Empty flag is cleared. This is driven by the write clock, which is asynchronous to the read clock driving the Empty flag flip flop. Since the write clock can occur at any time, it is possible due to minor differences in internal delays and board layout that the Empty flag on one FIFO could clear in one clock period while the Empty flag in the other FIFO would just miss this cycle and not be cleared until the next clock. Since the Empty flag inhibits reading, one FIFO could be read but the other FIFO could not. A traditional solution to this problem is to AND the flags so that both flags must be cleared before reading is allowed. This requires an extra component and an extra delay to feed the signal back to the read enable input.

The 422X5 series provides a better solution. Pin programming is used to define master and slave parts. The SLV pin on the 422X5 series controls the Empty and Full flag output drivers. In the single FIFO and master FIFO case, the SLV pin is high and the output drivers are active. In the slave case, the SLV pin is low and the flag pins serve as inputs. The Empty and Full flags from the master are connected to the corresponding inputs on the slave part(s). The slave part flag inputs gate the enable lines internal to the FIFO in the same manner as normal FIFO operation. The only difference is that only one set of flags from the master FIFO are used to control all FIFOs.

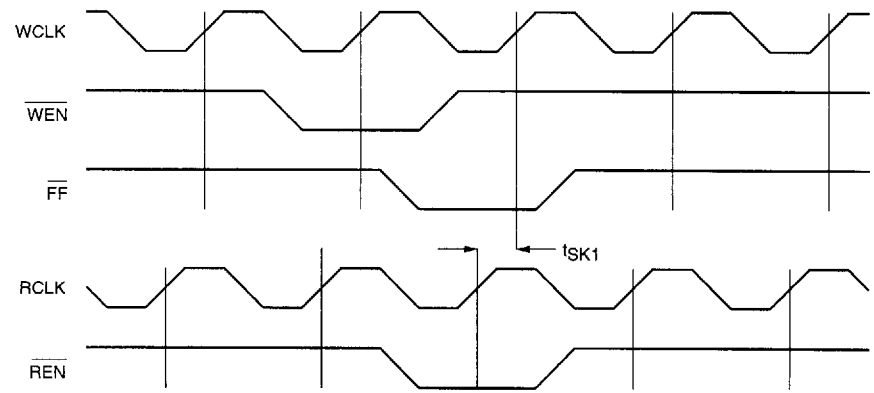
If the master Empty flag is cleared, the slave FIFO is enabled for reading even if its internal Empty flip flop has not been cleared. This condition would occur if the slave internal Empty flip flop had just missed being cleared by the clock while the master Empty FF was cleared. In this case, the data is ready

Timing Diagrams

Read and Write Timing for First Word in FIFO



Read and Write Timing for Last Word in FIFO



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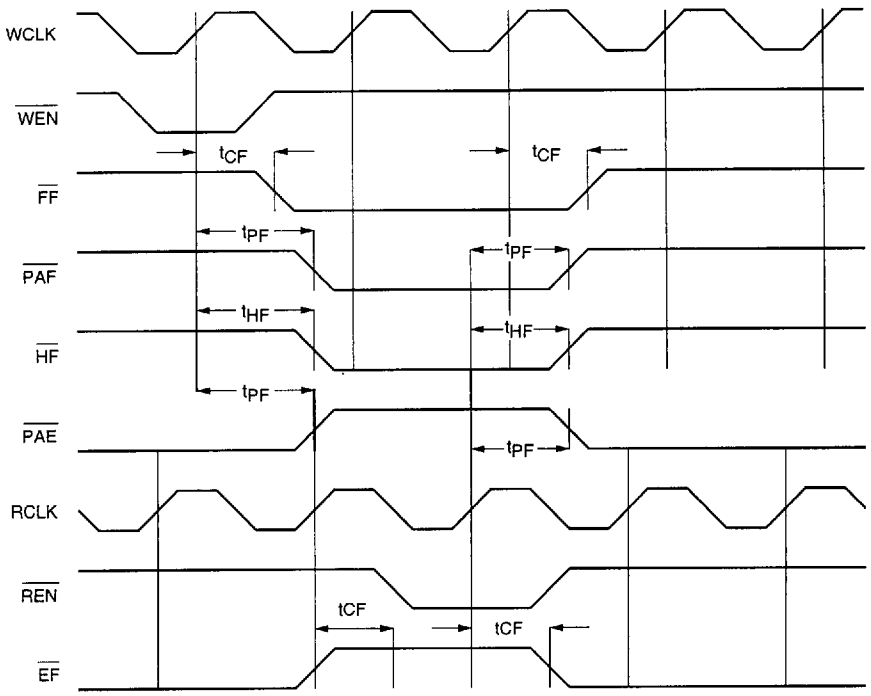
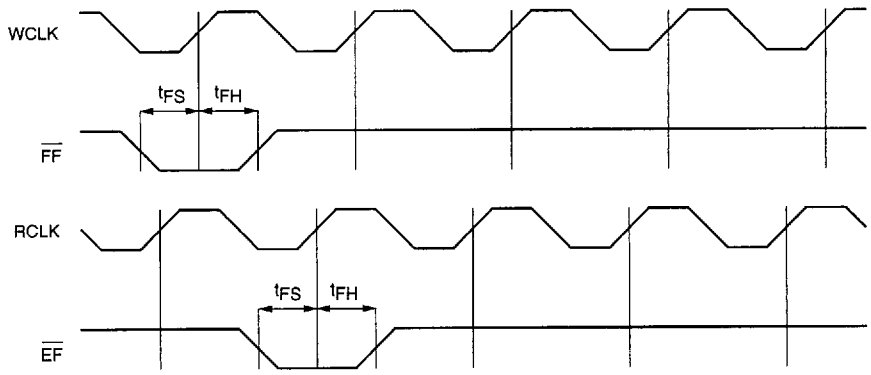
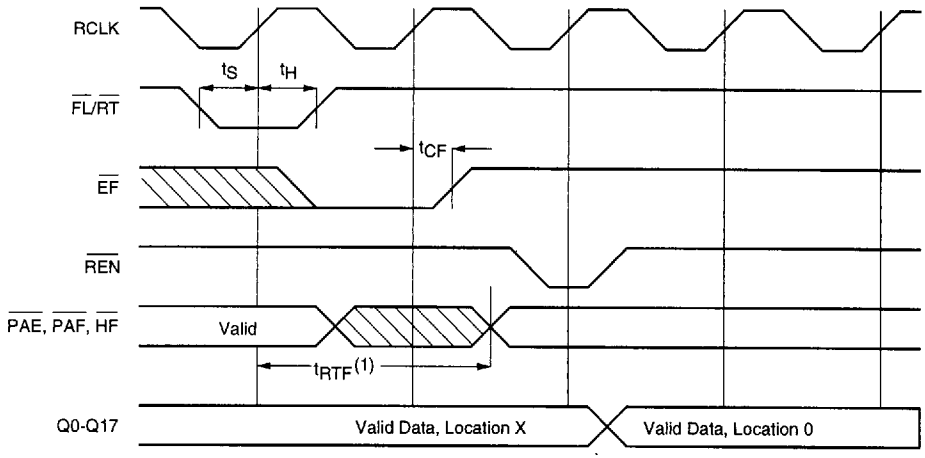
Flag Timing



Slave Flag Timing

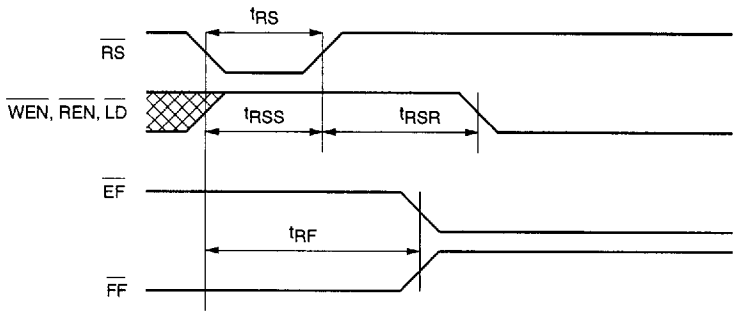


Retransmit Timing

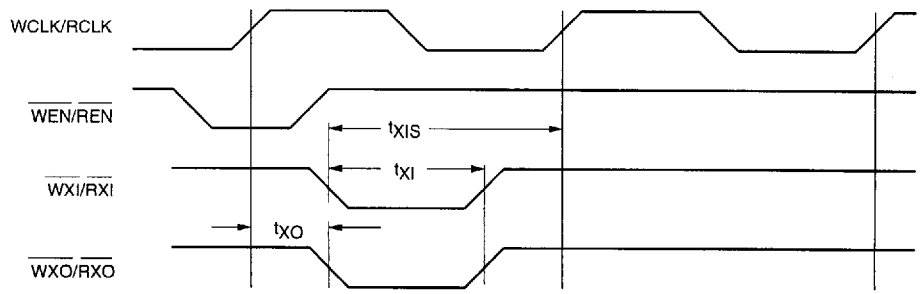


Note: 1. Writing is not allowed during t_{RTF}

Reset Flag Timing



Expansion Timing



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to be clocked out of the slave FIFO RAM because it has had the same amount of time to propagate through the RAM as the data in the master FIFO. Only the internal Empty flag flip flop on the slave part is wrong. Therefore, it is possible to use the master Empty flag to control the slave. If the slave internal Empty flag flip flop was cleared and the master was not, access to the data will be delayed by one cycle, and there is no timing problem here either.

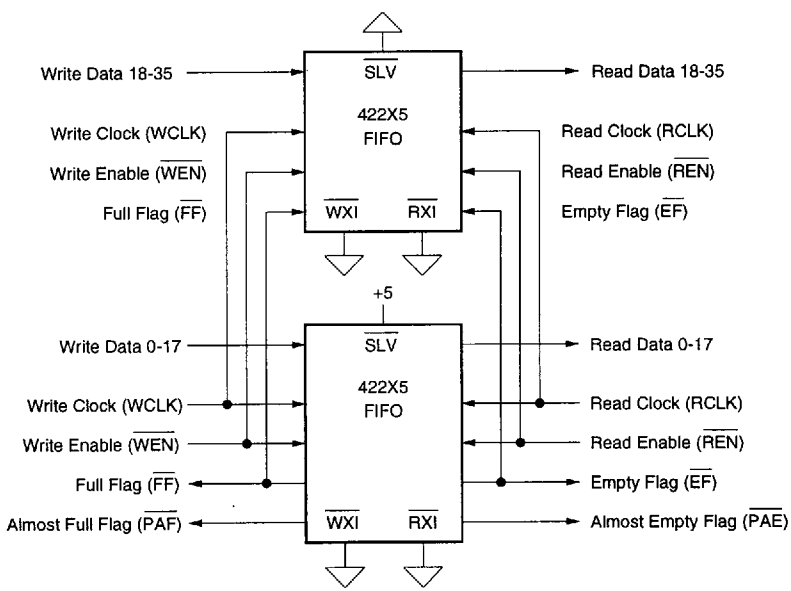
The master and slave situation for the Full flag is similar to the Empty flag. The Full flag from the master is used to control the Full flag inputs for the slave in the same manner.

Note that there is no problem with the transition from non empty to empty or non full to full. Empty is made active by the read clock, as enabled by read enable. If the required read enable setup time is met for both the master and slave FIFOs, both the master and the internal slave Empty flip flops will always be set at the same time. This is also true for the Full flags.

Depth Expansion

Some designs require FIFO buffers larger than can be provided by a single FIFO. The 422X5 FIFO series provides controls which allow FIFOs to be combined for greater depth. This is called depth expansion. FIFOs can be expanded in depth up to 32K words without external logic. This corresponds to eight 4Kx18 FIFOs. The Depth Expansion Block Diagram shows three 42245 4Kx18 FIFOs connected to form a 12Kx18 FIFO.

Depth expansion is implemented by running the FIFOs in parallel with a circulating enable bit for read and write. One FIFO is designated as the First FIFO by grounding the $\overline{FL}$ pin during reset. This pin is typically tied permanently to ground. This FIFO is used to generate the flag signals. The other FIFOs are designated second, etc. by having their $\overline{FL}$ pins tied high during reset. The $\overline{RXI}$ and $\overline{RXO}$ pins are used to propagate the read expansion pulse, and the $\overline{WXI}$ and $\overline{WXO}$ pins are used to propagate the write expansion pulse. The FIFOs are arranged electrically in a ring, with $\overline{RXO}$ connected to $\overline{RXI}$ and $\overline{WXO}$ connected to $\overline{WXI}$, as shown in the Depth

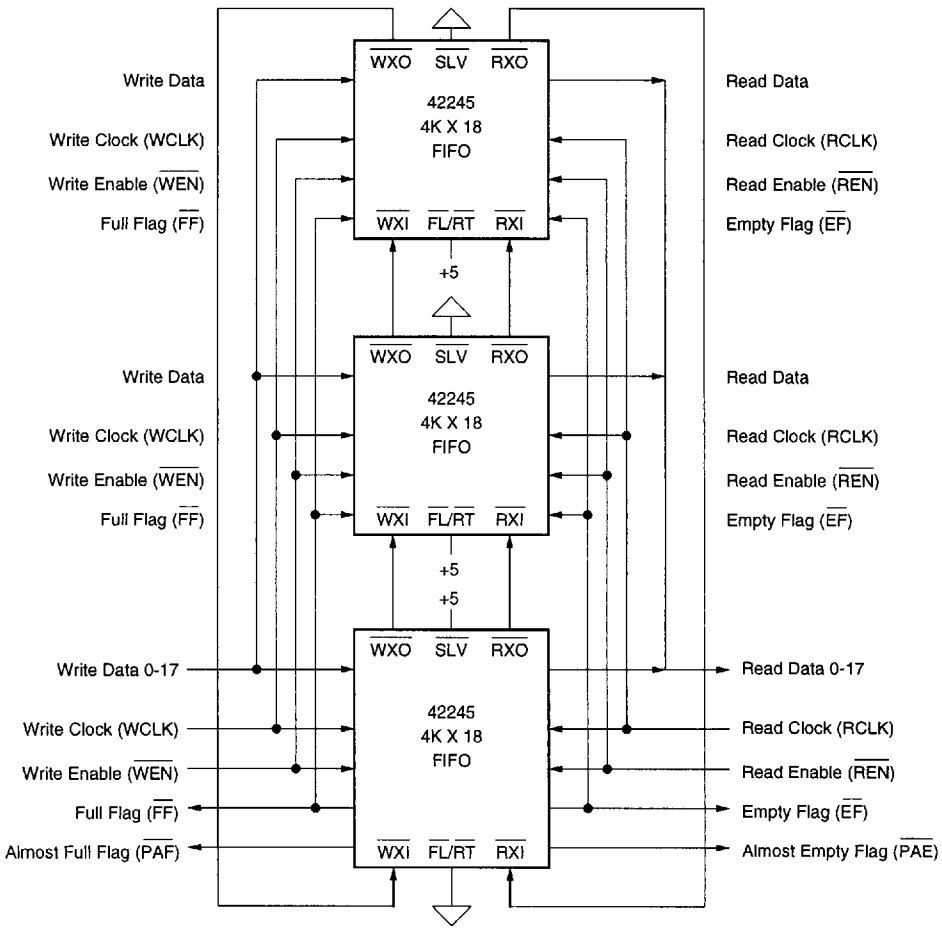


Width Expansion Block Diagram

Expansion Block Diagram. The clocks, enables, flags and data pins are connected in parallel. The flags on the second, etc. devices are disabled by tying the $\overline{SLV}$ pin low, making them slave devices.

Writing starts with the first FIFO. When the last location in the first FIFO is being written, its $\overline{WXO}$ pin goes low. On the rising edge of the next write clock, writing is enabled in the second FIFO and inhibited in the first FIFO. When the second FIFO is full, it propagates a pulse to the third FIFO, etc. This continues around the ring to the first FIFO again, assuming that reading has occurred so that the composite FIFO is not full. Read operations are similar, with a pulse propagating from $\overline{RXO}$ of the first FIFO to $\overline{RXI}$ of the second FIFO, etc. when all the words in the first FIFO has been read.

The depth expansion pulse sets an enable latch in the FIFO it enters. All FIFO address counters operate in parallel. All the read counters contain the same value, and all the write counters contain the same value. The read depth expansion enable latch determines whether its FIFO outputs will be enabled, and the write depth expansion latch determines whether its FIFO RAM will be written. In the First FIFO, the $\overline{FL}$ pin is low during reset which sets both read and write depth expansion enable latches. In the other FIFOs, the $\overline{FL}$ pin is high during reset which clears their depth expansion latches.



Depth Expansion Block Diagram

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The first FIFO generates the Empty and Full flags for the composite FIFOs. The first FIFO is the master with active flag outputs, and the other FIFOs are slaves with their flag pins as inputs. The master and slave configuration solves flag timing problems for depth expansion in the same manner as it does for width expansion. Since the first FIFO generates the Empty and Full flags, the other FIFOs must use these flags rather than their internal flag flip flops to avoid synchronization problems.

The HF flag shares the same pin as the WXO signal. As a result, the HF flag is not available in the depth expansion mode.

Single FIFO (Depth not Expanded)

The 422X5 series FIFOs may be expanded in depth, but are most often used as single, stand alone FIFOs. To operate as a single FIFO or as a bank of single FIFOs in the width expansion mode, the RXI and WXI pins are grounded.

Offset and Depth Register Programming

There are three programmable registers in the 422X5 series FIFOs: the Empty and Full Offset registers, and the Depth register. The Empty and Full Offset registers are 16-bit registers which define the distance from Empty and Full for the PAE and PAF flags, respectively. The Depth register is a 6-bit register which defines the total number of FIFOs in the depth expansion ring for the case of depth expanded FIFOs so that the flags operate correctly. The Empty and Full Offset registers are set at reset to default values shown in the default tables, and the Depth register defaults to a single FIFO.

The Offset and Depth registers are programmed by writing data into the FIFO through the write port while activating the LD and WEN pins. This is shown in the Offset and Depth Register Programming Table. These three registers are written in a rotating sequence. The first write following a reset loads a value into the Empty Offset register; the second write loads a value into the Full Offset register; the third write loads a value into the Depth register. A fourth write would write new data into the Empty Offset register again, etc. If the LD pin is held low with the WEN pin high, the register counter advances to the next register without writing data into the register. This can be used to select one of the registers for writing while leaving the other registers unmodified.

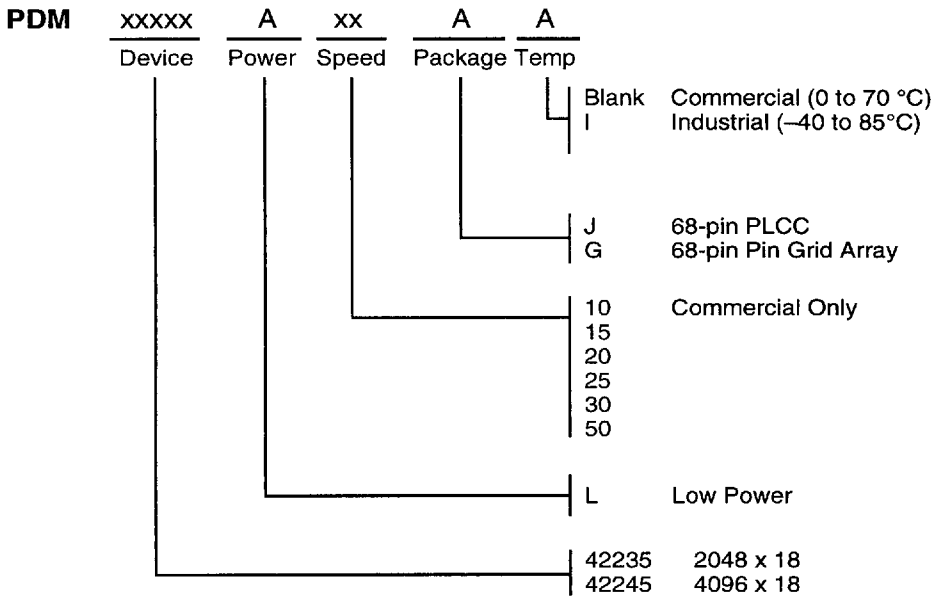
The contents of the Offset and Depth registers can be read by activating LD and REN. Activating LD and REN causes the contents of the selected register to be clocked to the output on the rising edge of the read clock. The LD and REN pins work in the same manner as LD and WEN, as described above except that the counter does not increment when LD is low and REN is high.

The contents of the Empty Offset register determines when the PAE flag goes active. If the Empty Offset register has a value of 120, the PAE flag will be active low when there are less than 120 words in the FIFO and will go high when there are 120 words (or more) in the FIFO.

The contents of the Full Offset register determines when the PAF flag goes active. If the Full Offset register has a value of 15, the PAF flag will be active low if there are 15 locations or less available in the FIFO and will go high if there are 16 or more words available in the FIFO.

The contents of the Depth register tells the flag logic how many FIFOs are connected in a depth expansion ring. This is a number between 0 and 63. If the value is zero or one, a single FIFO is indicated (no depth expansion). Zero is the default value loaded into the Depth register at reset. Values of 2 through 63 indicate the number of FIFOs in the depth expansion ring. For the three FIFO depth expansion example shown in the Depth Expansion Block Diagram, the Depth register value would be three. The Depth register and associated logic assume that all depth expansion FIFOs are the same depth. Depth expansion is limited to 32K words for depth expansion without external logic. A depth expansion ring is therefore limited to eight 4K FIFOs, 32 1K FIFOs, etc.

Ordering Information



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