SC2451
High Efficiency Dual Synchronous DC/DC Controller With Current Sharing Circuitry

Description

The SC2451 is a versatile 2 phase, synchronous, voltage mode PWM controller that may be used in two distinct ways from input supply range 4.5V to 30V. First, the SC2451 is ideal for applications where point of use output power exceeds any single output power budget. Alternatively, the SC2451 can be used as a dual switcher.

The SC2451 features a temperature compensated voltage reference, hiccup or shutdown mode of over current protection, internal level-shifted drive circuitry, programmable operating frequency up to 1.2MHz, soft start and SYNC functions.

SC2451 implements an asynchronous soft start mode, which keeps the lower side Mosfet off during soft start, a desired feature when a converter turns on to a preset external voltage or pre-bias voltage. With the lower Mosfet off, the external bus is not discharged, preventing any disturbances in the start-up slope and any latch-up of modern day ASIC circuits.

In a current sharing configuration, the SC2451 can produce a single output voltage from two separate voltage sources while maintaining current sharing between the channels. Current sharing is programmable to allow the loading of each input supply as required by the application.

In a dual switcher configuration, two feedback paths are provided for independent control of the separate outputs. The two switchers are 180° out of phase to minimize input and output ripple. Also a controlled output sequencing (Output1 first followed by Output2) ensures an orderly start-up.

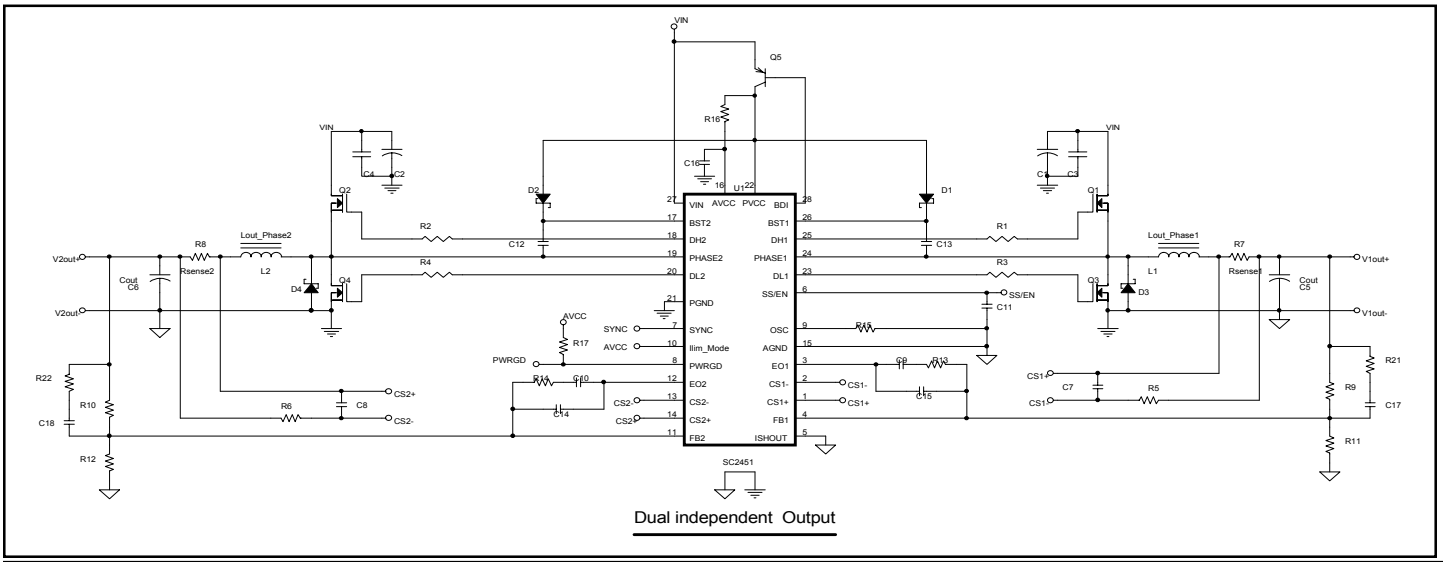
Features

- BICMOS Two phase current share or dual independent voltage mode PWM controller
- Out of phase operation to reduce input and output ripple
- Controlled sequencing (Output1 followed by Output2)
- 4.5V to 30V input voltage range
- Output voltages as low as 0.5V
- Programmable operating frequency up to 1.2MHz
- Soft start
- Hiccup or shutdown over current protection
- High efficiency synchronous switching
- 0% to 100% Duty cycle range (250ns minimum off time, Dmax 70% at 1.2MHz)
- Thermal shut down
- 2A Peak current driver
- Asynchronous start-up (during soft start)
- SYNC (oscillator synchronizes to an external clock)
- -40 to 105°C operating temperature
- 28 pin TSSOP Package

Applications

- Distributed power system
- Internet/network servers
- Point of use low voltage high current applications
- RF power supply
- Local microprocessor core power supplies
- Large memory arrays

Typical Application Circuit



Dual independent Output

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage to PGND	VIN	-0.3 to 35	V
BDI		-0.3 to 33	V
PVCC, AVCC, PWRGD, SS/EN, FB1, FB2 to PGND		-0.3 to 7	V
Inputs (CS+, CS-, FB, Ilim_mode, SYNC)		-0.3 to 7	V
PGND to AGND		+/-300	mV
DL1, DL2 to PGND		-0.3 to PVCC + 0.3V	V
BST1, BST2, PHASE1, PHASE2 to PGND		-0.3 to +35	V
DH1 to PHASE1, DH2 to PHASE2		-0.3 to PVCC + 0.3V	V
PHASE1 to BST1, PHASE2 to BST2		-6 to 0.3	V
Continuous Peak Output Drivers Currents (DL1,DL2,DH1,DH2)		+/-2.00	A
Thermal Resistance Junction to Case	JC	12.6	°C/W
Thermal Resistance Junction to Ambient	JA	36.6	°C/W
Ambient Temperature Range	TA	-40 to 105	°C
Junction Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	°C

All voltages with respect to AGND. Positive currents are into, and negative currents are out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Data sheet for thermal limitations and considerations of packages.

Electrical Characteristics

Unless otherwise specified, VIN = 12V, Rosc = 41.8kΩ, Fosc = Fphase1 = Fphase2 = 250kHz, 0mV < (CS(+) - CS(-)) < 60mV T_A = -40°C to 105°C, T_A = TJ

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
VIN		4.5		30	V
Operating Current	No load		11		mA
AVCC	VIN > 5.5V	5.4	6	6.6	V
PVCC	VIN > 5.5V	5.4	6	6.6	V
Undervoltage Lockout					
Start Threshold		4.312	4.4	4.488	V
UVLO Hysteresis			0.1		V
Error Amplifier					
Feedback Voltage		0.49	0.5	0.51	V
Input Bias Current				200	nA
Input Offset Voltage				5	mV
Open Loop Gain		90			dB
Unity Gain Bandwidth			3		MHz
Output Sink Current			2		mA
Output Source Current			2		mA
Slew Rate			1		V/µS
Oscillator					
Initial Accuracy	T_A = 25°C, RT = 21kohms	450	500	550	kHz
Voltage Stability	T_A = 25°C, RT = 21kohms		1		%
Total Variation	Line, Temperature, RT = 21kohms		10		kHz
Maximum Operation Frequency			1200		kHz
Oscillator Max Duty Cycle		95			%
Ramp Peak to Valley		1.3	1.5	1.7	V
Ramp Peak Voltage			2.0	2.15	V
Ramp Valley Voltage		0.45	0.5		V

Notes:
(1). Guaranteed by design.

Electrical Characteristics (Cont.)

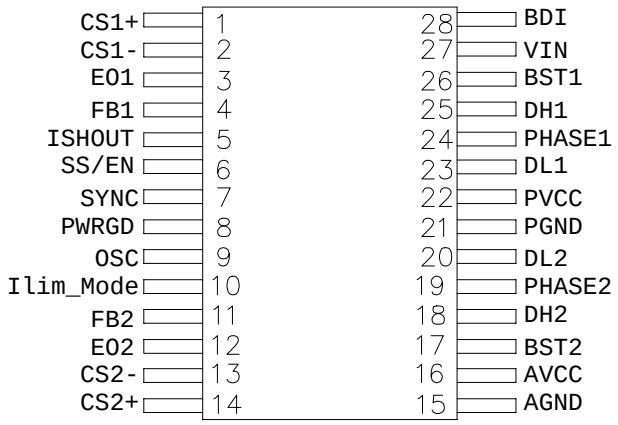
Unless otherwise specified, VIN = 12V, Rosc = 41.8kΩ, Fosc = Fphase1 = Fphase2 = 250kHz, 0mV < (CS(+) - CS(-)) < 60mV T_A = -40 °C to 105 °C, T_A = TJ

Parameter	Test Conditions	Min	Typ	Max	Unit
Sync/CLOCK					
Clock SYNC Threshold			1.0		V
Sync Frequency Range				F_{osc}*1.3	KHz
Current Limit					
Current Limit Voltage		60	70	80	mV
Current Sense Common Mode Voltage	CS+, and CS- to SGND		5		V
Fold Back Current	V_{OUT} = 0V		50%		I_{LIM}
Fold Back Voltage Knee	$I = I_{LIM}$			V_{OUT}	V
Input Bias Current	CS+1, CS-1 CS+2, CS-2			1	µA
SS/EN					
Shut Down Threshold		600			mV
Soft Start Charge Current			5		µA
Soft Start Enable			TBD		V
Power Good					
Power Good Window			±10		$\%V_{OUT}$
Gate Drive					
DL Sink Current	DL - PGND = 3.5V, COUT = 4.7nF	2			A
DL Source Current	PVCC - DL = 5V, COUT = 4.7nF	2			A
DH Sink Current	DH - PGND = 3.5V, COUT = 4.7nF	2			A
DH Source Current	BST - DH = 5V, COUT = 4.7nF	2			A
Dead Time			50		ns
Output Rise Time	Vgs = 3.3V, COUT = 4.7nF		16		ns
Output Fall Time	Vgs = 3.3V, COUT = 4.7nF		16		ns
Minimum Non-Overlap (1)			50		ns
Thermal Shut Down					
Shut Down Temperature	T_J		160		°C
Hysteresis			10		°C

Note:
(1). Guaranteed by design.

Pin Configuration

Top View



(28 Pin TSSOP)

Ordering Information

Part Number	Package(1)	Temp. Range (T_A)
SC2451ITSTR	TSSOP-28	-40°C to +105°C

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

VIN :

Input supply ranging from 4.5V to 30V.

AVCC :

Chip Analog circuitry supply voltage should be bypassed with a decoupling capacitor (70 to 100 mohms ESR) in parallel to a 1uF ceramic capacitor to AGND. AVCC is internally regulated from the external supply connected to VIN. If Vin is below 6.5V , the supply could be directly connected to the AVCC pin.

PVCC :

Supply for the output MOSFETs gate drive.

AGND :

Analog signal ground. SC2451 sensitive internal circuitry are referenced to AGND.

PGND :

Power GND. Return of gate drive currents.

EO1 :

Error Amplifier 1 output. A compensation network is connected from this pin to FB1. In current sharing operation, a resistor is also connected between EO1 and EO2.

EO2 :

Error Amplifier 2 output. A compensation network is connected from this pin to FB2. In current sharing operation, no compensation network is required and a resistor is connected between EO1 and EO2.

FB1 :

Feedback pin used to sense the output voltage via a resistive divider.

FB2 :

Feedback pin used to sense the output voltage via a resistive divider. By connecting this pin to AVCC, the device will be operating in the current sharing mode.

CS-1, CS-2 :

Current limit amplifiers negative inputs for the two channels. CS-1, and CS-2 are connected via a current limit programing resistor to the output side of the inductor current sense resistors.

The current limit programing resistor in conjunction with an internal current source (approximately equal to Iosc), programs the current limit threshold. Once the voltage drop (approximately 70mV) across the current sense resistor is larger than the drop across the programming resistor, current limit condition occurs, and the Shutdown or hiccup current limit protection is activated.

CS+1, CS+2 :

Current limit amplifiers positive inputs for the two channels. CS+1, and CS+2 are connected to inductor side of the inductor current sense resistors. A resistor equal to the current limit threshold resistor (connected to CS- pins) should be also connected in series with the CS+ pins.

BDI :

Base drive for the AVCC/PVCC regulator, a 2.7kohms resistor is recommended to be connected in series from BDI pin to the Base of the external drop out transistor.

PHASE1, PHASE2 :

The return path for the high side gate drive, also used to sense the voltage at the phase node for adaptive gate drive protection.

BST1, BST2 :

BST signal. Supply for high side driver; can be directly connected to an external supply or to a bootstrap circuit.

DH1, DH2 :

DH signal (Drive High). Gate drive for top MOSFETs; requires a small series resistor.

DL1, DL2 :

DL signal (Drive Low). Gate drive for Bottom MOSFETs; requires a small series resistor.

SS/ENA :

Soft start pin. Internal current source connected to external capacitor will determine the softstart duration. Inhibits the chip if pulled down.

PWRGD :

Open collector power good signal. Pulled low if output voltage are outside the power good window. A pull up resistor to an external supply is usually connected to PWRGD.

OSC :

Oscillator Frequency set pin. The peak voltage at this pin will be approximately equal to the bandgap voltage of 1.225V. An external resistor to AGND will program the oscillator frequency. The formula below can be used to approximate the Oscillator Frequency:

Iosc = Bandgap Voltage/Rosc

$Fosc = 1.225V/(Rosc)*(117*10^{-12})$

Fosc = Fphase1 = Fphase2

Pin Descriptions (Cont.)

SYNC :

Synchronization Input pin. An external clock signal connected to this pin will synchronize the internal oscillator to the external frequency. Also can be connected to a multi phase clock generator (SC4201) when multiple SC2451 are used in Multi Phase configuration.

ISHOUT :

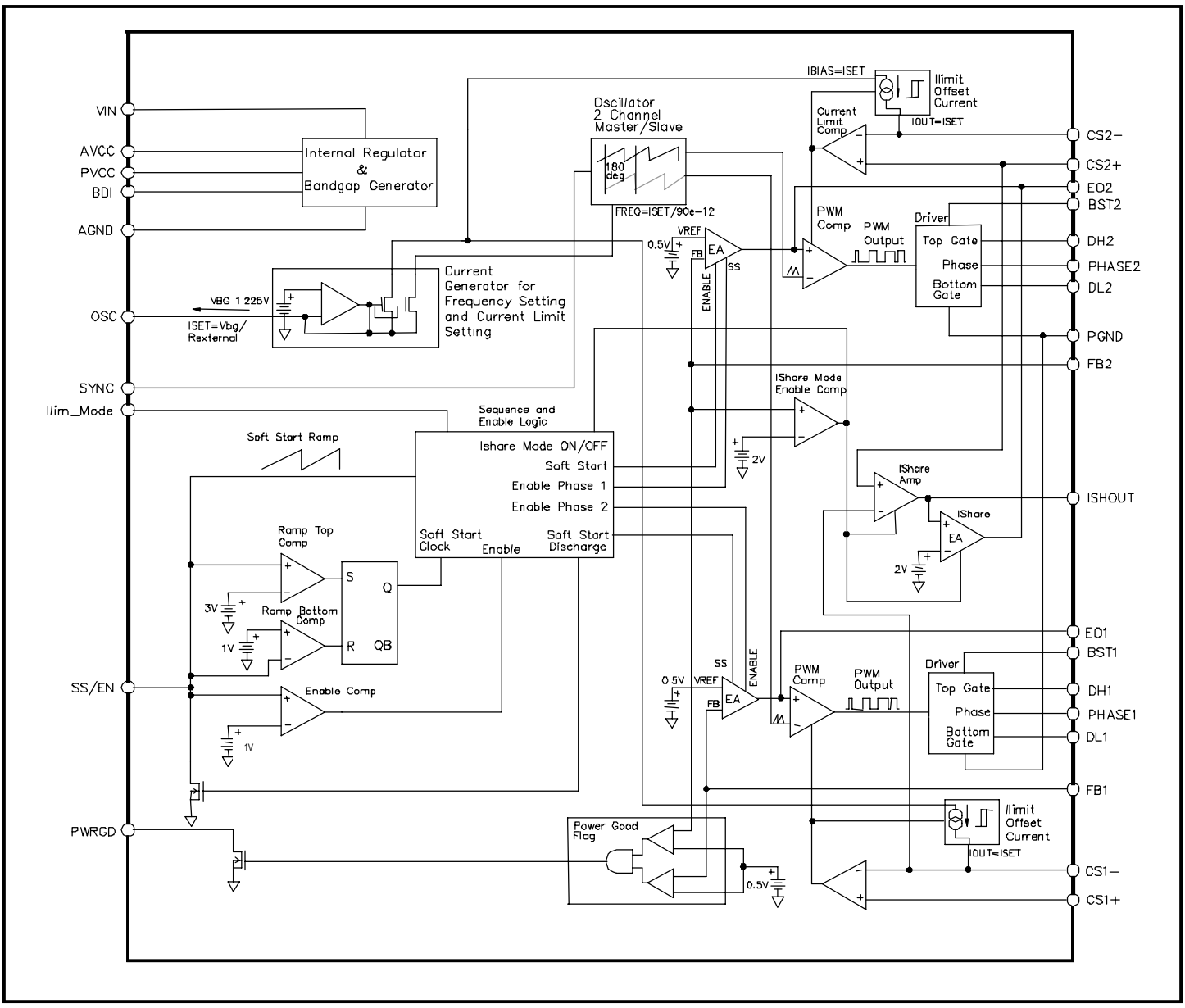
This pin is used in the Current Sharing mode. A 0.1uF capacitor is connected from this pin to AGND. In an independent mode of operation this pin should be connected to the AGND.

Ilim_Mode :

In the shut down current limit (ILIM_MODE pin pulled low to AGND), if OUT1 has a continuous fault , both OUT1 and OUT2 will be latched off. If a fault condition occurs only at OUTPUT2, it will be latched off while OUTPUT1 continues normal operation.

In the hiccup current limit (ILIM_MODE pin pulled high to AVCC), when the current limit has been triggered for a minimum of 16 (maximum of 31) clock pulses (at the switching frequency) the output is disabled for the duration of 7 dummy soft start cycles and the output is then restarted. This sequence repeats indefinitely until the over current condition is removed.

Block Diagram



Marking Information

Top Mark

yyww = Datecode (Example: 9912)
xxxxxx = Semtech Lot # (Example: 90101)

Application Information

Introduction

The SC2451 is a versatile 2 phase synchronous, voltage mode PWM controller with an input supply ranging 4.5V to 30V that may be used in two distinct ways.

The SC2451 can be configured as a dual converter or a bi-phase converter capable of driving N-channel MOSFETs for phase currents beyond 20A in high current applications.

The power dissipation is controlled using a novel low voltage supply technique, allowing high speed and integration with the high drive currents to ensure low MOSFET switching loss. The synchronous buck configuration also allows converter sinking current from load without losing output regulation.

Load current sharing within 10% typical can be achieved between phases by using precise feedback voltage divider resistors (typically 0.1%) to match individual phase output voltage in conjunction with the current share circuitry provided by the SC2451.

The internal reference is trimmed to 500mV with ± 2% accuracy, and the outputs voltages can be adjusted by two external resistors.

A fixed oscillator frequency (up to 1.2MHz) can be programmed by an external resistor. In bi-phase operation, the dual switching regulators are operated 180° out of phase. The oscillator can also be synchronized to an external reference clock for noise sensitive applications.

Other features of the SC2451 include:

Controlled output sequencing, wide operating voltage range (4.5V to 30V), low output voltages down to 500mV, softstart, hiccup or shut down over current protection, wide duty cycle range (0% to 100%), thermal shutdown, asynchronous start-up, and a -40 to 105 °C operating temperature range.

THEORY OF OPERATION

SUPPLIES

Three pins (Vin, AVCC, and PVCC) are used to power up the SC2451. A supply connected to the Vin pin is initially used to provide the base drive to the BDI pin to regulate the VCC. This supply should be by passed with a low ESR ceramic capacitor right at the IC.

The AVCC supply provides the bias for the Internal Reference, Oscillator, and control circuitry. This supply should be bypassed with a low ESR (70 to 100 mohms) tantalum or similar capacitor, and a 1uF ceramic capacitor directly at the AVCC to AGND pins of the SC2451.

The PVCC supply provides the bias for the low and the high side Mosfet gate drive. A low ESR capacitor directly at the PVCC to PGND pins of the SC2451 should be used to bypass the PVCC supply.

If an input supply greater than 6.5V will be used, BDI provides an on board drop out regulator control to an external PNP pass transistor that can be used to generate the AVCC and PVCC supplies.

The maximum rating for VCC supplies is 7V and for applications where input supply is below 6.5V, it may be connected directly to AVCC and PVCC, leaving the BDI pin open.

START UP SEQUENCE

Initially during the power up (VCC<4.4V), the SC2451 is in under voltage lockout condition and the SS/EN pin is pulled low by an internal switch.

Meanwhile, the high side and low side gate drivers DH, and DL, are kept low. Once VCC exceeds the UVLO threshold, the external soft start capacitor starts to be charged by a 5uA current source.

The gate drives are still kept off until the soft start capacitor voltage rises above 1V, at which point the low side gate is turned on and the high side gate is kept off for duration of one clock period .

At this point the top gate will start switching while keeping the bottom gate off, resulting in an asynchronous start up mode of operation.

As the SS/EN pin continues to rise, the error amplifier output also rises at the same rate and the duty cycle increases.

When the SS pin reaches 2V, the low side Mosfet will begin to switch and the convertor is fully operational in the synchronous mode.

Once the output voltage has reached regulation and is within ± 10%, an open collector power good flag is activated, and the error amplifier output will no longer be clamped to the SS/EN voltage. The SS/EN voltage continues to rise up to AVCC and will stay at that voltage level during normal operation.

If an over current condition occurs, the SS/EN pin will discharge to 500mV by an internal switch. During this time, both DH and DL will be turned off. Once the SS/EN reaches 1V, the low side gate will be turned on and the SS/EN pin will again start to be charged by the 5µA current source and the same soft start sequence mentioned above will be repeated.

Application Information (Cont.)

Bias Generation

A 4.5 to 6.5V supply voltage is required to power up the SC2451. This voltage could be provided by an external power supply or derived from Vin (Vin>6.5V) through an external PNP pass transistor.

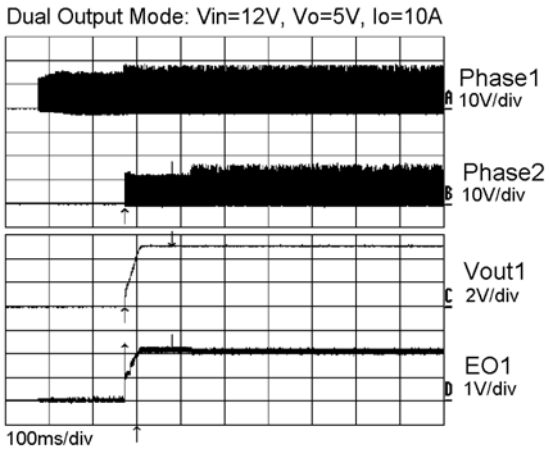
BDI is the control signal to the base of the PNP pass transistor that will regulate AVCC. The voltage at AVCC pin is compared to the bandgap, and the BDI output is adjusted to produce 5.4V to 6.6V at the AVCC pin.

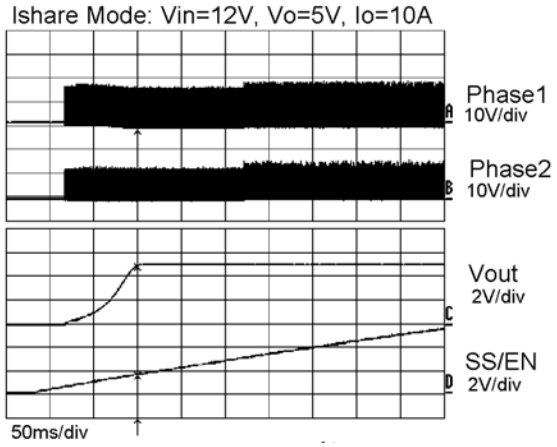
Soft start / Shut down

An external capacitor at the SS/EN pin is used to set up the soft start duration. The capacitor value in conjunction with the internal current source, controls the duration of soft start time. Below is an explanation of the soft start cycle:

If the SS/EN pin is pulled down to AGND, the SC2451 is disabled. The soft start pin is charged by a 5uA current source and discharged by an internal switch. When SS/EN is released it charges up to 0.5V as the control circuit starts up. The error amp outputs are now held off until the SS_EN pin has reached 1.0V (this prevents overshoot in the no load situation).

The error amp output will vary between 0.7 and 3.7V, depending on the duty cycle selected. (The 3V range represents 0 to 100% duty cycle). The error amp will be off until SS/EN reaches 1.0V and will move the output up to its desired voltage by the time SS/EN reaches 1.5V.



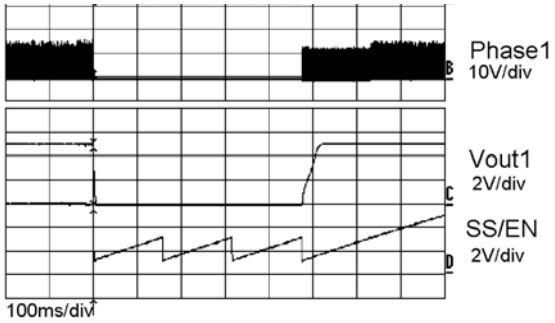


The gate drivers will be in asynchronous mode until the SS/EN pin reaches 3.0V. The intention for the asynchronous start up is to keep the low side Mosfet from being switched on which forces the low side Mosfet's body diode or the parallel Schottky diode to conduct. The conduction by the diode prevents any dips in an existing output voltage that might be present, allowing for a glitch free start up in applications that are sensitive to any bus disturbances.

In dual output mode, phase1 will start first followed by phase2. In single output mode (Ishare) both outputs come up together (the two phases are still 180 degrees out of phase). This sequencing change is automatic once the current share mode of operation is selected.

In case of a current limit, if phase 1 current limits and goes into hiccup mode both outputs will switch off. The outputs will be held off for the duration of 7 dummy soft start cycles. This period is defined by the SS cap being charged to 2V and sharply discharged to 1V making a 1V sawtooth. The part will try to restart on the next softstart cycle. If the fault has cleared, the outputs will start in sequence again. If the fault still remains, the part will repeat the soft start cycle above indefinitely until the fault has been removed.

Application Information (Cont.)



If phase2 current limits, it will go through the same softstart cycle as above but phase1 will be unaffected.

In Ishare mode, both outputs start together and will both shutdown and restart in the event of a current limit fault.

The soft start time is determined by the value of the softstart capacitor (see formula below).

$$T_{SS} \cong C_{SS} \times (167 \cdot 10^3)$$

Oscillator Frequency Selection

The internal oscillator sawtooth signal is generated by charging an internal capacitor with a current source. The charge current is set by an external resistor connected from OSC to AGND pins.

Following is the equation to calculate the oscillator frequency and some typical Rosc values:

$$F_{OSC} \cong \frac{10.5 \times 10^9}{R_{OSC}}$$

Rosc = 21kohms. produces;

Fosc = Fphase1 = Fphase2 = 500kHz

SYNC

In noise sensitive applications where synchronization of the oscillator frequency to a reference frequency is required, the SYNC pin can accept the external clock. An external control signal running at a higher frequency (Fosc*1.1) than the oscillator connected to the SYNC pin will result in synchronization of the internal oscillator frequency to the positive edge of the external control signal. SYNC is a positive edge triggered input with a threshold set to 1.5V.

Power Good

PWRGD pin provides an open collector output which will be pulled low if the output voltage is not within tolerance (Vo ± 10% typical). The PWRGD pin will stay low until softstart cycle has been completed and the output voltage is with in the power good limits.

This indicator signal could be used to flag supervisory circuit to a fault condition. A 10kohms pull up resistor to AVCC or an external supply is recommended at the PWRGD pin.

Current Limit (Hiccup or Shut down mode)

Hiccup and shutdown modes of over current protection are available to the designer using the SC2451. The output inductor current is sensed via a current sense resistor, or lossless inductive sensing. The voltage across Rsense is filtered by placing resistors in series from Rsense to the CS+ and CS- pins of the SC2451. A small capacitor is also placed between the CS+ and CS- pins. This signal is then used for over current protection and the current sharing mode of operation.

The current limit level is set by the value of the series resistor connected to the CS- pin. The following formula can be used to approximate the current limit level:

R_{sense}	=	current sensing resistor
V_{I_Limit}	=	Current limit threshold (Typical 70mv)
I_{OUT_MAX}	=	Maximum output current limit
R_{OSC}	=	Oscillator resistor
V_{BG}	=	Bandgap voltage (Typical 1.225V)

$$R_{Sense} \cong \frac{V_{I\_Limit}}{I_{OUT\_MAX}}$$

$$R_{CS-} \cong \frac{I_{OUT\_MAX} \times R_{Sense} \times R_{OSC}}{V_{BG}}$$

Once an over current event has occurred, the PWM cycle will end until the current decays below 2/3 of the selected current limit level (30% hysteresis). It should be noted that the operational limit for the CS- and CS+ inputs is 0.5V below the AVCC supply.

Hiccup current limit

With the hiccup mode selected (ILIM_MODE pin pulled high), the cycle by cycle current limit will trigger a counter which will cause the output to go into hiccup mode. The phase which goes into current limit first will dictate how the outputs will switch off. If Phase1 current limits first, then both channels will be switched off and re-soft started in sequence. If phase 2 current limits first, only phase 2 will switch off and be re-soft started while phase1 is undisturbed.

Application Information (Cont.)

When the current limit has been triggered for a minimum of 16 (maximum of 31) clock pulses (at the switching frequency) the output is disabled for the duration of 7 dummy soft start cycles and the output is then restarted. This sequence repeats indefinitely until the over current condition is removed.

Shut down current limit

In the shut down current limit (ILIM_MODE pin pulled low to AGND), if OUT1 has a continuous fault , both OUT1 and OUT2 will be latched off. If a fault condition occurs only at OUTPUT2, it will be latched off while OUTPUT1 continues normal operation. The latched off condition can be reset by either powering down the supply and then bringing it up above the UVLO limit, or by pulling down the SS/EN pin and then releasing it to be pulled up high again.

Fault Protection

In addition to current limit, the SC2451 monitors over temperature and VCC supply under-voltage conditions. The over temperature detect will shut the part down if the die temperature exceeds 160°C.

Under Voltage Lock Out

Under Voltage Lock Out (UVLO) circuitry senses the VCC through a voltage divider. If this signal falls below 4.4V (typical) with a 100mV hysteresis (typical), the error amplifier and the PWM comparator outputs are pulled low, hence causing the lower MOSFET gate to be on while keeping the upper MOSFET gate off for both phases. During the thermal shutdown, the same fault shutdown sequence is applied as mentioned above.

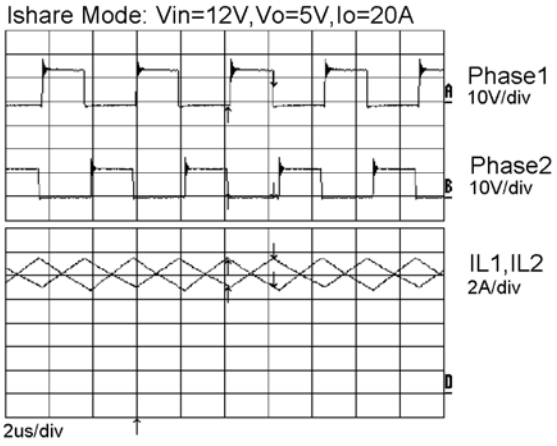
Current sharing mode (ISHOUT)

In addition to the standard dual output synchronous buck configuration, SC2451 also can be setup for a single output dual phase operation (running 180° out of phase) providing the benefits of input and output current ripple cancellation for the higher power applications. The current share mode is simply set up by placing a current sharing amplifier gain resistor between the EO1 and EO2 pins and an averaging capacitor placed from the ISHOUT pin to AGND.

The inductor current of the two phases is sensed via the current sensing resistors. The current difference between the two phases is then averaged via the Ishare capacitor. This averaged value is used to produce a current source or sink which has a full range of ± 80uA. This offset current will then create an offset voltage in conjunction with the resistor connected between the EO1 and EO2. The offset produced will in turn cause the duty cycle of the phases to be adjusted in order to achieve current sharing between them.

The maximum offset possible is 3V, which is the oscillator ramp amplitude (0 to 100% duty cycle).

The resistor connected between the EO1 and EO2 value dictates the gain and hence the accuracy of the ishare loop.



The following example can be used for choosing the resistor value:

Vin=12V

Vo=5V

D = 41.7%

Fosc = Fphase1 = Fphase2 = 500kHz

Io = 20A, Io1 = 9A, Io2 = 11A

Rsense = 5mohms

Oscillator Ramp Peak = 3V (100% duty cycle)

Approximate error voltage is about:

D*Ramp Peak = .417*3 = 1.25V.

The current error between the two phases is 2A, which is about 10mV (10%).

The 10% offset voltage needed to balance the current sharing at the output of the EO1 and EO2 (voltage across the resistor) will be about 125mV.

Keeping the center point of the current source around 40uA, the resistor value that can be used is:

125mV/40uA = 3.125 kohms.

Application Information (Cont.)

The optimum capacitor value will depend on the switching frequency, since the output ripple current is being averaged.

Gate Drive/Control

The SC2451 also provides integrated high current gate drives for fast switching of large Mosfets. The high side and low side Mosfet gates could be switched with a peak gate current of 2A. The higher gate current will reduce switching losses of the larger MOSFETs.

The low side gate drives are supplied from the PVCC. The high side gate drives could be provided with either the classical boot strapping technique or an external supply voltage up to 12V connected to the BST pin.

Cross conduction prevention circuitry ensures a non overlapping (50ns typical) gate drive between the top and bottom Mosfets. This prevents shoot through losses which provides higher efficiency. Typical total minimum off time for the SC2451 is about 250ns which will cause the maximum duty cycle at higher frequencies to be limited to lower than 100% (70% at 1.2MHz).

Application Information (Cont.)

ERROR AMPLIFIER DESIGN

The SC2451 is a voltage mode buck controller that utilizes an externally compensated high bandwidth error amplifier to regulate output voltage. The power stage of the synchronous rectified buck converter control-to-output transfer function is as shown below:

$$G_{VD}(s) = \frac{V_{IN}}{V_S} \times \left(\frac{1 + sESR_C C}{1 + s\frac{L}{R_L} + s^2 LC} \right)$$

where,

V_{IN} – Input voltage

R_L – Load resistance

L – Output inductance

C – Output capacitance

ESR_C – Output capacitor ESR

V_S – Peak to peak ramp voltage

The classical Type III compensation network can be built around the error amplifier as shown below:

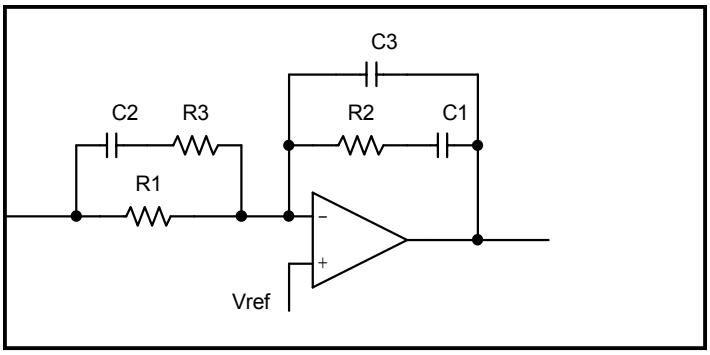


Figure 1. Voltage mode buck converter compensation network

The transfer function of the compensation network is as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{(1 + \frac{s}{\omega_{Z1}})(1 + \frac{s}{\omega_{Z2}})}{(1 + \frac{s}{\omega_{P1}})(1 + \frac{s}{\omega_{P2}})}$$

where,

$$\omega_{Z1} = \frac{1}{R_2 C_1}, \quad \omega_{Z2} = \frac{1}{(R_1 + R_3)C_2}, \quad \omega_o = \frac{1}{\sqrt{Lout \times Cout}}$$

$$\omega_I = \frac{1}{R_1(C_1 + C_3)}, \quad \omega_{P1} = \frac{1}{R_3 C_2}, \quad \omega_{P2} = \frac{1}{R_2 \frac{C_1 C_3}{C_1 + C_3}}$$

The design guidelines are as following:

1. Set the loop gain crossover frequency w_c for given switching frequency.

2. Place an integrator in the origin to increase DC and low frequency gains.

3. Select w_{Z1} and w_{Z2} such that they are placed near w_0 to dampen peaking; the loop gain has –20 dB rate to go across the 0 dB line for obtaining a wide bandwidth.

4. Cancel w_{ESR} with compensation pole w_{P1} ($w_{P1} = w_{ESR}$).

5. Place a high frequency compensation pole w_{P2} at half the switching frequency to get the maximum attenuation of the switching ripple and the high frequency noise with the adequate phase lag at w_C.

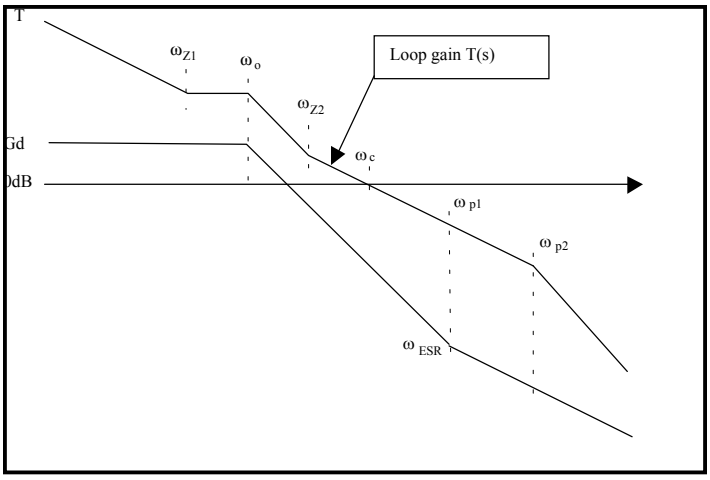


Figure 2. Simplified asymptotic diagram of buck power stage and its compensated loop gain.

Application Information (Cont.)

PCB LAYOUT GUIDELINES

Careful attention to layout is necessary for successful implementation of the SC2451 PWM controller. High switching currents are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power section of the circuit should be laid out first. A ground plane should be used. The number and position of ground plane interruptions should not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas; for example, the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (M1), and the Bottom FET (M2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of M1, M2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short. Top FET gate charge currents flow in this trace.

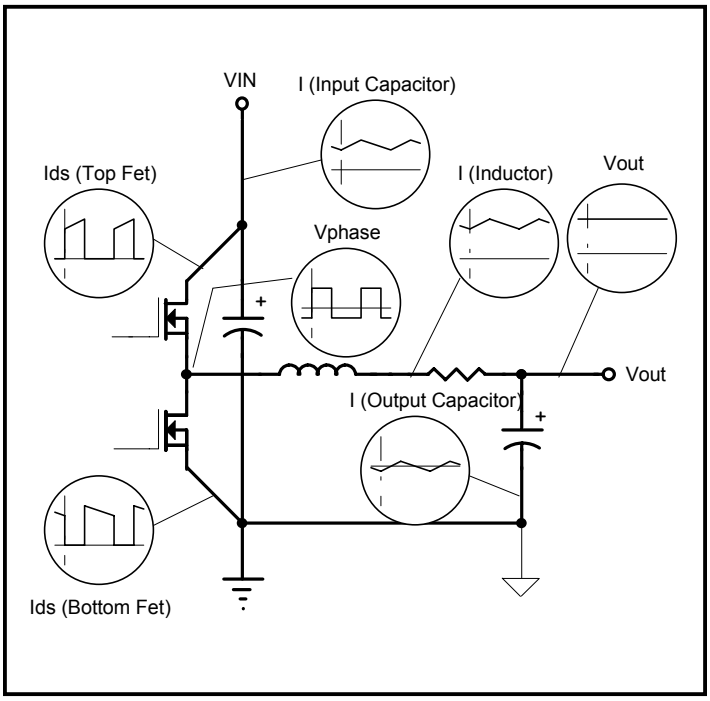
4) The Output Capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only, and therefore, connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC2451 is best placed over a quiet ground plane area. Avoid pulse currents in the Cin, M1, M2 loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, M1, M2 loop. Under no circumstances should GND be returned to a ground inside the Cin, M1, M2 loop.

6)If the BST for the SC2451 is supplied from the 12V supply, the BST pin should be decoupled directly to GND by a 0.1uF ceramic capacitor. Trace lengths should be as short as possible. If a 12V supply is not available, a classical boot strap method could be implemented to achieve the upper MOSFETs gate drive.

7) For current share mode of operation, the two converters should be laid out as symmetrical as possible for the best current sharing accuracy.

8) Allow adequate heat sinking area for the power components. If multiple layers will be used, provide sufficent vias for heat ransfer



Voltage and current waveforms of buck power stage .

Application Information (Cont.)

COMPONENT SELECTION:
SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \leq \frac{V_t}{I_t}$$

Where

V_t = **Maximum transient voltage excursion**

I_t = **Transient current step**

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Capacitor		Qty Rqd.	Total	
	C (uF)	ESR (mΩ)		C (uF)	ESR (mΩ)
Low ESR Tantalum	330	60	6	2000	10
OS-CON	330	25	3	990	8.3
Low ESR Aluminum	1500	44	5	7500	8.8

The choice of which to use is simply a cost/performance issue, with low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above.
The maximum inductor value may be calculated from:

$$L \leq \frac{R_{ESR}\ C}{I_t}(V_{IN} - V_O)$$

The calculated maximum inductor value assumes 100% duty cycle, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions. We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L\ RIPPLE} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS\ (on)} \cdot D$$

where

$$D = \text{duty cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, If we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot 10^{-3}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{osc}}{4}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to as-

Application Information (Cont.)

sume that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

To a first order approximation, it is convenient to only consider conduction losses to determine FET suitability. For a 5V in, 2.8V out at 14.2A requirement, typical FET losses would be:

FET Type	$R_{DS(on)}$ (mΩ)	PD(W)	Package
IRL3402S	15	1.69	D²PAK
IRL2203	10.5	1.19	D²PAK
Si4410	20	2.26	SO-8

Using 1.5X Room temp $R_{DS(ON)}$ to allow for temperature rise.

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it resulting in low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1 - D)$$

For the example above:

FET Type	$R_{DS(on)}$ (mΩ)	P_D(W)	Package
IRL3402S	15	1.33	D²PAK
IRL2203	10.5	0.93	D²PAK
Si4410	20	1.77	SO-8

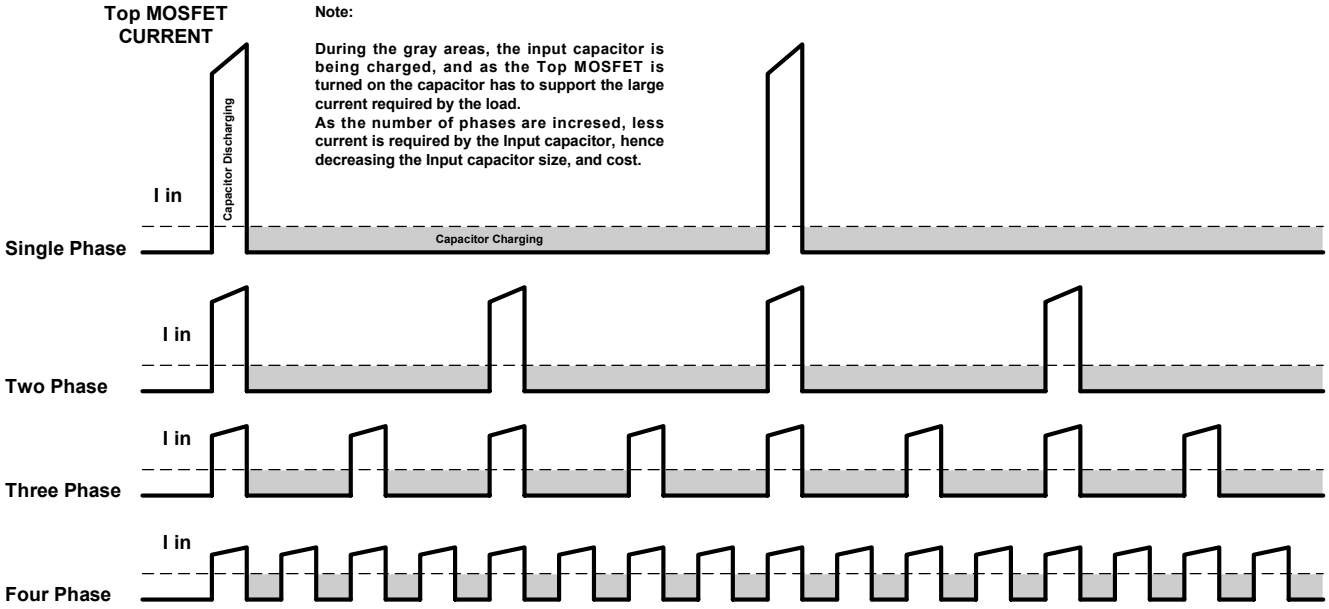
Each of the package types has a characteristic thermal impedance, for the TO-220 package, thermal impedance is mostly determined by the heatsink used. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D²PAK and 80°C/W for the SO-8 are readily achievable. The corresponding temperature rise is detailed below:

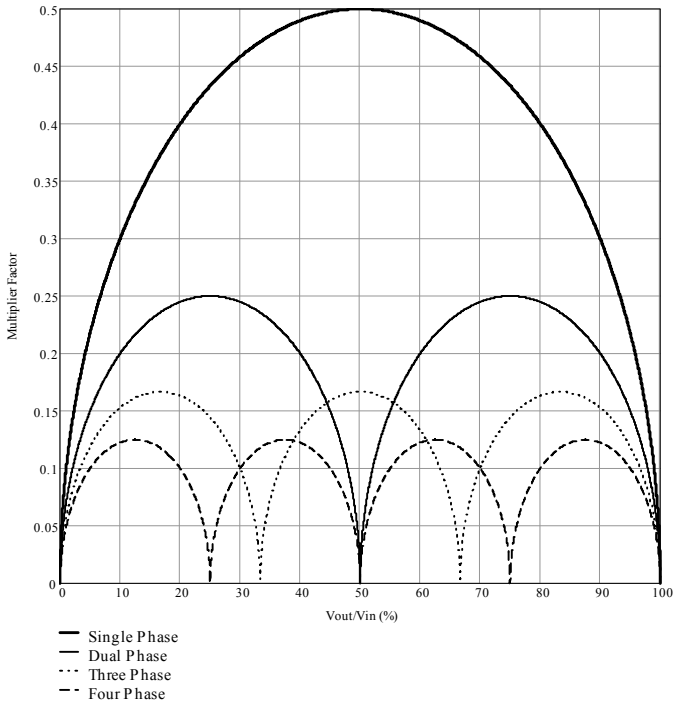
	Temperature rise (°C)	
FET Type	Top FET	Bottom FET
IRL3402S	67.6	53.2
IRL2203	47.6	37.2
Si4410	180.8	141.6

It is apparent that single SO-8 Si4410 are not adequate for this application, By using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

INPUT CAPACITORS - Since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

Applications Information (Cont.)





Following procedure will determine the input capacitor RMS current:

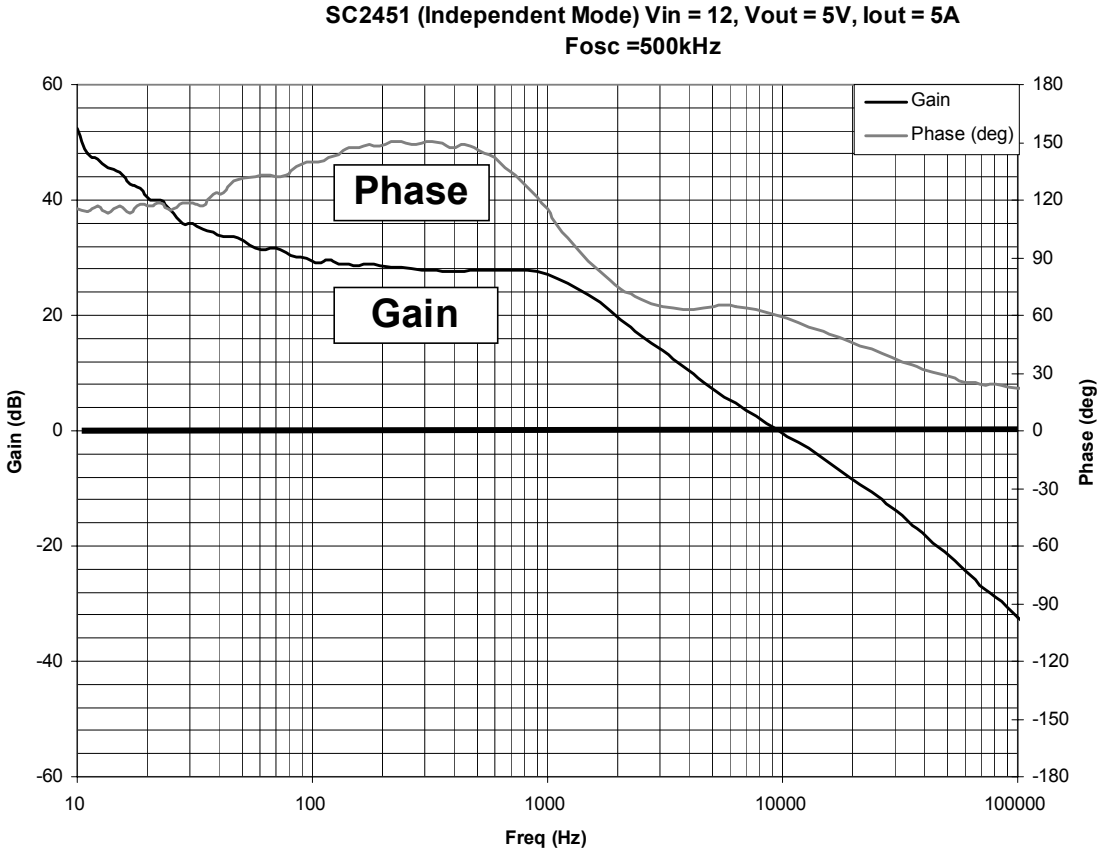
1- Calculate Duty Cycle Ratio = Vout/Vin.

2- Use the Calculated Duty Cycle and the number of phases in the converter to find the Multiplier Factor from the Curve above.

3- Multiply the full load current by the multiplier factor; this will be the RMS current that the input capacitors need to support.

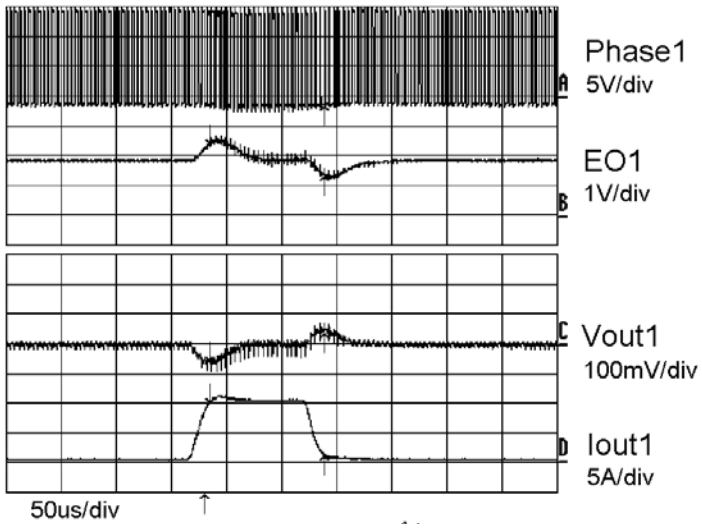
Typical Characteristics

Gain & Phase Margin

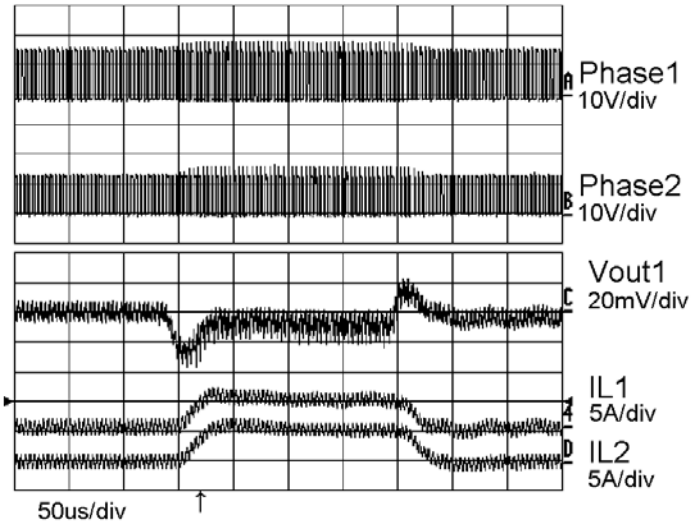


Typical Step Load

Vin =12V, Vout=5V, Iout=10A

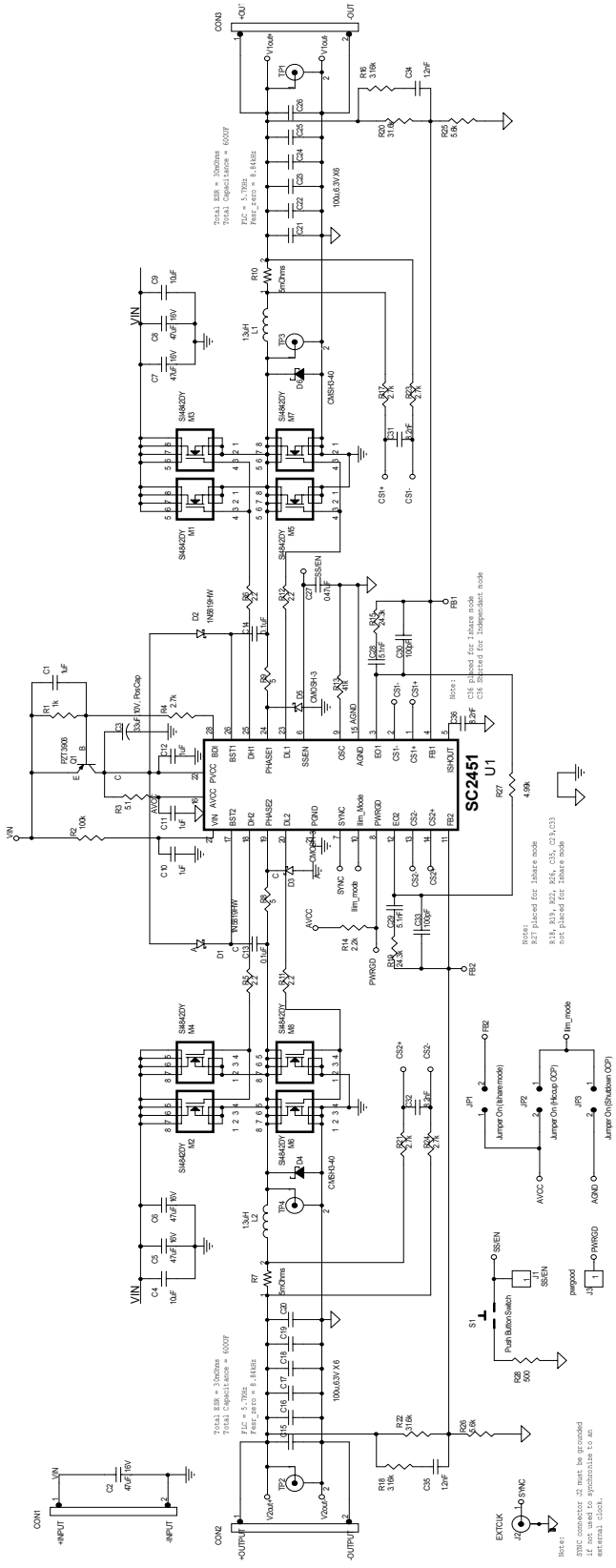


Dual Output Mode



Ishare Mode

Evaluation Board Schematic



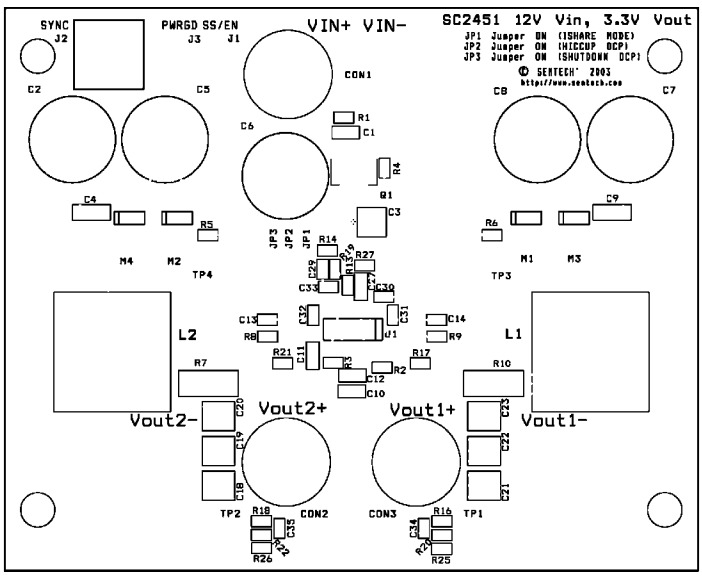
Evaluation Board Bill of Materials

SC2451 Evaluation Board 12Vin 3.3Vout
SC2451_12Vin_3.3vout Revision: 1a

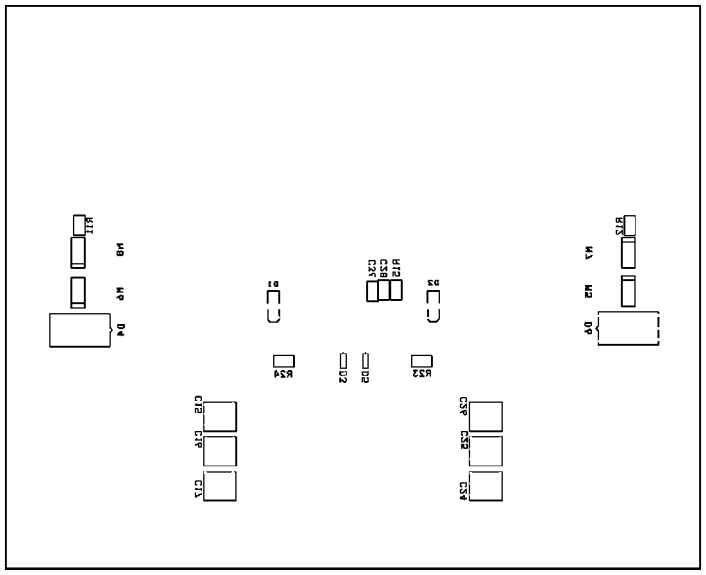
Bill Of Materials November 5,2003 16:22:25

Item	Quantity	Reference	Part	Manufacturer #	Foot Print
1	3	CON1,CON2,CON3	Dual_banana		DUAL_BANANASOCKET
2	4	C1,C10,C11,C12	1uF		SM/C_0805
3	5	C2,C5,C6,C7,C8	47uF, 16V	TDK (C5750X5R1C476MT)	SM/C_2220
4	1	C3	33uF,10V, PosCap	10TPB33M (Sanyo)	SM/C_B2
5	2	C4,C9	10uF		SM/C_1206
6	2	C14,C13	0.1uF		SM/C_0603
7	12	C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26	100u,6.3V	12106D107MAT(AVX)	SM/C_1210_GRM
8	1	C27	0.47uF		SM/C_0805
9	2	C28,C29	5.1nF		SM/C_0603
10	2	C33,C30	100pF		SM/C_0603
11	3	C31,C32,C36	8.2nF		SM/C_0603
12	2	C35,C34	1.2nF		SM/C_0603
13	2	D1,D2	1N5819HW	1N5819HW(Diodes Inc.)	SOD123
14	2	D5,D3	CMOSH-3	CMOSH-3 (Central Semiconductor)	SOD523
15	2	D4,D6	CMSH3-40	CMSH3-40(Central Semiconductor)	SM/D_SMC
16	1	JP1	Jumper On (Ishare mode)		VIA\2P
17	1	JP2	Jumper On (Hiccup OCP)		VIA\2P
18	1	JP3	Jumper On (Shutdown OCP)		VIA\2P
19	1	J1	SS/EN		tp
20	1	J2	EXTCLK		RF/PCB/BNC/F
21	1	J3	pwrgood		tp
22	2	L1,L2	1.3uH	PULSE (PG0077.142)	PCC-S1
23	8	M1,M2,M3,M4,M5,M6,M7,M8	SI4842DY	Vishay	SO-8
24	1	Q1	PZT3906		SM/SOT223_BCEC
25	1	R1	1k		SM/R_0603
26	1	R2	100k		SM/R_0603
27	1	R3	5.1		SM/R_0603
28	5	R4,R17,R21,R23,R24	2.7k		SM/R_0603
29	4	R5,R6,R11,R12	2.2		SM/R_0603
30	2	R7,R10	5mOhms		SM/R_2512
31	2	R9,R8	5		SM/R_0603
32	1	R13	41k		SM/R_0603
33	1	R14	2.2k		SM/R_0603
34	2	R15,R19	24.3k		SM/R_0603
35	2	R18,R16	3.16k		SM/R_0603
36	2	R20,R22	31.6k		SM/R_0603
37	2	R26,R25	5.6k		SM/R_0603
38	1	R27	4.99k		SM/R_0603
39	1	R28	500		SM/R_0603
40	4	TP1,TP2,TP3,TP4	Probe_TP		Probe_TP
41	1	U1	SC2451	Semtech	TSSOP28

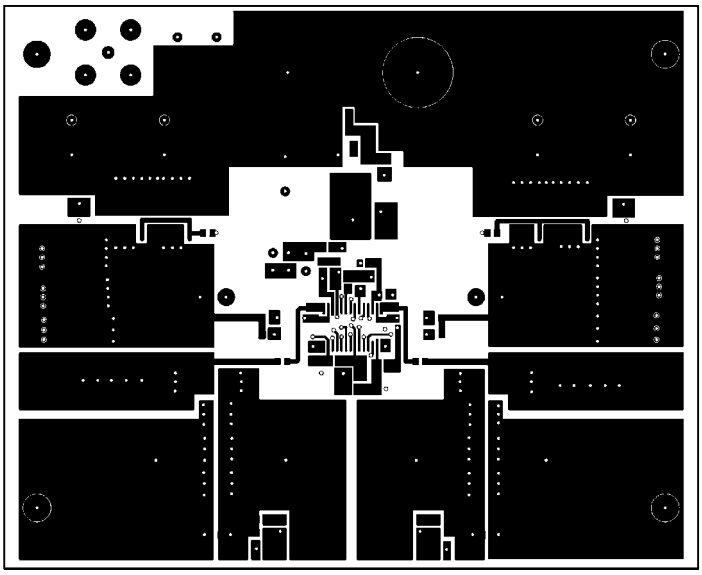
Evaluation Board Gerber Plots



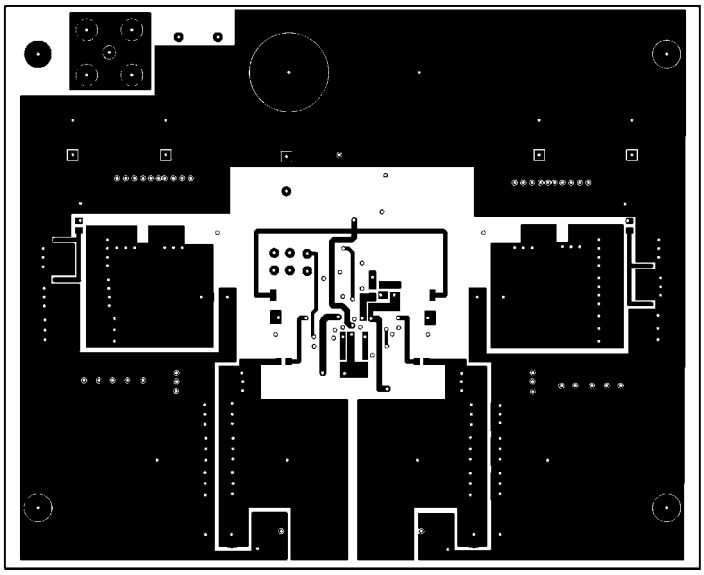
Board Layout Assembly Top



Board Layout Assembly Bottom

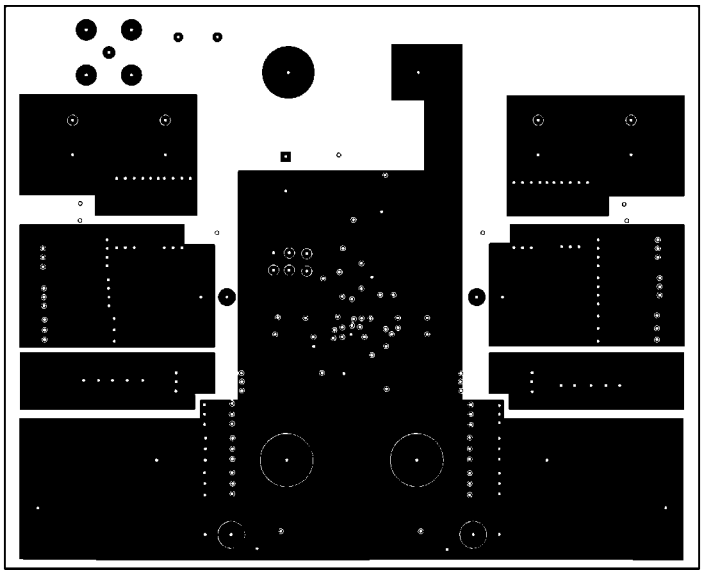


Board Layout Top

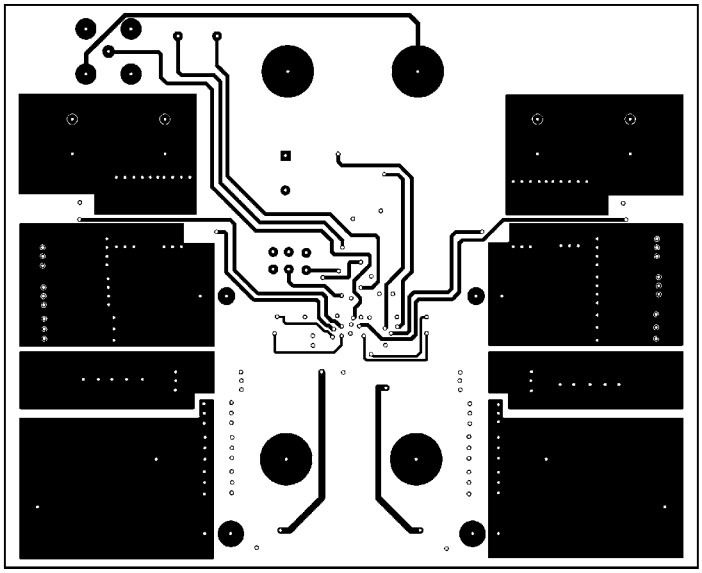


Board Layout Bottom

Evaluation Board Gerber Plots (Cont.)

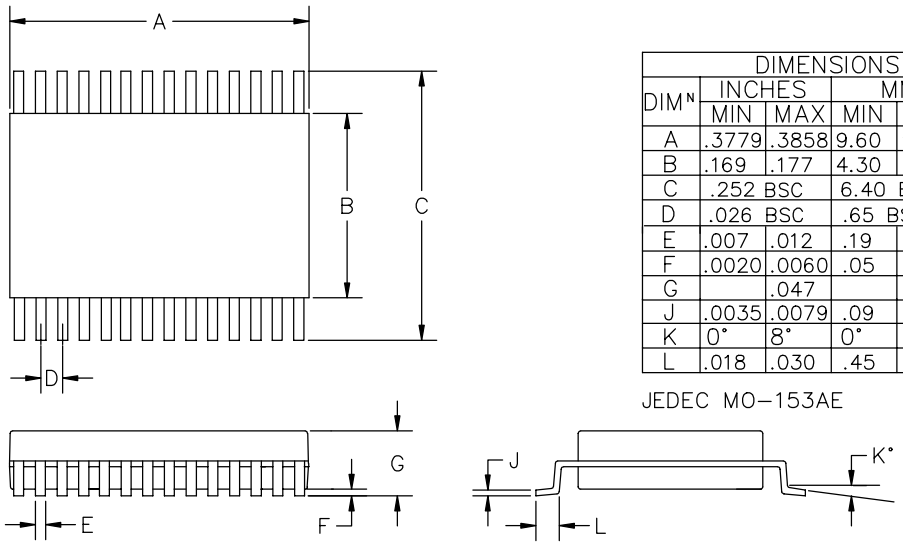


Board Layout INNER1



Board Layout INNER2

Outline Drawing - TSSOP-28



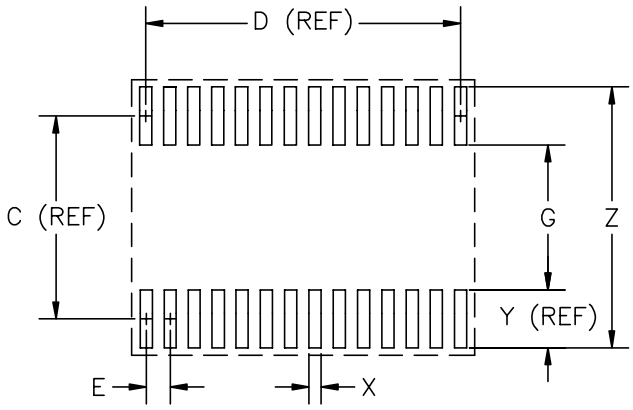
DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AE

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.333	—	8.45	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	—
Y	—	.062	—	1.583	REF
Z	—	.280	—	7.113	—

[2] GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

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