2111 • 2111-1 • 2111-2 • 2611-XA, IK

DESCRIPTION

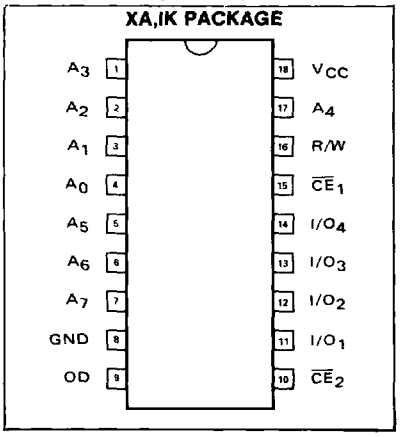
The 2111 series are 1024-bit high performance, low power static read/write RAMS organized as 256 words by 4 bits.

The 2111 series are fully static and no refresh operations, sense amplifiers, or clocks are required. All inputs and outputs are directly TTL-compatible and only one +5V power supply is required.

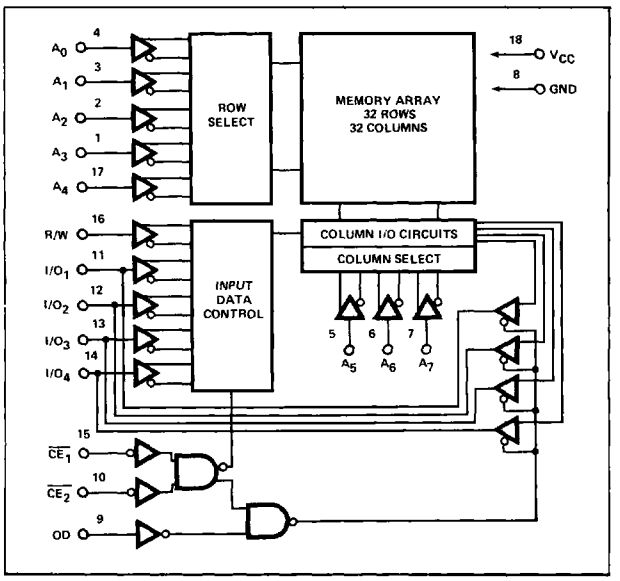
The 2111 series is fabricated with N-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

PIN CONFIGURATION

XA,IK PACKAGE



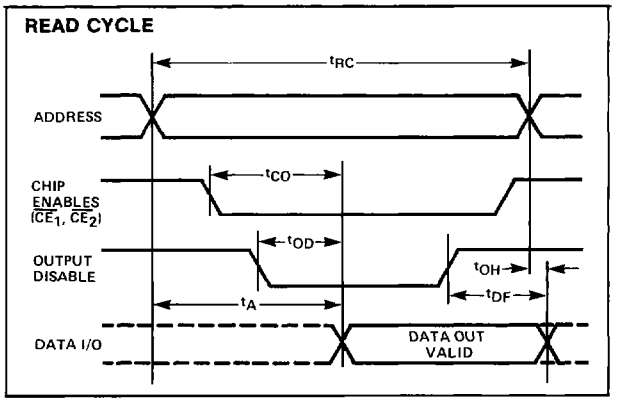
BLOCK DIAGRAM

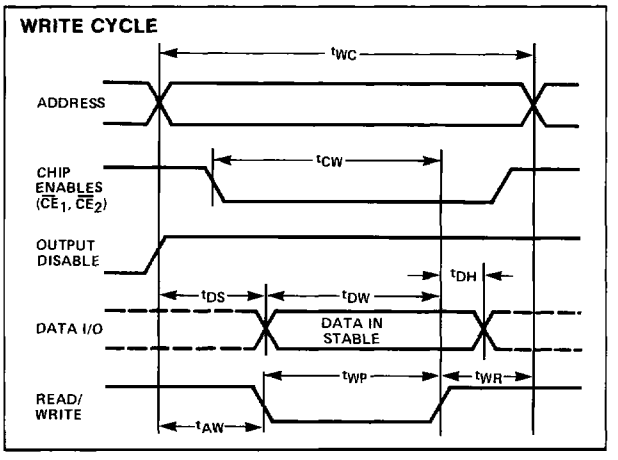


SWITCHING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

			2111		2111-1		2111-2		2611		
READ CYCLE	**Parameter**	**Test Conditions**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle		1,000		500		650		400		ns
t_A	Access Time	t_r, t_f = 20ns		1,000		500		650		400	ns
t_{CC}	Chip Enable To Output	V_{IN} = +0.65V to +2.2V		800		350		400		175	ns
t_{OD}	Output Disable To Output	Timing Reference = 1.5V		700		300		350		150	ns
t_{DF} (3)	Data Output to High Z State	Load = 1 TTL Gate	0	200	0	150	0	150		125	ns
t_{OH}	Previous Read Data Valid after change of Address	and C_L = 100pF.	40		40		40		40		ns
WRITE CYCLE											
t_{WC}	Write Cycle		1,000		500		650		400		ns
t_{AW}	Write Delay	t_r, t_f = 20ns	150		100		150			400	ns
t_{CW}	Chip Enable To Write	V_{IN} = +0.65V to +2.2V	900		400		550		150		ns
t_{DW}	Data Setup	Timing Reference = 1.5V	700		280		400		125		ns
t_{DH}	Data Hold	Load = 1 TTL Gate	100		100		100		50		ns
t_{WP}	Write Pulse	and C_L = 100pF.	750		300		400		150		ns
t_{WR}	Write Recovery		50		50		50		0		ns
t_{DS}	Output Disable Setup		200		150		150		150		ns


READ CYCLE
tRC
ADDRESS
CHIP ENABLES ($\overline{CE_1}$, $\overline{CE_2}$)
tCO
tOD
OUTPUT DISABLE
tOH
tDF
tA
DATA I/O
DATA OUT VALID


WRITE CYCLE
tWC
ADDRESS
tCW
CHIP ENABLES ($\overline{CE_1}$, $\overline{CE_2}$)
OUTPUT DISABLE
tDH
tDS
tDW
DATA I/O
DATA IN STABLE
tWP
tWR
READ/ WRITE
tAW