TELEDYNE COMPONENTS

CDG308 CDG4308
CDG309 CDG4309

# QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCHES

## FEATURES

- **High OFF Isolation .....68 dB @ 10 MHz**
- **Low Insertion Loss.....–1 dB @ 100 MHz**
- **Low Channel-to-Channel Cross Talk .....–80 dB @ 10 MHz**
- **CMOS-Compatible Inputs**
- **Low OFF Leakage**
- **Industry Standard Pinout (CDG308/CDG309)**

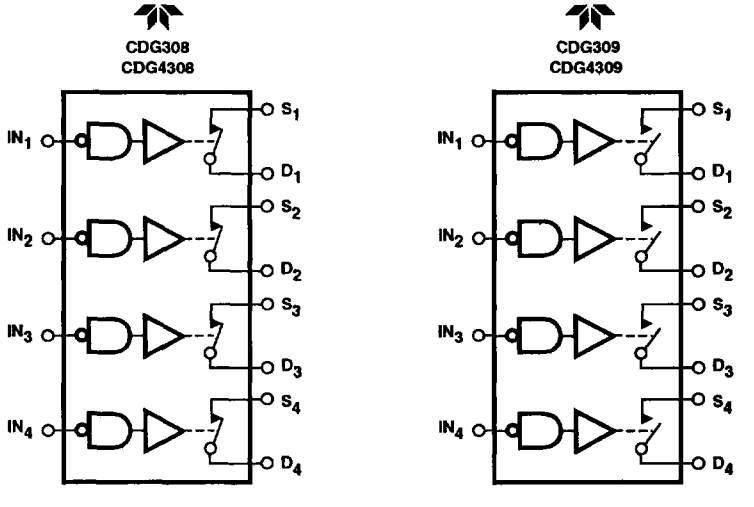
## APPLICATIONS

- **Glitch-Free Analog Switching**
- **RF and Video**
- **Track-and-Hold**
- **Sample-and-Hold**

## GENERAL DESCRIPTION

Teledyne Components' CMOS/DMOS analog switches feature high-speed, low-power CMOS input logic and level translation circuitry, and high-speed, low-capacitance, lateral DMOS switches. CMOS and lateral DMOS circuitry are fabricated together on a single silicon chip. The CDG4308 and CDG4309 use the same die as CDG308 and CDG309; the extra isolating pin between switch input and output increases isolation by 6 dB.

## FUNCTIONAL BLOCK DIAGRAMS




NOTES: 1. Four SPST switches per package.
2. Switches shown in logic "1" position.
3. CDG308/CDG4308: Logic "0" = OFF; Logic "1" = ON
CDG309/CDG4309: Logic "0" = ON; Logic "1" = OFF

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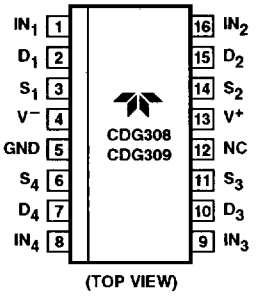
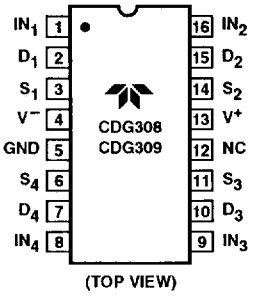
# QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCHES

## CDG308 CDG4308 CDG309 CDG4309

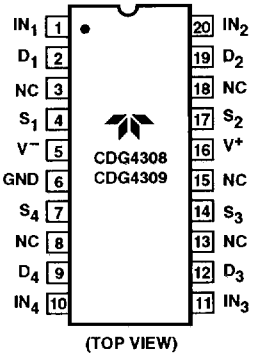
## PIN CONFIGURATIONS



(TOP VIEW)



(TOP VIEW)



(TOP VIEW)

NC = NO INTERNAL CONNECTION

## ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|---|---|---|
| CDG308COE | 16-Pin SO | 0°C to +70°C |
| CDG308CPE | 16-Pin Plastic DIP | 0°C to +70°C |
| CDG308EJE | 16-Pin CerDIP | –40°C to +85°C |
| CDG308EOE | 16-Pin SO | –40°C to +85°C |
| CDG308EPE | 16-Pin Plastic DIP | –40°C to +85°C |
| CDG308MJE | 16-Pin CerDIP | –55°C to +125°C |
| CDG309COE | 16-Pin SO | 0°C to +70°C |
| CDG309CPE | 16-Pin Plastic DIP | 0°C to +70°C |
| CDG309EJE | 16-Pin CerDIP | –40°C to +85°C |
| CDG309EOE | 16-Pin SO | –40°C to +85°C |
| CDG309EPE | 16-Pin Plastic DIP | –40°C to +85°C |
| CDG309MJE | 16-Pin CerDIP | –55°C to +125°C |
| CDG4308CPP | 20-Pin Plastic DIP | 0°C to +70°C |
| CDG4308EPP | 20-Pin Plastic DIP | –40°C to +85°C |
| CDG4309CPP | 20-Pin Plastic DIP | 0°C to +70°C |
| CDG4309EPP | 20-Pin Plastic DIP | –40°C to +85°C |

## ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage ..... –20V
Positive Supply Voltage ..... +20V
Control Input Voltage Range ..... $V^+$ +0.3V, $V^-$ –0.3V
Continuous Current, Any Pin Except S or D ..... 20 mA
Continuous Current, S or D ..... 30 mA
Peak Pulsed Current, S or D,
80 µs, 1%, Duty Cycle ..... 180 mA
Junction Temperature Range ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Power Dissipation ..... 500 mW

**NOTE:** All devices contain diodes to protect inputs against damage due to high-static voltages or electric fields. However, it is advised precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level ($V_{DD}$ or GND). Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Negative Supply Voltage ..... −8V to −15V
Positive Supply Voltage ..... +8V to +15V
Control Input Voltage Range ..... 0V to +5V
Analog Switch Voltage Range ..... ±10V
Operating Temperature Range
- C Suffix ..... 0°C to +70°C
- E Suffix ..... −40°C to +85°C
- M Suffix ..... −55°C to +125°C

## ELECTRICAL CHARACTERISTICS: $T_A$ = +25°C, $V^-$ = −15V, $V^+$ = +15V per channel, unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| $V_{ANALOG}$ | Analog Signal Range | | −10 | — | +10 | V |
| $r_{DS(ON)}$ | Switch ON Resistance | $V_S$ = −10V | — | 40 | 80 | Ω |
| | | $V_S$ = +2V | — | 45 | 80 | Ω |
| | | $V_S$ = +10V | — | 100 | 160 | Ω |
| $V_{IH}$ | High Level Input Voltage | | 4.5 | 3.4 | — | V |
| $V_{IL}$ | Low Level Input Voltage | | — | — | 1 | V |
| $I_{IN}$ | Logic Input Leakage Current | $V_{IN}$ = +5V | — | 0.01 | 0.1 | µA |
| | | $V_{IN}$ = +15V | — | 0.02 | 0.1 | µA |
| $I_{D(OFF)}$ | Switch OFF Leakage Current | $V_D$ = +10V, $V_S$ = −10V<br>$V_{IN}$ = +5V (CDG309/CDG4309)<br>$V_{IN}$ = +1V (CDG308/CDG4308) | — | 0.2 | 5 | nA |
| $I_{S(OFF)}$ | Switch OFF Leakage Current | $V_S$ = +10V, $V_D$ = −10V<br>$V_{IN}$ = +5V (CDG309/CDG4309)<br>$V_{IN}$ = +1V (CDG308/CDG4308) | — | 0.4 | 5 | nA |
| $I^-$ | Negative Supply Quiescent Current | $V_{IN}$ = +5V (CDG309/CDG4309)<br>$V_{IN}$ = +1V (CDG308/CDG4308) | — | −0.1 | −0.5 | µA |
| $I^+$ | Positive Supply Quiescent Current | $V_{IN}$ = +5V (CDG309/CDG4309)<br>$V_{IN}$ = +1V (CDG308/CDG4308) | — | 0.1 | 0.5 | µA |
| **Dynamic** | | | | | | |
| $t_{ON}$ | Switch Turn-On Time | $V_{IN}$ = +1V (CDG308/CDG4308)<br>$V_{IN}$ = +5V (CDG309/CDG4309) | — | 140 | 250 | ns |
| $t_{OFF}$ | Switch Turn-Off Time | $V_{IN}$ = +1V (CDG308/CDG4308)<br>$V_{IN}$ = +5V (CDG309/CDG4309) | — | 80 | 220 | ns |
| OIRR | Off Isolation Rejection Ratio | f = 10 MHz, $R_L$ = 50Ω (CDG308/CDG309) | 60 | 62 | — | dB |
| | | f = 10 MHz, $R_L$ = 50Ω (CDG4308/CDG4309) | 66 | 68 | — | dB |
| $C_{CRR}$ | Cross-Coupling Rejection Ratio | f = 10 MHz, $R_L$ = 50Ω | — | 80 | — | dB |
| $C_D$ | Drain-Node Capacitance | $V_D$ = $V_S$ = 0, f = 1 MHz<br>$V_{IN}$ = +1V (CDG308/CDG4308)<br>$V_{IN}$ = +5V (CDG309/CDG4309) | — | 0.3 | — | pF |
| $C_S$ | Source-Node Capacitance | $V_D$ = $V_S$ = 0, f = 1 MHz<br>$V_S$ = 0, f = 1 MHz, $V_{IN}$ = 0V<br>$V_{IN}$ = +5V (CDG309/CDG4309) | — | 3 | — | pF |

# CDG308 CDG4308
# CDG309 CDG4309

**ELECTRICAL CHARACTERISTICS:** $V^- = -15V$, $V^+ = +15V$ per channel, unless otherwise noted.
**Limits at Temperature Extremes**

| Symbol | Parameter | Test Conditions | Maximum @ $T_A$ = −55°C | −40°C | +70°C | +85°C | +125°C | Unit |
|---|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | | |
| $V_{ANALOG}$ | Analog Signal Range | | ±10 | ±10 | ±10 | ±10 | ±10 | V |
| $r_{DS(ON)}$ | Switch ON Resistance | $V_S = +2V$, $V_S = -10V$ | 80 | 80 | 120 | 120 | 150 | Ω |
| | | $V_S = +10V$ | 160 | 160 | 240 | 240 | 300 | Ω |
| $I_{IN}$ | Logic Input Leakage Current | $V_{IN} = +5V$ | 0.1 | 0.1 | 1 | 1 | 10 | µA |
| | | $V_{IN} = +15V$ | 0.1 | 0.1 | 2 | 2 | 20 | µA |
| $I_{D(OFF)}$ | Switch OFF Leakage Current | $V_D = +10V$, $V_S = -10V$ | 5 | 5 | 100 | 100 | 1000 | nA |
| $I_{(OFF)}$ | Switch OFF Leakage Current | $V_S = +10V$, $V_D = -10V$ | 5 | 5 | 100 | 100 | 1000 | nA |
| $I^-$ | Negative Supply Quiescent Current | | −0.5 | −0.5 | −20 | −20 | −100 | µA |
| $I^+$ | Positive Supply Quiescent Current | | 0.5 | 0.5 | 20 | 20 | 100 | µA |

## SWITCH CONTACTS

Switches are bidirectional (analog input can be to source or drain). However, for optimum performance in video applications, connect input to source and output to drain. (See Figure 1.)

## POWER SUPPLY DECOUPLING CIRCUIT

By inserting 1 kΩ resistors in series with $V^+$ and $V^-$ power supply lines, and decoupling both pins at the device socket, it is possible to improve video switch power supply rejection ratios by 50 dB at frequencies of 20 MHz and higher. (See Figure 2.)

## APPLICATIONS

### Very Low Distortion Circuit for Low Frequency/Large Signal Applications

The circuit shown in Figure 3 provides very low distortion (<0.1%) and high off isolation (>90 dB) at signal levels equal to the supply voltage. The signal passes through a "T" switch configuration and at the same time modulates the power supply. This modulation maintains a constant ON resistance, $r_{DS(ON)}$, which in turn reduces distortion. R5 is for bypassing the power supply and has a typical value of 1 kΩ; R4 should be a value that can be accommodated by the signal source as load; R3 is only necessary at loads lower

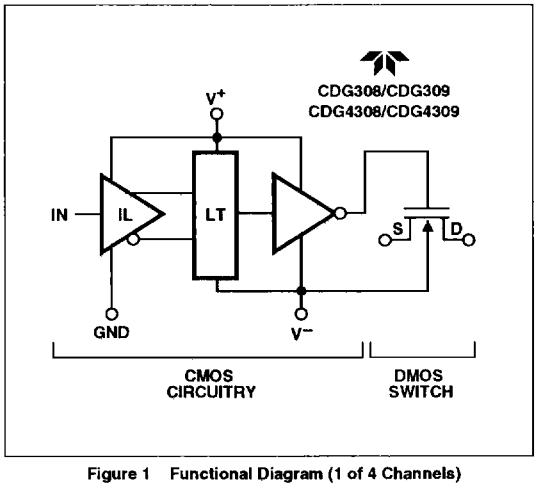



Figure 1 Functional Diagram (1 of 4 Channels)

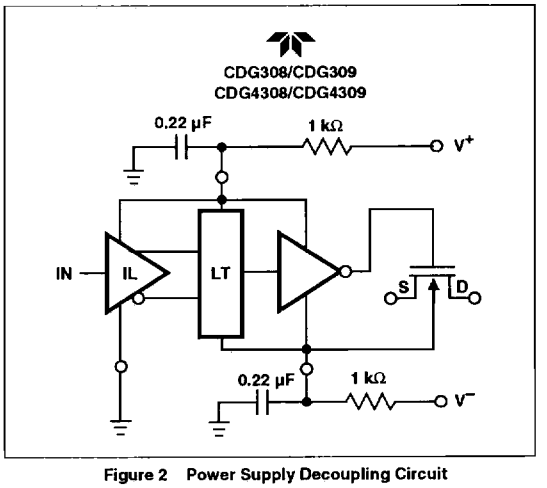



Figure 2 Power Supply Decoupling Circuit

than 100Ω and should be selected during initial circuit design; C1 has to be large enough for the lowest signal to pass and C2 will have to bypass all signals. R1 and R2 set up the logic "1" level for the control input and should be set to 5V.

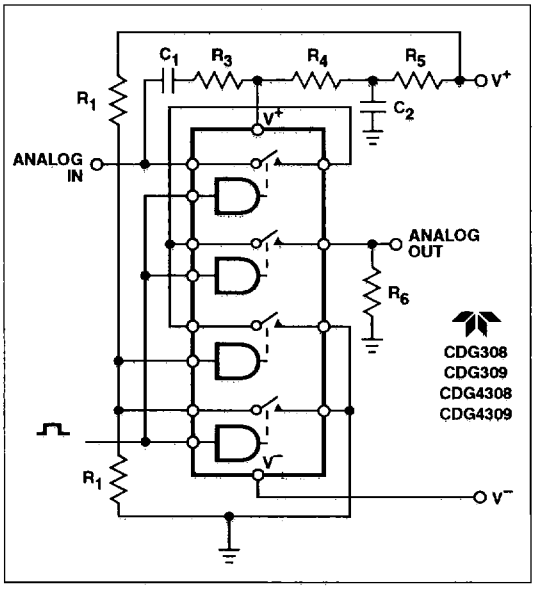



Figure 3 Low Distortion, Rail-to-Rail Analog Switch

## Logic Inverter

The circuit shown in Figure 4 provides logic inversion with two resistors and one switch. It does not require additional logic parts. The resistors divide the supply voltage to a 5V level when high, and are switched to a low level via the switch. This configuration allows a single-pole, single-throw switch to be changed into a single-pole, double-throw switch.

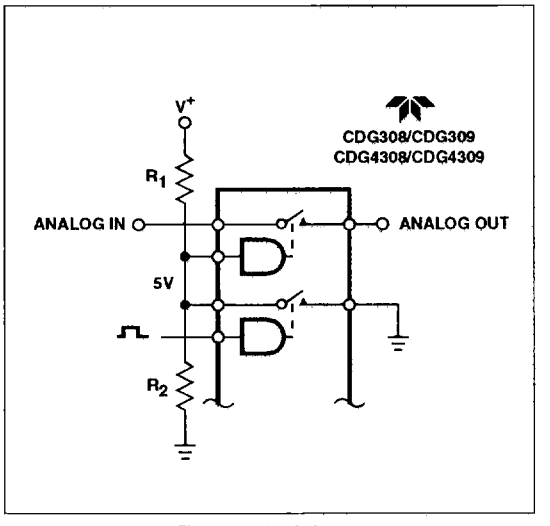



Figure 4 Logic Inverter

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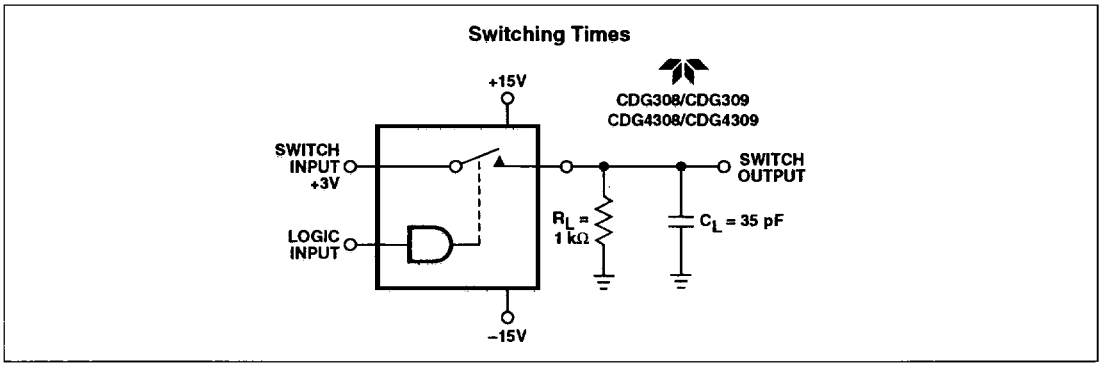
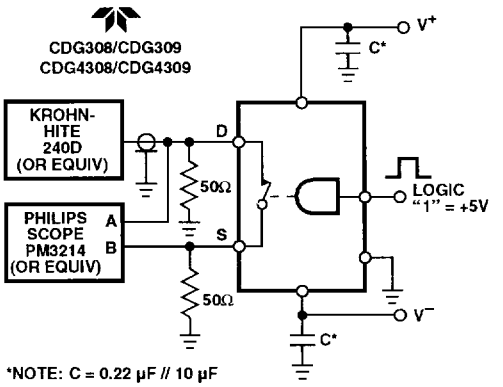
## TEST CIRCUITS



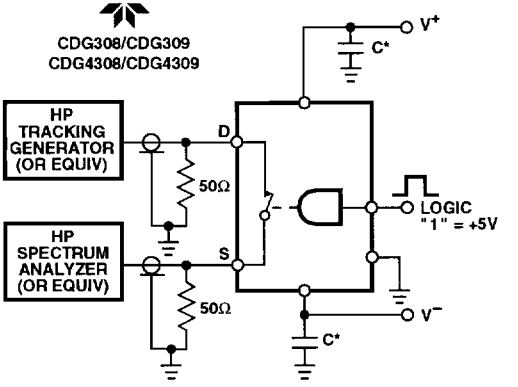
## TEST CIRCUITS (Cont.)

### Off Isolation




*NOTE: C = 0.22 µF // 10 µF

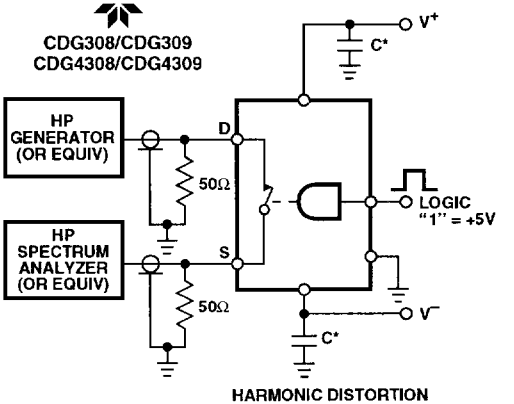
### Switch ON Resistance vs Frequency




ON RESISTANCE
20 MHz TO 100 MHz

*NOTE: C = 0.22 µF // 10 µF

### Distortion vs Frequency

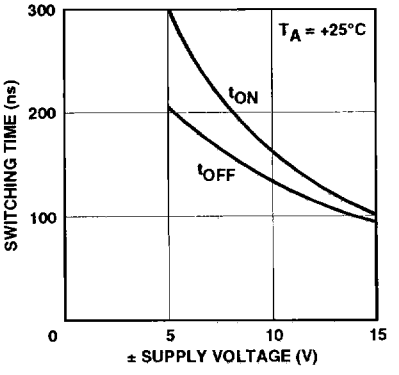



HARMONIC DISTORTION
10 MHz TO 40 MHz

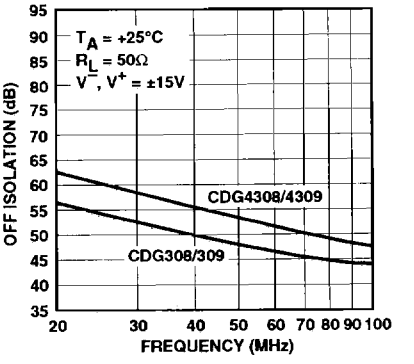
*NOTE: C = 0.22 µF // 10 µF

## TYPICAL PERFORMANCE CHARACTERISTICS

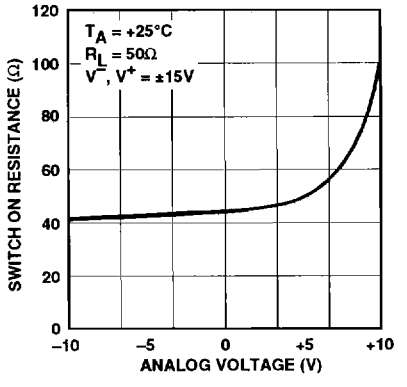
Switching Time
vs Supply Voltage



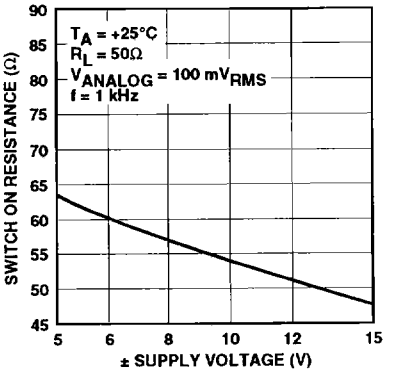

Off Isolation Rejection Ratio
vs Frequency




Switch ON Resistance
vs Analog Voltage




Switch ON Resistance
vs Supply Voltage

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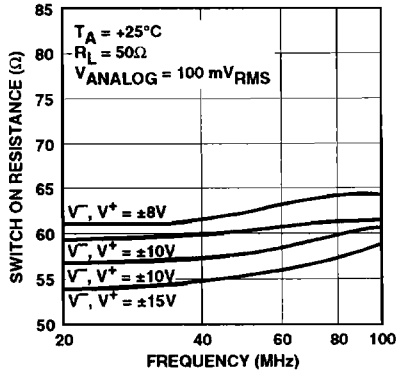
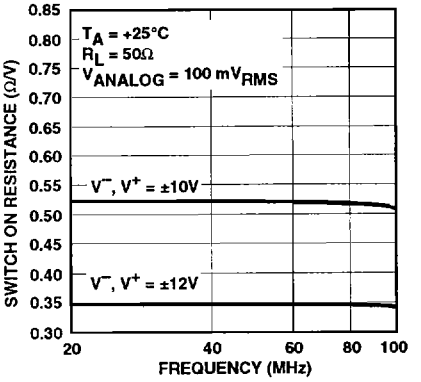
## TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

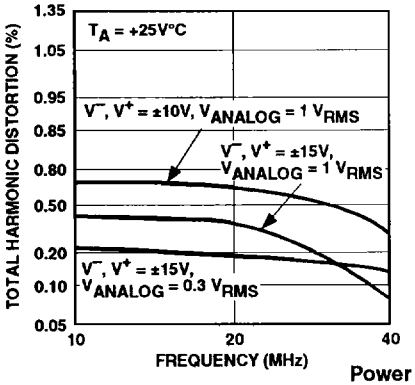
Switch ON Resistance vs Frequency



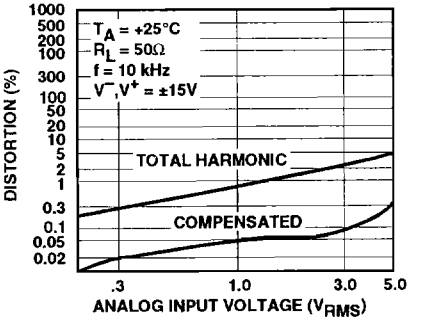

Switch ON Resistance vs Supply Voltage and Frequency




Total Harmonic Distortion vs Frequency




Distortion vs Analog Input Voltage




Power Supply Rejection Ratio vs Frequency