RICMOS™ — SOI GATE ARRAYS

HX2000 FAMILY

FEATURES

- Fabricated on Honeywell's Radiation Hardened 0.65 µm RICMOS™ IV SOI Process
- Array Sizes from 10K to 336K Available Gates (Raw)
- Supports 5V, 3.3V, or 2.5V Core Operation With Mixed Voltage I/O Buffers
- TTL or CMOS Compatible I/O
- Full Complement of Screening Flows
- Configurable Multi-Port Gate Array SRAM
- Modular Custom SRAM Drop-In Capability
- Supports Chip Level Power Down for Cold Sparing
- Supports System Speeds Beyond 100 MHz
- Total Dose Hardness of $\geq 1 \times 10^{6}$ rad(SiO_2)
- Dose Rate Upset Hardness: $\geq 1 \times 10^{10}$ rad(Si)/sec (5V)
  $\geq 1 \times 10^{9}$ rad(Si)/sec (3.3V)
  - Option Available for: $\geq 1 \times 10^{11}$ rad(Si)/sec (5V)
    $\geq 1 \times 10^{10}$ rad(Si)/sec (3.3V)
- Dose Rate Survivability $\geq 1 \times 10^{12}$ rad(Si)/sec
- SEU Immunity $\leq 1 \times 10^{-11}$ Errors/Bit-Day
- Neutron Fluence Hardness to $1 \times 10^{14}/cm^2$
- No Latchup

GENERAL DESCRIPTION

The HX2000 family of gate arrays are performance oriented sea-of-transistor gate arrays, fabricated on Honeywell's 0.65 µm RICMOS™ IV SOI process. The high density and performance characteristics of the RICMOS (Radiation Insensitive CMOS) SOI process make it possible for device operation beyond 100 MHz over the full military temperature range, even after exposure to ionizing radiation exceeding 1×10^{6} rad(SiO_2). Flip-Flops have been designed for a Soft Error Rate (SER) of less than 1×10^{-11} errors/bit/day in the Adams 10% worst case environment.

Designers can choose from a wide variety of I/O types. Output buffer options include 8 drive strengths, CMOS/TTL levels, IEEE 1149.1 boundary scan, pull-up/pull-down resistors, and three-state capability. Input buffers can be selected with CMOS/TTL/Schmitt trigger levels, IEEE 1149.1 boundary scan and pull-up/pull-down resistors. Bi-directional buffers are also available.

Another important feature is the dual voltage I/O capability in which the designer has complete flexibility in terms of placement of I/O buffers. This feature allows adjacent I/O buffers with different supplies.

Each HX2000 design is founded on our proven RICMOS ASIC library of SSI and MSI logic elements, configurable RAM cells, Flexible Supercells™ and selectable I/O pads.

The gate arrays feature a global clock network capable of handling multiple clock signals with low clock skew between registers. This family is fully compatible with Honeywell's high reliability screening procedures for QML Class Q and V requirements.

The HX2000 family provides options for configurable multi-port SRAMs. Word widths can be sized in single bit increments. A variety of SRAM read and write port options are available to serve most applications. Custom drop-in macrocells can also be implemented to further increase chip density.

The HX2000 family has a special feature to allow a chip level power down mode, in which the associated buses connected to the chip can remain active. This high impedance off-state buffer feature allows users to power down portions of their system for power savings or for "cold sparing."

Logic designers need not have a background in radiation hardening. Honeywell's VDS Toolkit and RICMOS IV libraries provide all the necessary guidance to achieve first pass design success. The VDS Toolkit supports industry standard platforms including Mentor Graphics, and VHDL simulation.

HX2000 Characteristics	HX2080	HX2160	HX2300	HX2400
Total Core Gate Count	76K	160K	295K	400K
Usable Gate Count	47K	91K	156K	200K
Maximum Die I/O	148	220	336	372
Maximum Package I/O (1)	148	216	320	372
Typical Delay		270 ps at 5.0V, 290 ps at 3.3V, 350 ps at 2.5V		
Selectable I/O		Driver, Receiver, Bi-Directional, Three-State		
I/O Interface Levels		CMOS, TTL, Schmitt Trigger		
Typical Power Dissipation, µW/Gate/MHz		0.6 @ 5.0V, 0.22 @ 3.3V, 0.12 @ 2.5V		
Operating Temperature		-55°C to 125°C		
Process Technology		RICMOS™ IV SOI		
Minimum Geometry		0.65 µm L_{eff} / 0.8 µm drawn (5V) 0.55 µm L_{eff} / 0.7 µm drawn (3.3V/2.5V)		

(1) Design and package dependent

Honeywell can perform design translations to the HX2000 arrays from other CAD platforms. Our synthesis capabilities allow customers to use familiar CAD tools and libraries, and have Honeywell map the design to RICMOS library components.

The HX2000 family of gate arrays is the right choice for your high reliability applications demanding extremely high density and radiation performance. Find out more on how Honeywell's variety of space components can meet your needs.

For technical assistance, please contact our Customer Logistics Department at 612-954-2888.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

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