16Mb Sync. Pipelined SRAM
Specification

100 TQFP with Pb & Pb-Free
(RoHS compliant)

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Document Title

512Kx36/x32 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial draft	Feb. 23. 2001	Preliminary
0.1	1. Add JTAG Scan Order	May. 10. 2001	Preliminary
0.2	1. Add x32 org and industrial temperature . 2. Add 165FBGA package	Aug. 31. 2001	Preliminary

0.3	1. Speed Bin Merge
	   From K7A1636(32/18)09A to K7A1636(32/18)00A
	2. AC parameter change
	   tOH(min)/tHZC(min) from 0.8 to 1.5 at -25
	   tOH(min)/tHZC(min) from 1.0 to 1.5 at -22
	   tOH(min)/tHZC(min) from 1.0 to 1.5 at -20
		Dec. 26. 2001	Preliminary

1.0	1. Final spec release	May. 10. 2002	Final
2.0	1. Release Icc.	May. 22. 2002	Final

part #	From	To
-25	440	470
-22	400	430
-20	370	400
-16	340	350
-14	280	290

Rev. No.	History	Draft Date	Remark
2.1	1. Delete 119BGA package. 2. Correct the Ball Size of 165 FBGA.	April 04. 2003	Final
3.0	1. Delete x32 Org. 2. Delete 165FBGA package. 3. Delelte the 225MHz and 200MHz speed bin.	Nov. 17, 2003	Final

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16Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7B161825A-QC(I)75/85	SB	3.3	7.5/8.5ns	Q : 100TQFP	C ; Commercial Temp.Range I ; Industrial Temp.Range
	K7A161800A-QC(I)25/16/14	SPB(2E1D)	3.3	250/167/138MHz		
	K7A161801A-QC(I)20/16	SPB(2E2D)	3.3	200/167MHz		
512Kx36	K7B163625A-QC(I)75/85	SB	3.3	7.5/8.5ns		
	K7A163600A-QC(I)25/16/14	SPB(2E1D)	3.3	250/167/138MHz		
	K7A163601A-QC(I)20/16	SPB(2E2D)	3.3	200/167MHz		

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512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V +0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V +0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A
- Operating in commeical and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-25	-16	-14	Unit
Cycle Time	t_{CYC}	4.0	6.0	7.2	ns
Clock Access Time	t_{CD}	2.6	3.5	4.0	ns
Output Enable Access Time	t_{OE}	2.6	3.5	4.0	ns

GENERAL DESCRIPTION

The K7A163600A and K7A161800A are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(32/18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence (linear or interleaved).
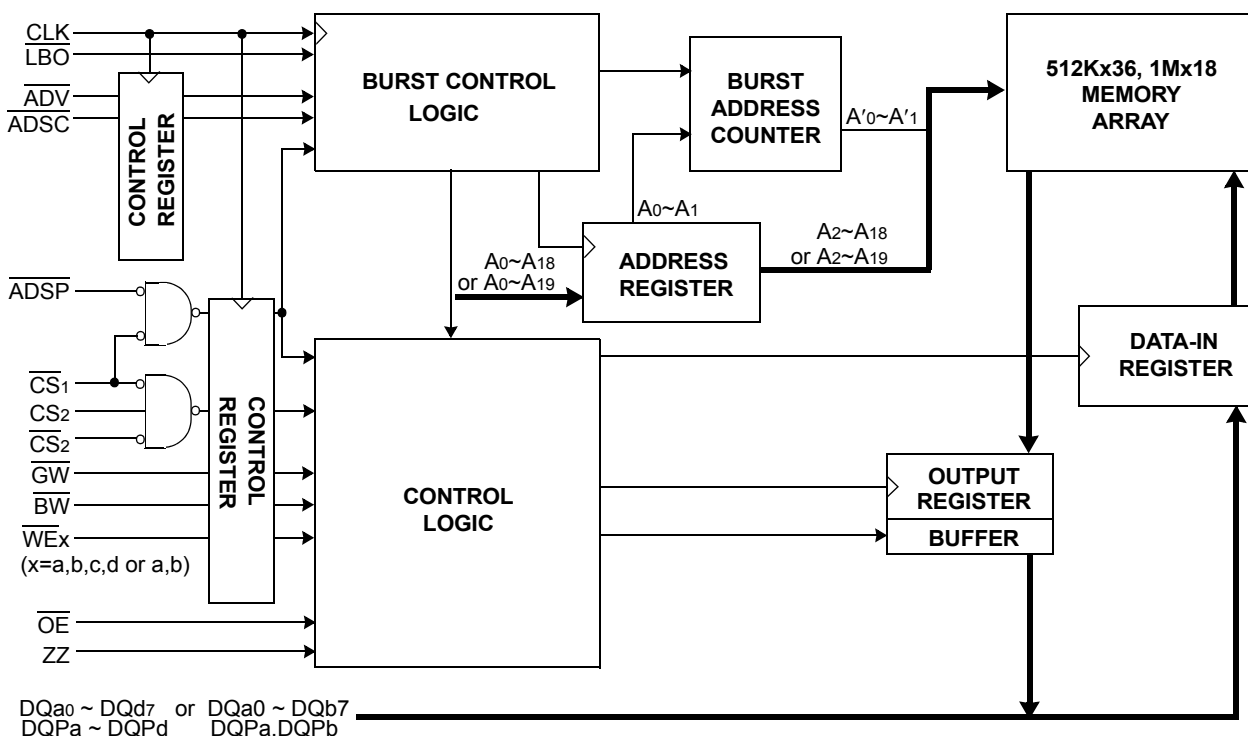
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163600A and K7A161800A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM

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K7A163600A
K7A161800A
512Kx36 & 1Mx18 Synchronous SRAM

PIN CONFIGURATION(TOP VIEW)

Top pins (left to right): A6, A7, $\overline{CS_1}$, CS_2, $\overline{WEd}$, $\overline{WEc}$, $\overline{WEb}$, $\overline{WEa}$, $\overline{CS_2}$, VDD, Vss, CLK, $\overline{GW}$, $\overline{BW}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, A8, A9

Left pins (top to bottom):
- 1 NC/DQPc
- 2 DQc0
- 3 DQc1
- 4 VDDQ
- 5 VSSQ
- 6 DQc2
- 7 DQc3
- 8 DQc4
- 9 DQc5
- 10 VSSQ
- 11 VDDQ
- 12 DQc6
- 13 DQc7
- 14 N.C.
- 15 VDD
- 16 N.C.
- 17 VSS
- 18 DQd0
- 19 DQd1
- 20 VDDQ
- 21 VSSQ
- 22 DQd2
- 23 DQd3
- 24 DQd4
- 25 DQd5
- 26 VSSQ
- 27 VDDQ
- 28 DQd6
- 29 DQd7
- 30 NC/DQPd

100 Pin TQFP
(20mm x 14mm)
K7A163600A(512Kx36)

Right pins (top to bottom):
- 80 DQPb/NC
- 79 DQb7
- 78 DQb6
- 77 VDDQ
- 76 VSSQ
- 75 DQb5
- 74 DQb4
- 73 DQb3
- 72 DQb2
- 71 VSSQ
- 70 VDDQ
- 69 DQb1
- 68 DQb0
- 67 VSS
- 66 N.C.
- 65 VDD
- 64 ZZ
- 63 DQa7
- 62 DQa6
- 61 VDDQ
- 60 VSSQ
- 59 DQa5
- 58 DQa4
- 57 DQa3
- 56 DQa2
- 55 VSSQ
- 54 VDDQ
- 53 DQa1
- 52 DQa0
- 51 DQPa/NC

Bottom pins (pins 31-50, left to right): $\overline{LBO}$, A5, A4, A3, A2, A1, A0, N.C., N.C., Vss, VDD, A18, A17, A10, A11, A12, A13, A14, A15, A16

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,81,82,99,100	VDD Vss	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
$\overline{ADSP}$	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS_2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
$\overline{CS_2}$	Chip Select	92	DQPa~Pd		51,80,1,30
$\overline{WEx}$(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	or N.C		
$\overline{OE}$	Output Enable	86	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88		(3.3V or 2.5V)	
$\overline{BW}$	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Note : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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PIN CONFIGURATION(TOP VIEW)

100 Pin TQFP
(20mm x 14mm)
K7A161800A(1Mx18)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{19}	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50 80,81,82,99,100	V_{DD} V_{SS}	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29
$\overline{ADSP}$	Address Status Processor	84			30,38,39,51,52,53,56,57
$\overline{ADSC}$	Address Status Controller	85			66,75,78,79,95,96
CLK	Clock	89			
$\overline{CS_1}$	Chip Select	98	$DQa_0 \sim a_7$	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS_2	Chip Select	97	$DQb_0 \sim b_7$		8,9,12,13,18,19,22,23
$\overline{CS_2}$	Chip Select	92	DQPa, Pb		74,24
$\overline{WEx}(x=a,b)$	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	V_{DDQ}	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

Note : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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K7A163600A
K7A161800A

512Kx36 & 1Mx18 Synchronous SRAM

FUNCTION DESCRIPTION

The K7A163600A and K7A161800A are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WEx}$ and $\overline{ADSC}$)using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WEx}$ are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}_1$.

All byte write is done by $\overline{GW}$(regaedless of $\overline{BW}$ and $\overline{WEx}$.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WEx}$ when $\overline{GW}$ is high.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WEx}$. $\overline{WEx}$ are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WEx}$ are sampled Low(regaedless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WEx}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WEx}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$ or $\overline{WEd}$) sampled low. The $\overline{WEa}$ control $DQa_0 \sim DQa_7$ and DQPa, $\overline{WEb}$ controls $DQb_0 \sim DQb_7$ and DQPb, $\overline{WEc}$ controls $DQc_0 \sim DQc_7$ and DQPc, and $\overline{WEd}$ control $DQd_0 \sim DQd_7$ and DQPd. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WEx}$ are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes
1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

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TRUTH TABLES
SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".   2. The rising edge of clock is symbolized by ↑.

    3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.

     $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

    4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

    2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

    2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}		V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}		V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}		V_{IN}	-0.3 to V_{DD}+0.3	V
Voltage on I/O Pin Relative to V_{SS}		V_{IO}	-0.3 to V_{DDQ}+0.3	V
Power Dissipation		P_D	1.6	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_{OPR}	0 to 70	°C
	Industrial	T_{OPR}	-40 to 85	°C
Storage Temperature Range Under Bias		T_{BIAS}	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O$(0°C \leq T_A \leq 70°C)$

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

OPERATING CONDITIONS at 2.5V I/O$(0°C \leq T_A \leq 70°C)$

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*$(T_A=25°C, f=1MHz)$

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

*Note : Sampled not 100% tested.

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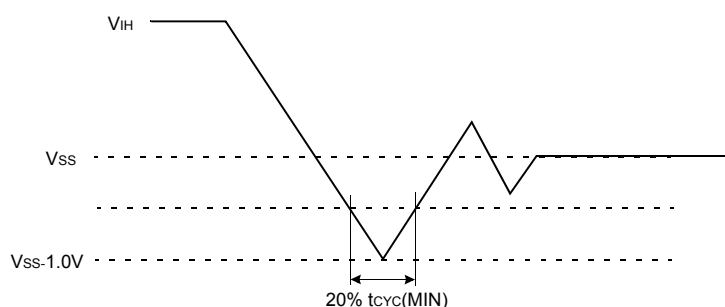
DC ELECTRICAL CHARACTERISTICS(V_DD=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	I_IL	V_DD = Max ; V_IN=Vss to V_DD		-2	+2	μA	
Output Leakage Current	I_OL	Output Disabled, V_OUT=Vss to V_DDQ		-2	+2	μA	
Operating Current	I_CC	Device Selected, I_OUT=0mA, ZZ≤V_IL , Cycle Time ≥ tcyc Min	-25	-	470	mA	1,2
			-16	-	350		
			-14	-	290		
Standby Current	I_SB	Device deselected, I_OUT=0mA, ZZ≤V_IL, f=Max, All Inputs≤0.2V or ≥ V_DD-0.2V	-25	-	120	mA	
			-16	-	90		
			-14	-	90		
	I_SB1	Device deselected, I_OUT=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_DD-0.2V or 0.2V)		-	70	mA	
	I_SB2	Device deselected, I_OUT=0mA, ZZ≥V_DD-0.2V, f=Max, All Inputs≤V_IL or ≥V_IH		-	60	mA	
Output Low Voltage(3.3V I/O)	V_OL	I_OL=8.0mA		-	0.4	V	
Output High Voltage(3.3V I/O)	V_OH	I_OH=-4.0mA		2.4	-	V	
Output Low Voltage(2.5V I/O)	V_OL	I_OL=1.0mA		-	0.4	V	
Output High Voltage(2.5V I/O)	V_OH	I_OH=-1.0mA		2.0	-	V	
Input Low Voltage(3.3V I/O)	V_IL			-0.3*	0.8	V	
nput High Voltage(3.3V I/O)	V_IH			2.0	V_DD+0.3**	V	3
Input Low Voltage(2.5V I/O)	V_IL			-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_IH			1.7	V_DD+0.3**	V	3

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. In Case of I/O Pins, the Max. V_IH=V_DDQ+0.3V.
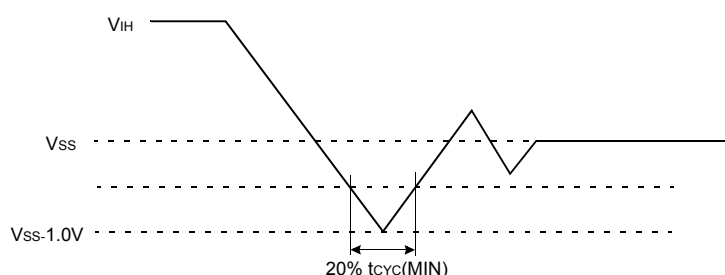
TEST CONDITIONS
(V_DD=3.3V+0.165V/-0.165V,V_DDQ=3.3V+0.165/-0.165V or V_DD=3.3V+0.165V/-0.165V,V_DDQ=2.5V+0.4V/-0.125V, T_A=0to70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_DDQ/2
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.

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Output Load(A)

Output Load(B),
(for t$_{LZC}$, t$_{LZOE}$, t$_{HZOE}$ & t$_{HZC}$)
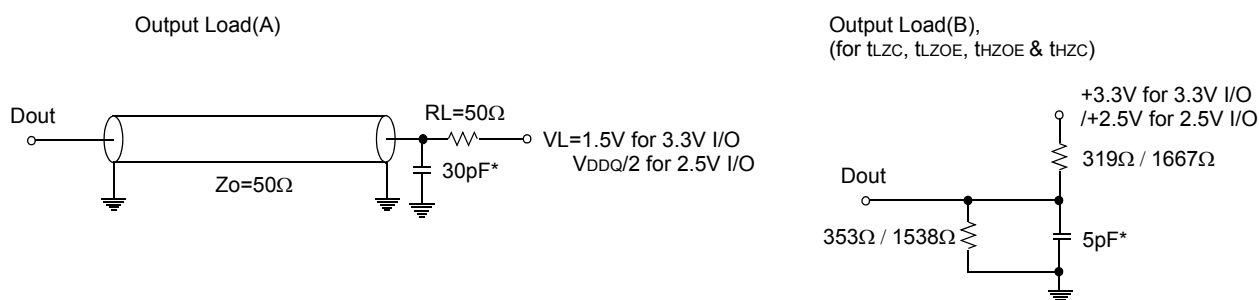
* Including Scope and Jig Capacitance

Fig. 1

AC TIING CHARACTERISTICS(V$_{DD}$=3.3V+0.165V/-0.165V, T$_A$=0°C to +70°C)

Parameter	Symbol	-25		-16		-14		Unit
		MIN	MAX	Min	Max	Min	Max	
Cycle Time	t$_{CYC}$	4.0	-	6.0	-	7.2	-	ns
Clock Access Time	t$_{CD}$	-	2.6	-	3.5	-	4.0	ns
Output Enable to Data Valid	t$_{OE}$	-	2.6	-	3.5	-	4.0	ns
Clock High to Output Low-Z	t$_{LZC}$	0	-	0	-	0	-	ns
Output Hold from Clock High	t$_{OH}$	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t$_{LZOE}$	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t$_{HZOE}$	-	2.6	-	3.0	-	3.5	ns
Clock High to Output High-Z	t$_{HZC}$	1.5	2.6	1.5	3.0	1.5	3.5	ns
Clock High Pulse Width	t$_{CH}$	1.7	-	2.1	-	2.5	-	ns
Clock Low Pulse Width	t$_{CL}$	1.7	-	2.1	-	2.5	-	ns
Address Setup to Clock High	t$_{AS}$	1.2	-	1.5	-	1.5	-	ns
Address Status Setup to Clock High	t$_{SS}$	1.2	-	1.5	-	1.5	-	ns
Data Setup to Clock High	t$_{DS}$	1.2	-	1.5	-	1.5	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t$_{WS}$	1.2	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	t$_{ADVS}$	1.2	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	t$_{CSS}$	1.2	-	1.5	-	1.5	-	ns
Address Hold from Clock High	t$_{AH}$	0.3	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t$_{SH}$	0.3	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t$_{DH}$	0.3	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t$_{WH}$	0.3	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t$_{ADVH}$	0.3	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t$_{CSH}$	0.3	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t$_{PDS}$	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t$_{PUS}$	2	-	2	-	2	-	cycle

Notes : 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
4. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

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TIMING WAVEFORM OF READ CYCLE

NOTES : $\overline{\text{WRITE}}$ = L means $\overline{\text{GW}}$ = L, or GW = H, $\overline{\text{BW}}$ = L, $\overline{\text{WEx}}$ = L

$\overline{\text{CS}}$ = L means $\overline{\text{CS}_1}$ = L, CS_2 = H and $\overline{\text{CS}_2}$ = L

$\overline{\text{CS}}$ = H means $\overline{\text{CS}_1}$ = H, or CS_2 = H, or $\overline{\text{CS}_2}$ = L and CS_1 = L, and CS_2 = L

Don't Care

Undefined

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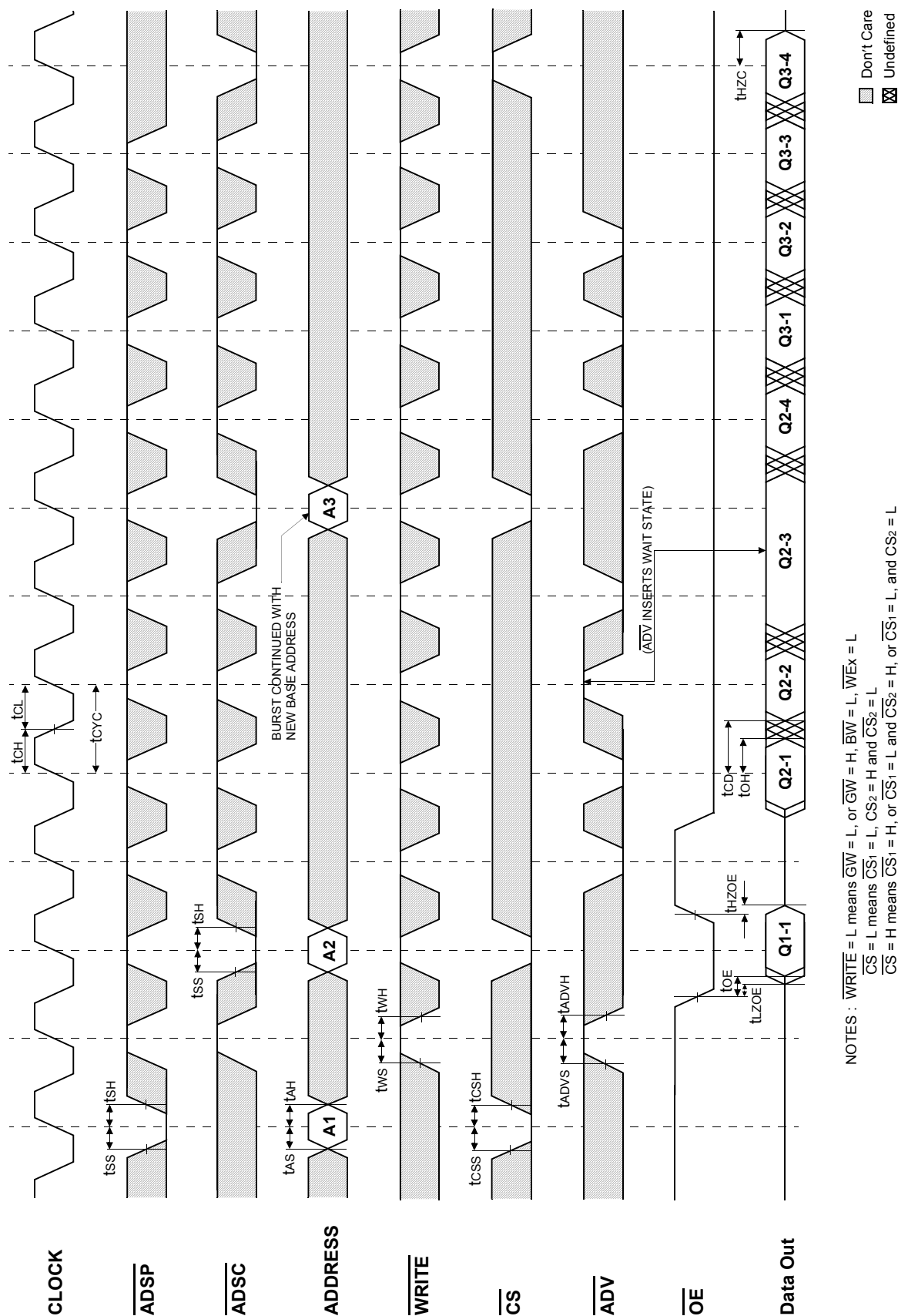
TIMING WAVEFORM OF WRTE CYCLE

- Don't Care
- Undefined

Signals: CLOCK, ADSP, ADSC, ADDRESS, WRITE, CS, ADV, OE, Data In, Data Out

Timing parameters: tCH, tCL, tCYC, tSS, tSH, tAS, tAH, tCSS, tCSH, tWS, tWH, tADVS, tADVH, tDS, tDH, tHZOE

Address: A1, A2, A3

(ADSC EXTENDED BURST)
(ADV SUSPENDS BURST)

Data In: D1-1, D2-1, D2-2, D2-2, D2-3, D2-4, D3-1, D3-2, D3-3, D3-4

Data Out: Q0-3, Q0-4

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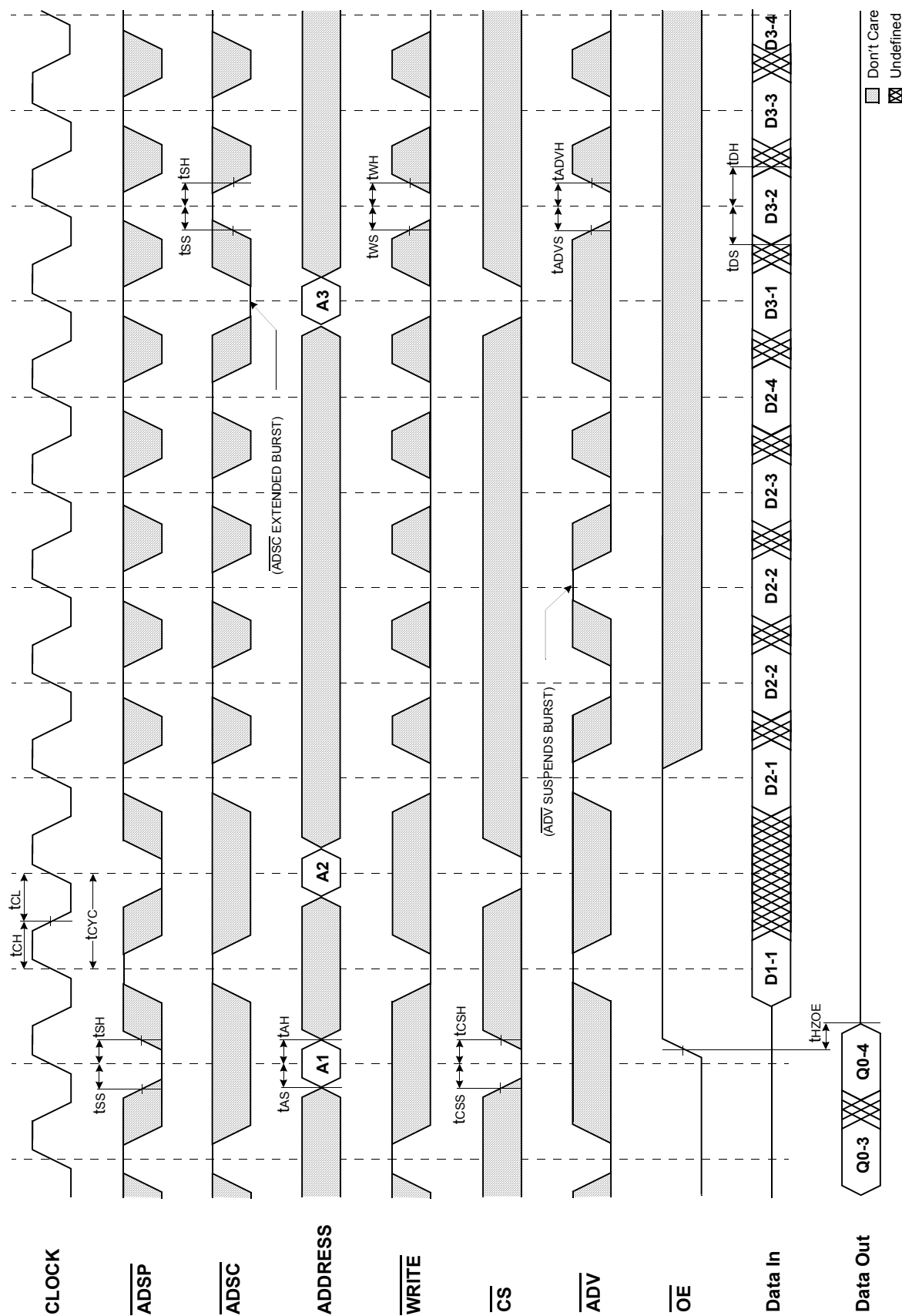
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED , ADSC=HIGH)

CLOCK

ADSP

ADDRESS

WRITE

CS

ADV

OE

Data In

Data Out

Don't Care
Undefined

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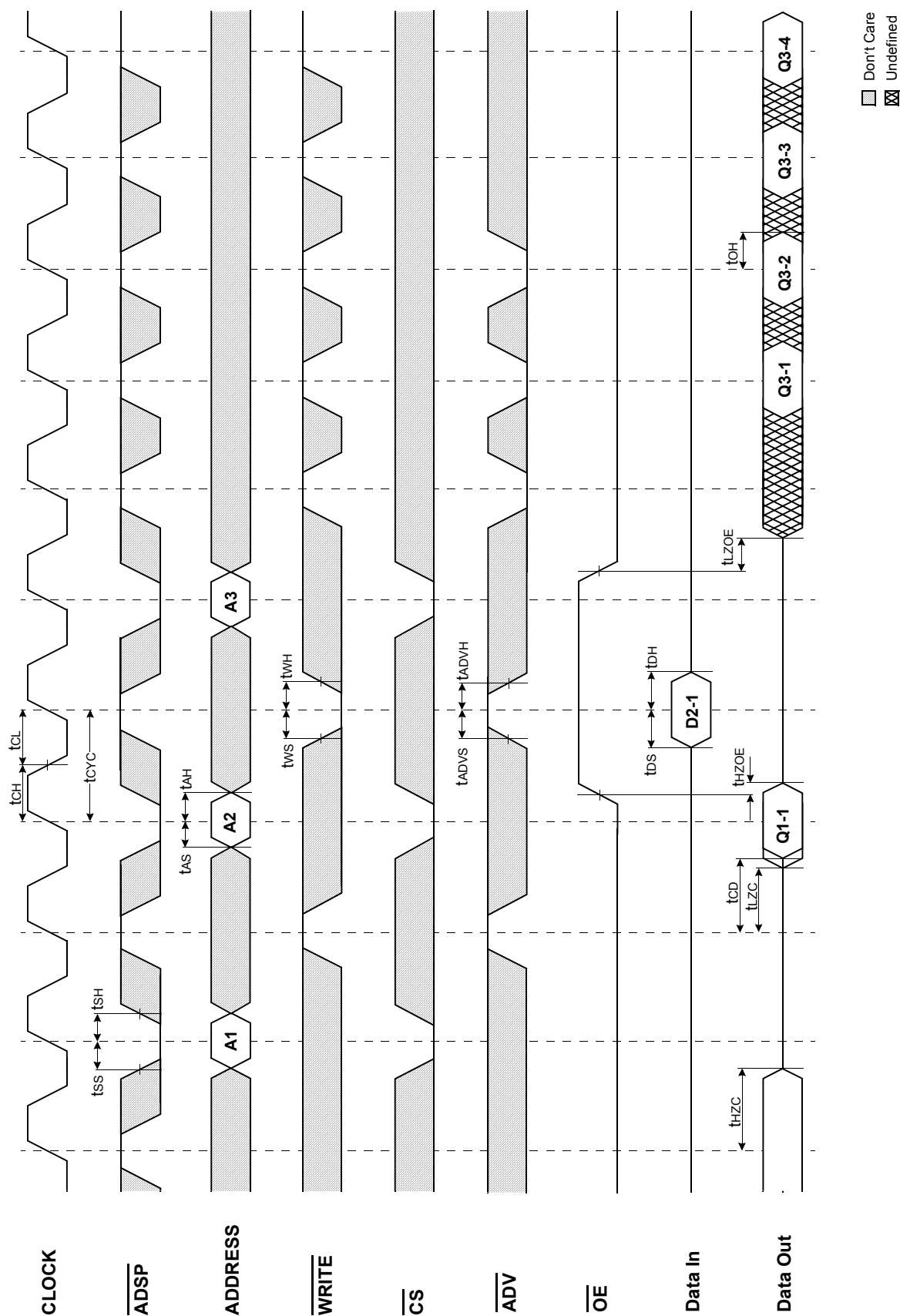
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED , ADSP=HIGH)

Don't Care
Undefined

CLOCK
ADSC
ADDRESS
WRITE
CS
ADV
OE
Data Out
Data In

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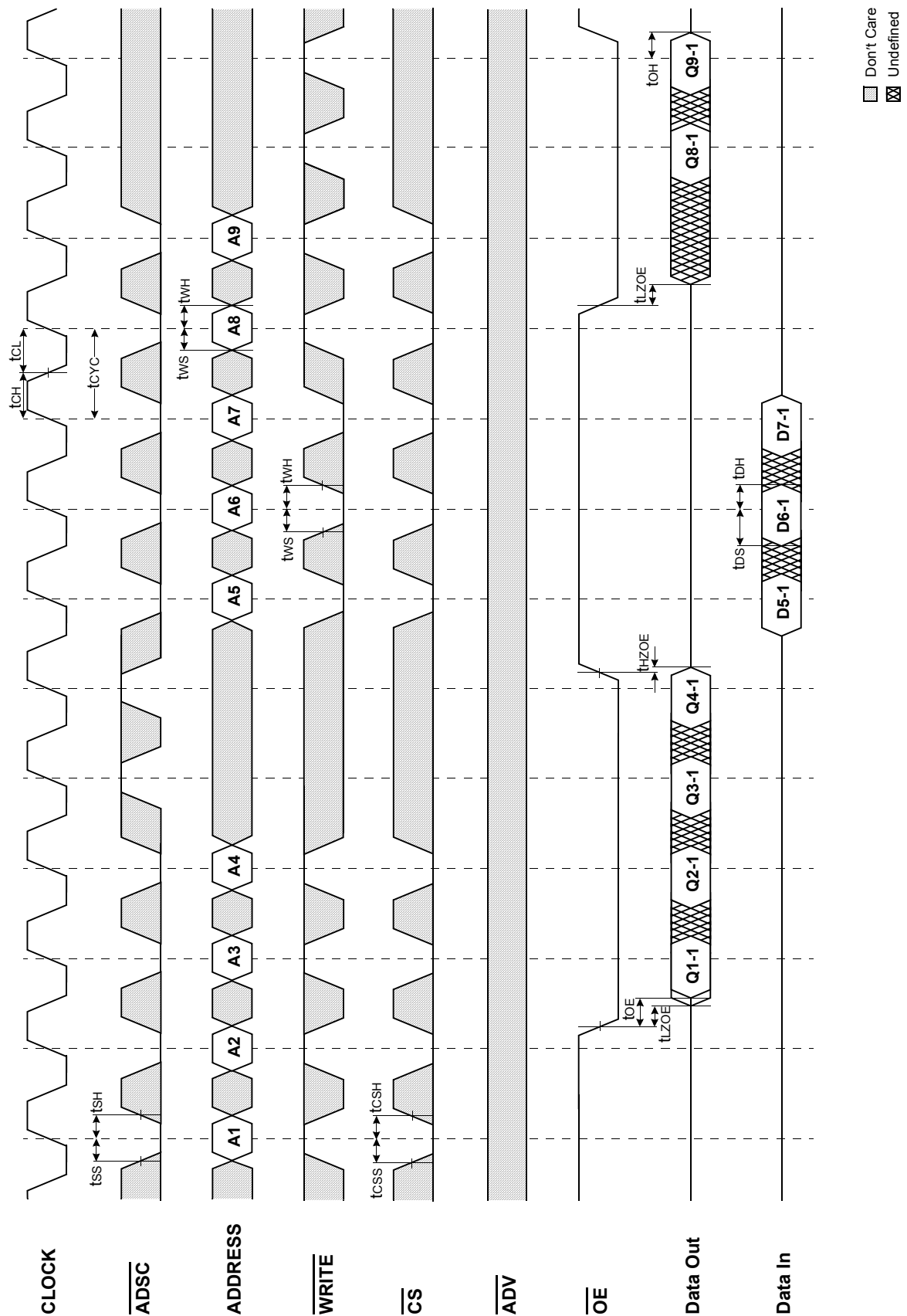
TIMING WAVEFORM OF POWER DOWN CYCLE

CLOCK

$\overline{ADSP}$

$\overline{ADSC}$

ADDRESS

$\overline{WRITE}$

$\overline{CS}$

$\overline{ADV}$

$\overline{OE}$

Data In

Data Out

ZZ

tSS, tSH, tAS, tAH, tCSS, tCSH, tSS, tCH, tCL, tCYC, tWS, tWH, A1, A2, tOE, tLZOE, tHZOE, tLZC, tPDS, tPUS, Q1-1, D2-1, D2-2

ZZ Setup Cycle, Sleep State, ZZ Recovery Cycle, Normal Operation Mode

Don't Care, Undefined

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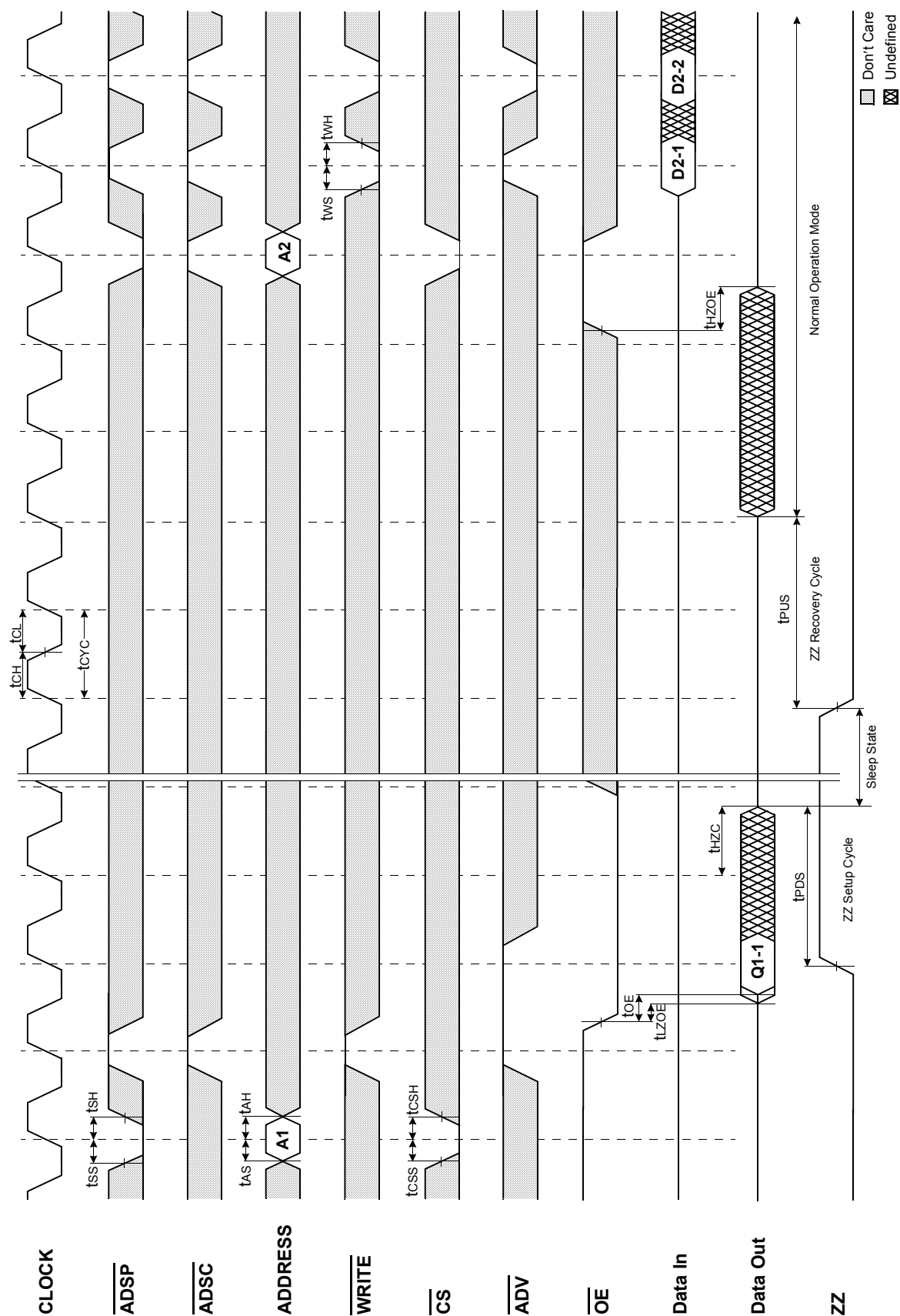
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 512Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion.
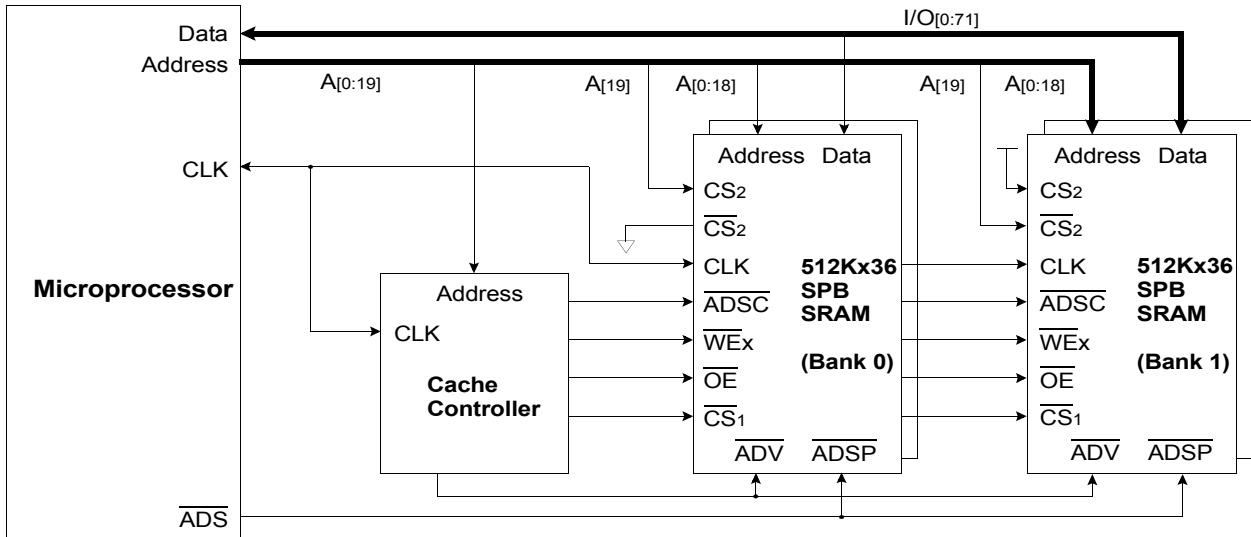This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.

Data
Address

I/O[0:71]

A[0:19]   A[19]   A[0:18]   A[19]   A[0:18]

CLK

Microprocessor

Address   Data   Address   Data

CS_2 CS_2
$\overline{CS_2}$ $\overline{CS_2}$
CLK   512Kx36   CLK   512Kx36
$\overline{ADSC}$ SPB $\overline{ADSC}$ SPB
$\overline{WE}x$ SRAM $\overline{WE}x$ SRAM
$\overline{OE}$ $\overline{OE}$
$\overline{CS_1}$ (Bank 0) $\overline{CS_1}$ (Bank 1)

$\overline{ADV}$ $\overline{ADSP}$ $\overline{ADV}$ $\overline{ADSP}$

Address
CLK

Cache
Controller

$\overline{ADS}$

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)

Clock

$\overline{ADSP}$

t_{SS} t_{SH}

ADDRESS
[0:n]

A1   A2

t_{AS} t_{AH}

WRITE

t_{WS} t_{WH}

$\overline{CS_1}$

t_{CSS} t_{CSH}

A_{n+1}

Bank 0 is selected by CS_2, and Bank 1 deselected by $\overline{CS_2}$

Bank 0 is deselected by CS_2, and Bank 1 selected by $\overline{CS_2}$

$\overline{ADV}$

t_{ADVS} t_{ADVH}

$\overline{OE}$

t_{OE}

t_{HZC}

t_{LZOE}

Data Out
(Bank 0)

Q1-1   Q1-2   Q1-3   Q1-4

t_{CD}
t_{LZC}

Data Out
(Bank 1)

Q2-1   Q2-2   Q2-3   Q2-4

*Notes : n = 14 32K depth ,   15   64K depth
16 128K depth ,   17   256K depth
18 512K depth ,   19   1M depth

Don't Care   Undefined

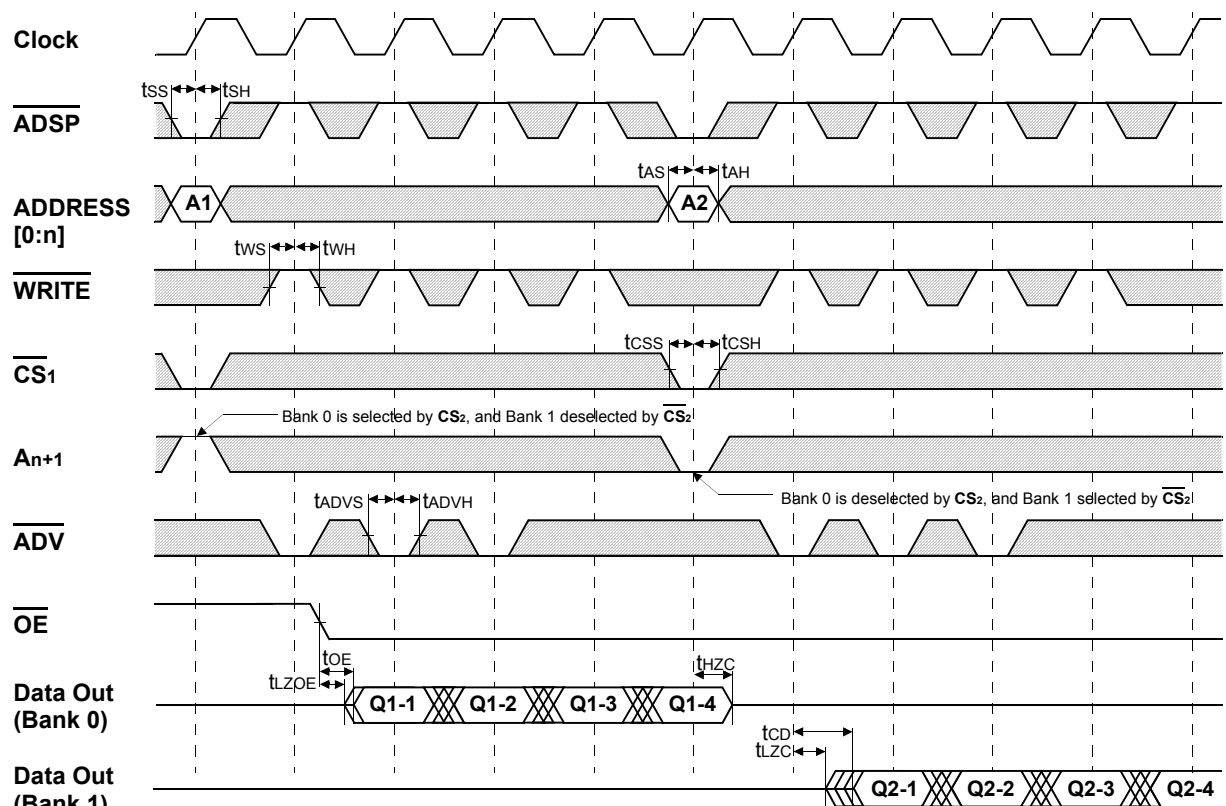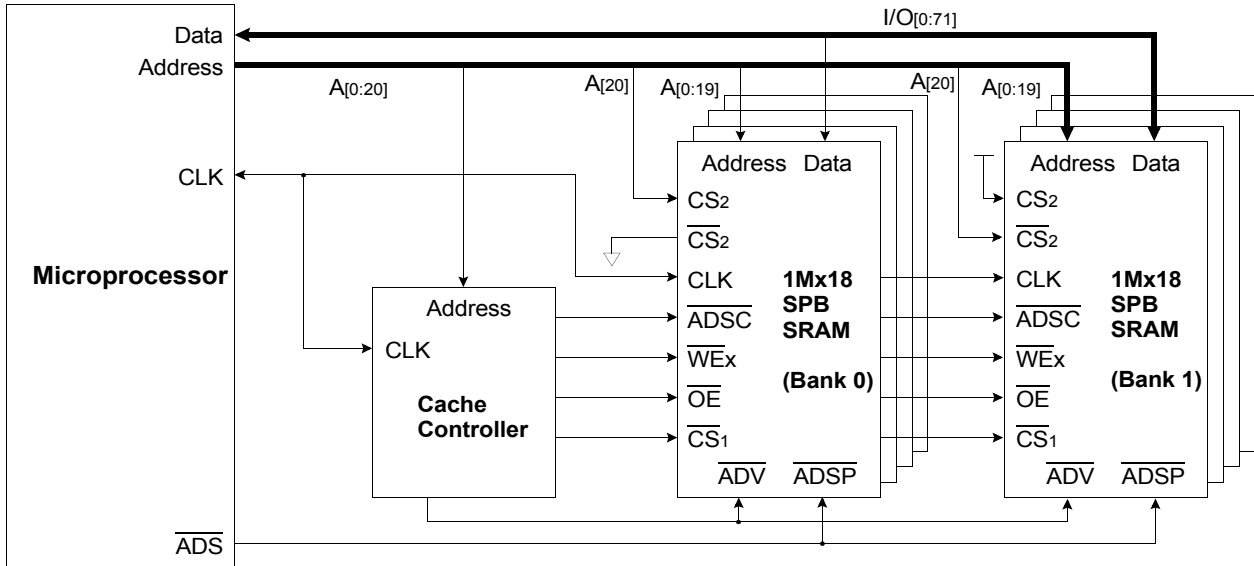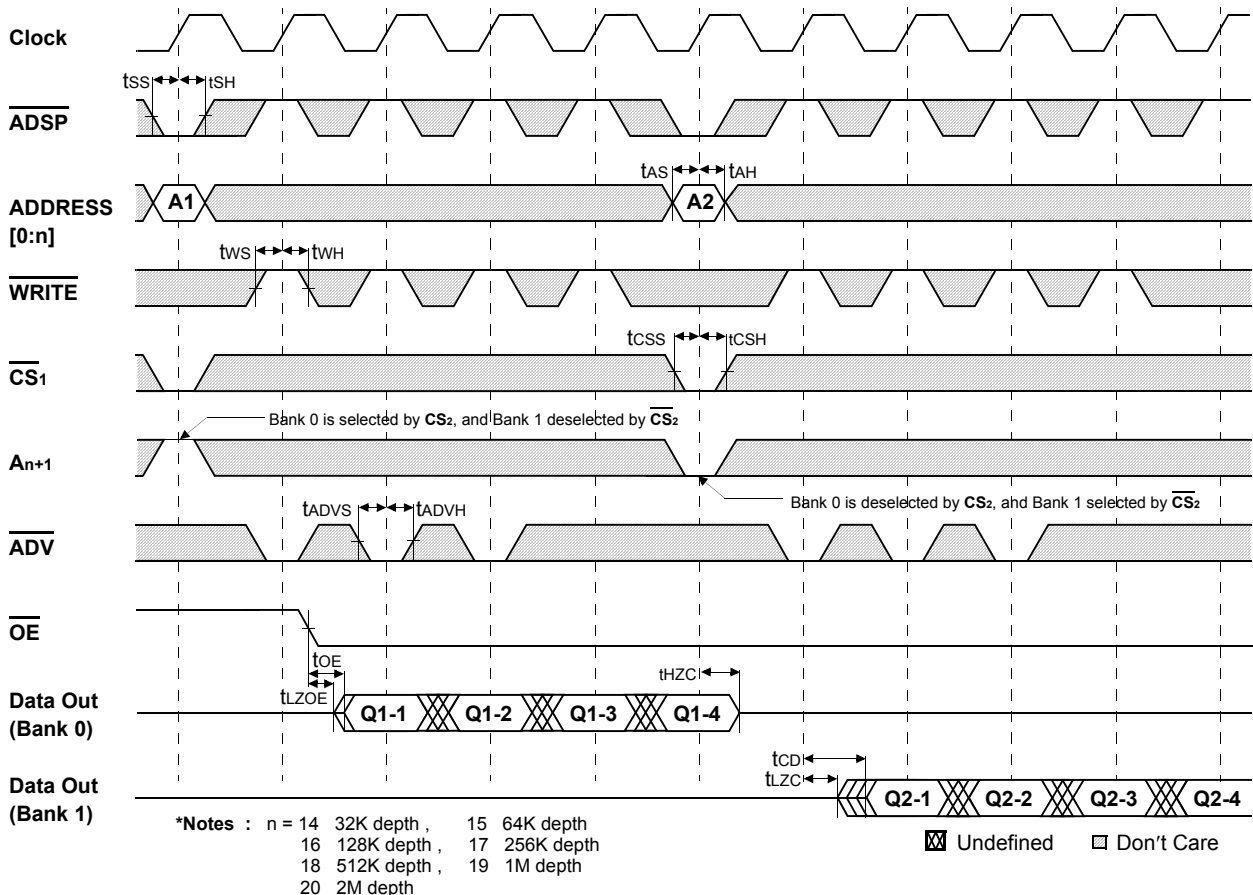**SAMSUNG**

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APPLICATION INFORMATION
DEPTH EXPANSION

The Samsung 1Mx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)
($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)

*Notes : n = 14   32K depth ,   15   64K depth
          16   128K depth ,   17   256K depth
          18   512K depth ,   19   1M depth
          20   2M depth

☒ Undefined   ☐ Don't Care

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PACKAGE DIMENSIONS

100-TQFP-1420A

Units ; millimeters/Inches

22.00 ±0.30

20.00 ±0.20

0~8°

0.127 +0.10 -0.05

16.00 ±0.30

14.00 ±0.20

0.10 MAX

(0.83)

0.50 ±0.10

#1

0.65

0.30 ±0.10

(0.58)

0.10 MAX

1.40 ±0.10   1.60 MAX

0.05 MIN

0.50 ±0.10

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