Ordering number : ENN*6748

CMOS IC

# LC86E7148

## 8-Bit Single Chip Microcontroller with the UVEPROM

**Preliminary**

## Overview

The LC86E7148 is a CMOS 8-bit single chip microcontroller with UVEPROM for the LC867100 series. This microcontroller has the function and the pin description of the LC867100 series mask ROM version, and 48K-byte EPROM. The program data is rewritable. It is suitable to develop the program.

## Features

(1) Option switching by EPROM data
The option function of the LC867100 series can be specified by the EPROM data.
LC86E7148 can be checked the functions of the trial pieces using the mass production board.
(2) Internal EPROM capacity : 49152 bytes
(3) Internal RAM capacity : 1152 bytes
Used EPROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86E7148.

| Mask ROM version | EPROM capacity | RAM capacity |
|---|---|---|
| LC867148 | 49152 bytes | 1152 bytes |
| LC867140 | 40960 bytes | 1152 bytes |
| LC867132 | 32768 bytes | 768 bytes |
| LC867128 | 28672 bytes | 768 bytes |
| LC867124 | 24576 bytes | 768 bytes |
| LC867120 | 20480 bytes | 640 bytes |
| LC867116 | 16384 bytes | 640 bytes |
| LC867112 | 12288 bytes | 512 bytes |
| LC867108 | 8192 bytes | 512 bytes |

(4) Operating supply voltage : 4.5V to 6.0V
(5) Instruction cycle time : 1µs to 366µs
(6) Operating temperature : +10°C to +40°C
(7) The pin compatible with the LC867100 series mask ROM devices
(8) Applicable mask ROM version : LC867148/LC867140/LC867132/LC867128/LC867124/LC867120 /LC867116/LC867112/LC867108
(9) Factory shipment : QIC80S




SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Notice for use

At using, take notice of the followings.

(1) A point of difference LC86E7148 and LC867100 series

| Item | LC86E7148 | LC867148/40/32/28/24/20/16/12/08 |
|---|---|---|
| Port form at reset | Please refer 'Port form at reset' on next page. | |
| Operation after reset releasing | The option is specified until 3ms after going to a 'H' level to the reset terminal by degrees. The program is executed from 00H of the program counter. | The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal. |
| Operating supply voltage range (VDD) | 4.5V to 6.0V | 2.5V to 6.0V |
| Total output current [∑IOAL(2)] [∑IOAL(3)] | Refer to 'electrical characteristics' on the semiconductor news. | |
| Power dessipation | | |

LC86E7148 uses 256 bytes that is addressed on 0FF00H to FFFFH in the program memory as the option configuration data area. This option configuration can execute all options which LC867100 series have. Next tables show the options that correspond and not correspond to LC86E7148.

• A kind of the option corresponding of the LC86E7148

| A kind of option | Pins, Circuits | Contents of the option |
|---|---|---|
| Input/output form of input/output ports | Port 0 (specified in a bit) | 1. Input : No Pull-up MOS Tr.<br>Output: N-channel open drain *1 |
| | | 2. Input : Pull-up MOS Tr.<br>Output: CMOS *2 |
| | Port 1 (specified in a bit) *1 | 1. Input : Programmable pull-up MOS Tr.<br>Output: N-channel open drain<br>2. Input : Programmable pull-up MOS Tr.<br>Output : CMOS |
| Pull-up MOS Tr. of input port | Port 7 (specified in a bit) *1<br>Each of P74 and P75 has no option | 1. No Pull-up MOS Tr.<br>2. Pull-up MOS Tr. |

*1) Specified in a bit.
*2) Specified in nibble unit. Pull-up MOS Tr. is not provided in N-channel open drain output port.

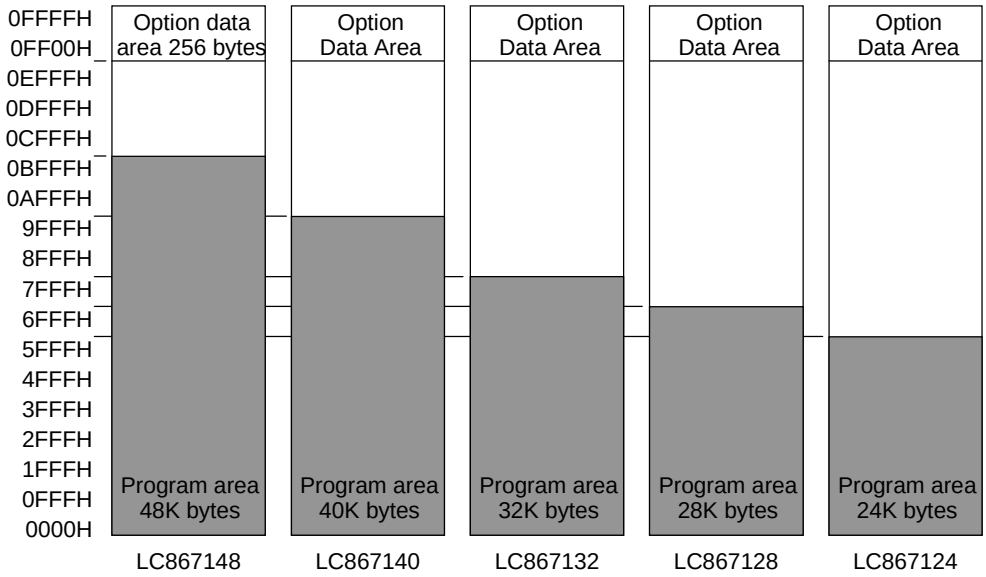
The port operation related the option is different at reset. Refer to the next table.

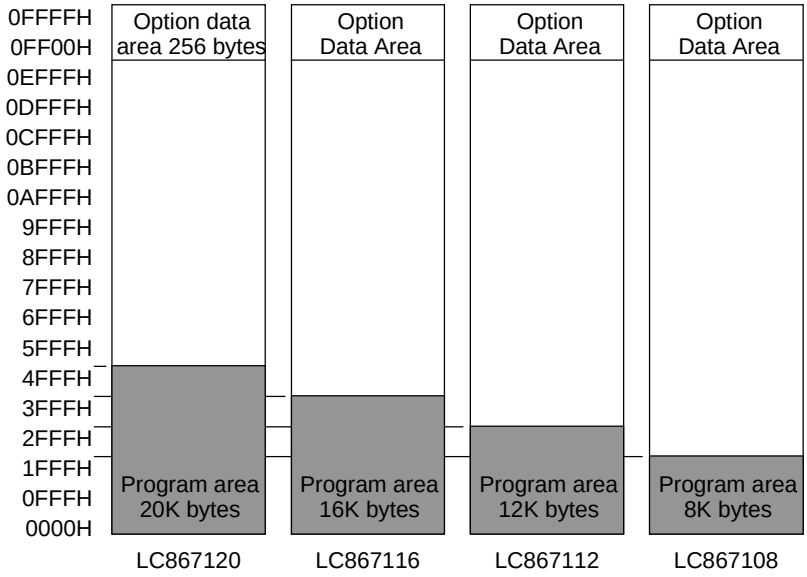
(2) Option

The option data is created by the option specified program “SU86K.EXE”. The created option data is linked to the program area by linkage loader “L86K.EXE”.

(3) ROM space

LC86E7148 and LC867100 series use 256 bytes that is addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. These program memory capacity are 49152 bytes that is addressed on 0000H to 0BFFFH.



## How to use

(1) Specification of option

The LC86E7148 must be programmed after specifying option data. The option is specified by "SU86K.EXE". The specified option file and the file created by our macro assembler "M86K.EXE" are linked by our linkage loader "L86K.EXE" which creates .HEX file, then the option code is put in the option specified area (0FF00H to 0FFFFH) of its .HEX file.

(2) How to program for the EPROM

The LC86E7148 can be programmed by EPROM programmer with attachment ; W86EP7148Q

• Recommended EPROM programmer

| Productor | EPROM programmer |
|---|---|
| Advantest | R4945, R4944, R4943 |
| Andou | AF-9704 |
| AVAL | PKW-1100, PKW-3000 |
| Minato electronics | MODEL1890A |

• "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set to "0 to 0FFFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function

"Data security" is the disabled function to read the data of the EPROM.

The following is the process in order to execute the data security.

1. Set 'ON' the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

• Data security is not executed when the data of all address have 'FFH' at the sequence 2 above.
• The programming by a sequential operation "BLANK=>PROGRAM=>VERIFY" cannot be executed data security at the sequence 2 above.
• Set to 'OFF' the jumper after executing the data security.

(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

(5) Shielding

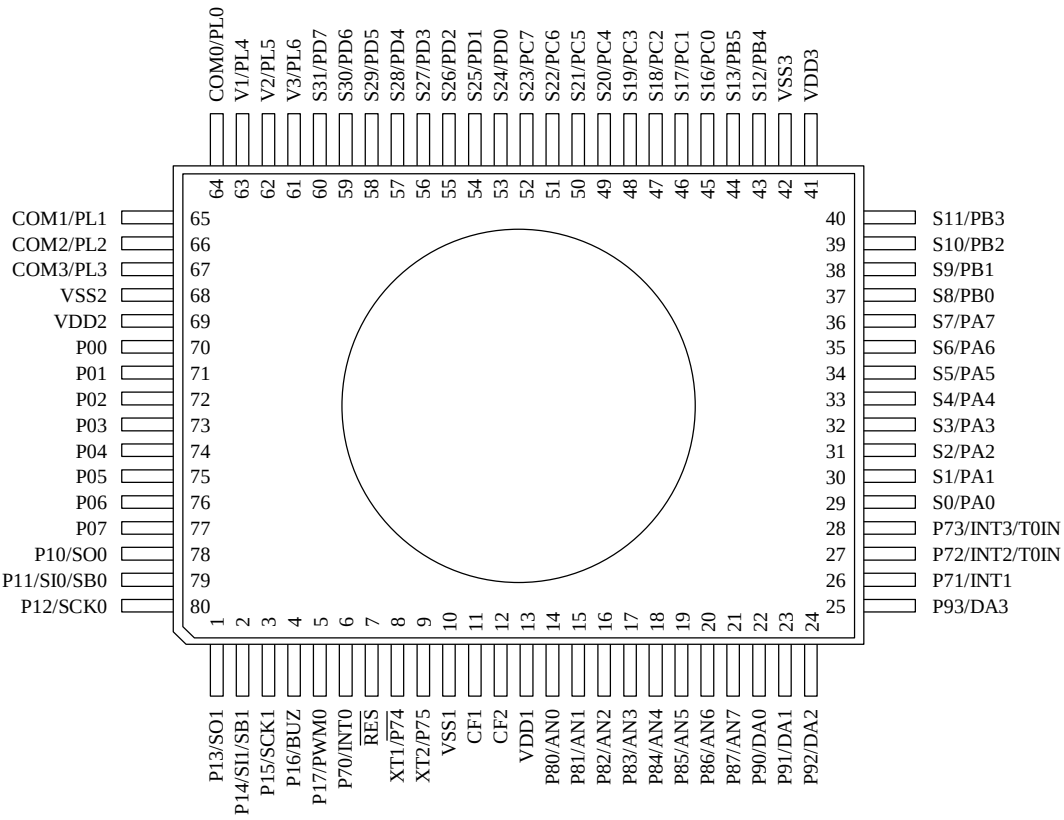
The UVEPROM (ultraviolet erasable programmable ROM) is in it. Put the seal on the window in use.

Data security

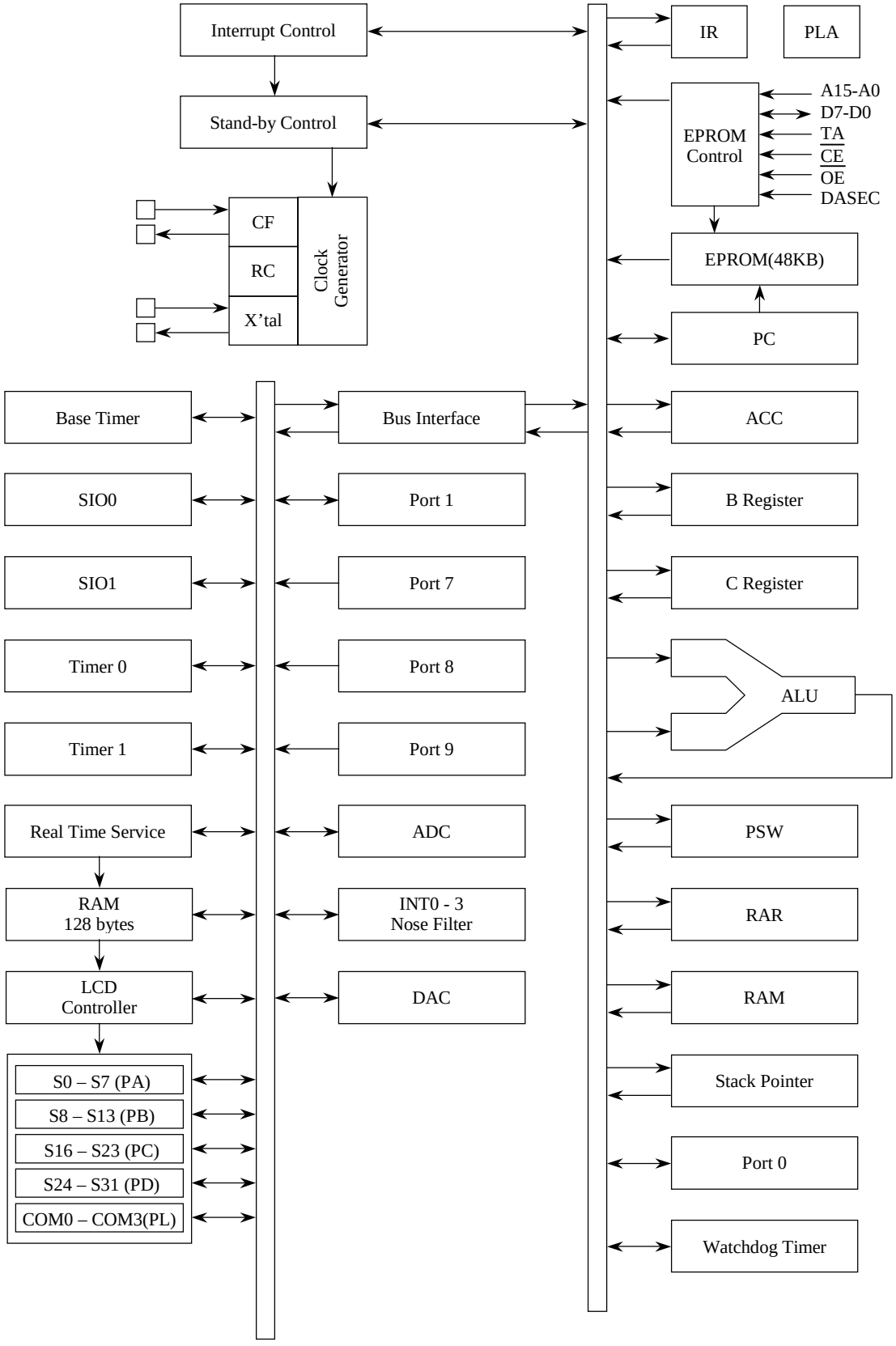
Not data security

W86EP7148Q

## Pin Assignment



## System Block Diagram



## Pin Description

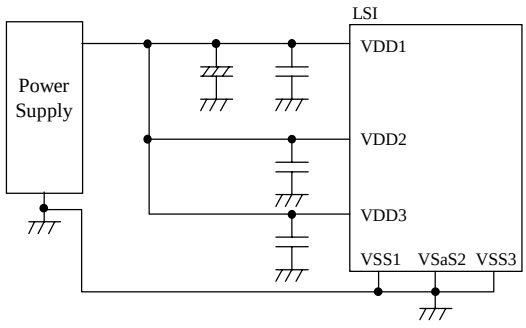
<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th><th>PROM mode</th></tr>
<tr><td>VSS1 *1</td><td>-</td><td>Power pin (–)</td><td>-</td><td></td></tr>
<tr><td>VSS2 *1</td><td>-</td><td>Power pin (–)</td><td>-</td><td></td></tr>
<tr><td>VSS3 *1</td><td>-</td><td>Power pin (–)</td><td>-</td><td></td></tr>
<tr><td>VDD1 *1</td><td>-</td><td>Power pin (+)</td><td>-</td><td></td></tr>
<tr><td>VDD2 *1</td><td>-</td><td>Power pin (+)</td><td>-</td><td></td></tr>
<tr><td>VDD3 *1</td><td>-</td><td>Power pin (+)</td><td>-</td><td></td></tr>
<tr><td>PORT0<br>P00 - P07</td><td>I/O</td><td>• 8-bit input/output port<br>Input/output in nibble units<br>• Input for port 0 interrupt<br>• Input for HOLD release</td><td>• Pull-up resistor :<br>Provided/Not provided<br>(specified in nibble units)<br>• Output form (P00 – P07) :<br>CMOS/N-channel open drain<br>(specified in a bit)</td><td></td></tr>
<tr><td>PORT1<br>P10 - P17</td><td>I/O</td><td>• 8-bit input/output port<br>Input/output can be specified in bit unit<br>• Other pin functions<br>P10 SIO0 data output<br>P11 SIO0 data input/bus input/output<br>P12 SIO0 clock input/output<br>P13 SIO1 data output<br>P14 SIO1 data input/bus input/output<br>P15 SIO1 clock input/output<br>P16 Buzzer output<br>P17 Timer1 output (PWM output)</td><td>• Output form :<br>CMOS/N-channel open drain<br>(specified in a bit)</td><td>Data line<br>D0 to D7</td></tr>
<tr><td>PORT7<br><br>P70<br><br>P71 - P73<br><br><br><br><br><br><br><br><br><br><br>$\overline{P74}$ - P75</td><td><br><br>I/O<br><br>I<br><br><br><br><br><br><br><br><br><br><br>I</td><td>• 6-bit input port<br>• Other pin functions<br>P70 : INT0 input/HOLD release input/<br>N-channel Tr. output for watchdog timer<br>P71 : INT1 input/HOLD release input<br>P72 : INT2 input/timer 0 event input<br>P73 : INT3 input with noise filter/timer 0 event input<br>• Interrupt received form, vector address
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table>
$\overline{P74}$ : XT1 terminal for crystal oscillation<br>P75 : XT2 terminal for crystal oscillation</td><td>Pull-up resistor :<br>Provided/Not provided<br>(specified in a bit)<br>(P70, P71, P72, P73)<br>* $\overline{P74}$, P75 don't have the pull-up resistor option.</td><td>Power for programming<br><br>PROM control signals<br>$\overline{DASEC}$(*2)<br>$\overline{OE}$(*3)<br>$\overline{CE}$(*4)</td></tr>
<tr><td>Port8<br>P80 – P87</td><td>I</td><td>• 8-bit input port<br>• Other function<br>AD input port (8 port pins)</td><td>-</td><td></td></tr>
<tr><td>PORT9<br>P90 - P93</td><td>I/O</td><td>• 4-bit input/output port<br>• Other function<br>DA output port (4 port pins)<br>AD input port (4 port pins)</td><td>-</td><td></td></tr>
</table>

| Pin name | I/O | Function description | Option | PROM mode |
|---|---|---|---|---|
| PORT A (S0/PA0 – S7/PA7) | I/O | • Segment output terminal for LCD display<br>• Can be used as a general input/output port | - | Address input A0 to A7 |
| PORT B (S8/PB0 – S13/PB5) | I/O | • Segment output terminal for LCD display<br>• Can be used as a general input/output port | - | Address input A8 to A13 |
| PORT C (S16/PC0 – S23/PC7) | I/O | • Segment output terminal for LCD display<br>• Can be used as a general input/output port | - | PROM control signal input<br>•*TA(*5)*<br>Address input<br>•*A14,A15* |
| PORT D (S24/PD0 – S31/PD7) | I/O | • Segment output terminal for LCD display<br>• Can be used as a general input/output port | - | |
| PORT L (COM0/PL0 – COM3/PL3) | I/O | • Common output terminal for LCD display<br>• Can be used as a general input port | - | |
| V1/PL4 – V3/PL6 | I | • Bias power terminal for LCD drive<br>• Can be used as a general input port | - | |
| $\overline{\text{RES}}$ | I | Reset pin | - | |
| XT1/ $\overline{\text{P74}}$ | I | • Input pin for 32.768kHz crystal oscillation<br>In case of non use, connect to VDD.<br>• Other function<br>A general input port $\overline{\text{P74}}$ | - | |
| XT2/P75 | O<br>( I ) | • Output pin for 32.768kHz crystal oscillation<br>In case of non use, should be left unconnected<br>• Other function<br>A general input port P75 | - | |
| CF1 | I | Input pin for ceramic resonator oscillation | - | |
| CF2 | O | Output pin for ceramic resonator oscillation | - | |

* All of port options can be specified in bit unit except the pull-up resistor of port 0.

[Notes] • The VDD1, VDD2 and VDD3 terminals must be shorted electrically each other.
• The VSS1, VSS2 and VSS3 terminals must be shorted electrically each other.

*1 Connect like the following figure to reduce noise into a VDD terminals.




*2 Memory select input for data security
*3 Output enable input
*4 Chip enable input
*5 TA → PROM control signal input

1. Absolute Maximum Ratings at Ta=25°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply voltage | | VDDMAX | VDD1, VDD2 VDD3 | VDD1=VDD2= VDD3 | | -0.3 | | +7.0 | V |
| LCD display voltage | | VLCD | V1/PL6, V2/PL5 V3/PL4 | VDD1=VDD2= VDD3 | | -0.3 | | VDD | |
| Input voltage | | VI | •Ports 71, 72, 73<br>•Ports $\overline{74}$, 75<br>•Port 8, Port L<br>•$\overline{RES}$ | | | -0.3 | | VDD+0.3 | |
| Input/output voltage | | VIO | •Ports 0, 1<br>•Port 9<br>•Ports A, B, C, D | | | -0.3 | | VDD+0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1 | •CMOS output<br>•At each pins | | -4 | | | mA |
| | | IOPH(2) | Ports A, B, C, D | | | -4 | | | |
| | | IOPH(3) | Port 9 | | | -4 | | | |
| | Total output current | ΣIOAH(1) | Ports 0, 1 | Total all pins | | -30 | | | |
| | | ΣIOAH(2) | Ports A, B | Total all pins | | -20 | | | |
| | | ΣIOAH(3) | Ports C, D | Total all pins | | -20 | | | |
| | | ΣIOAH(4) | Port 9 | Total all pins | | -20 | | | |
| Low level output current | Peak output current | IOPL(1) | Ports 0, 1 | At each pins | | | | 20 | |
| | | IOPL(2) | Ports A, B, C, D | At each pins | | | | 20 | |
| | | IOPL(3) | Port 9 | At each pins | | | | 20 | |
| | | IOPL(4) | Port 70 | At each pins | | | | 15 | |
| | Total output current | ΣIOAL(1) | Ports 0, 1 | Total all pins | | | | 40 | |
| | | ΣIOAL(2) | Ports A, B | Total all pins | | | | 24 | |
| | | ΣIOAL(3) | Ports C, D | Total all pins | | | | 24 | |
| | | ΣIOAL(4) | Port 9 | Total all pins | | | | 15 | |
| | | ΣIOAL(5) | Port 70 | Total all pins | | | | 10 | |
| Maximum power dissipation | | Pdmax | QIC80S | Ta=+10 to+40°C | | | | 515 | mW |
| Operating temperature range | | Topr | | | | +10 | | +40 | °C |
| Storage temperature range | | Tstg | | | | -65 | | +150 | |

Notes •The QFP packages should be heat-soaked for 12 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
•After pre-baking a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 24 hours.

2. Recommended Operating Range at Ta=+10°C to +40°C, VSS=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|
| Operating supply voltage range | VDD(1) | VDD1,VDD2,VDD3 | 0.98μs ≤ tCYC ≤ 400μs | | 4.5 | | 6.0 | V |
| | VDD(2) | | 3.9μs ≤ tCYC ≤ 400μs | | 2.5 | | 6.0 | |
| Hold voltage | VHD | VDD1,VDD2,VDD3 | RAMs and the registers hold voltage at HOLD mode. | | 2.0 | | 6.0 | |
| Input high voltage | VIH(1) | Port 0 | Output disable | 4.5-6.0 | 0.4VDD +0.9 | | VDD | |
| | VIH(2) | •Ports 1, 9<br>•Ports A, B, C, D<br>•Ports 72, 73 (Schmitt) | Output disable | 4.5-6.0 | 0.75VDD | | VDD | |
| | VIH(3) | •Port 70<br>Port input/interrupt<br>•Port 71<br>• $\overline{\text{RES}}$ (Schmitt) | Output N-channel Tr. OFF | 4.5-6.0 | 0.75VDD | | VDD | |
| | VIH(4) | Port 70<br>Watchdog timer | Output N-channel Tr. OFF | 4.5-6.0 | 0.9VDD | | VDD | |
| | VIH(5) | •Port 8 | Output N-channel Tr. OFF | 4.5-6.0 | 0.75VDD | | VDD | |
| Input low voltage | VIL(1) | Port 0 | Output disable | 4.5-6.0 | VSS | | 0.2VDD | |
| | VIL(2) | •Ports 1, 9<br>•Ports A, B, C, D<br>•Ports 72, 73 (Schmitt) | Output disable | 4.5-6.0 | VSS | | 0.25VDD | |
| | VIL(3) | •Port 70<br>Port input/interrupt<br>•Port 71<br>• $\overline{\text{RES}}$ (Schmitt) | Output N-channel Tr. OFF | 4.5-6.0 | VSS | | 0.25VDD | |
| | VIL(4) | Port 70<br>Watchdog timer | Output N-channel Tr. OFF | 4.5-6.0 | VSS | | 0.8VDD -1.0 | |
| | VIL(5) | •Port 8 | Output N-channel Tr. OFF | 4.5-6.0 | VSS | | 0.25VDD | |
| Operation cycle time | tCYC | | | 4.5-6.0 | 0.98 | | 400 | μs |
| | | | | 4.5-6.0 | 3.9 | | 400 | |

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|
| Oscillation frequency range (Note 1) | FmCF(1) | CF1, CF2 | •6MHz (ceramic resonator oscillation) •Refer to figure 1 | 4.5-6.0 | 5.88 | 6 | 6.12 | MHz |
| | FmCF(2) | CF1, CF2 | •3MHz (ceramic resonator oscillation) •Refer to figure 1 | 4.5-6.0 | 2.94 | 3 | 3.06 | |
| | FmRC | | RC oscillation | 4.5-6.0 | 0.4 | 0.8 | 3.0 | |
| | FsXtal | XT1, XT2 | •32.768kHz (crystal oscillation) •Refer to figure 2 | 4.5-6.0 | | 32.768 | | kHz |
| Oscillation stabilizing time period (Note 1) | tmsCF(1) | CF1, CF2 | •6MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5-6.0 | | | | ms |
| | tmsCF(2) | CF1, CF2 | •3MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5-6.0 | | | | |
| | tssXtal | XT1, XT2 | •32.768kHz (crystal oscillation) •Refer to figure 3 | 4.5-6.0 | | | | s |

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|
| Input high current | IIH(1) | •Port 1<br>•Port 0 without pull-up MOS Tr. | •Output disable<br>•Pull-up MOS Tr. OFF. VIN=VDD (including the off-leak current of the output Tr.) | 4.5-6.0 | | | 1 | μA |
| | IIH(2) | •Port 7 without pull-up MOS Tr.<br>•Port 8 | VIN=VDD | 4.5-6.0 | | | 1 | |
| | IIH(3) | Port 9 | VIN=VDD | 4.5-6.0 | | | 1 | |
| | IIH(4) | Ports A, B, C, D, L | VIN=VDD | 4.5-6.0 | | | 1 | |
| | IIH(5) | $\overline{RES}$ | VIN=VDD | 4.5-6.0 | | | 1 | |
| | IIH(6) | Ports $\overline{74}$,75 | Using as port VIN=VDD | 4.5-6.0 | | | 1 | |
| Input low current | IIL(1) | •Port 1<br>•Port 0 without pull-up MOS Tr. | •Output disable<br>•Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.) | 4.5-6.0 | -1 | | | |
| | IIL(2) | •Port 7 without pull-up MOS Tr.<br>•Port 8 | VIN=VSS | 4.5-6.0 | -1 | | | |
| | IIL(3) | Port 9 | VIN=VSS | 4.5-6.0 | -1 | | | |
| | IIL(4) | Ports A, B, C, D, L | VIN=VSS | 4.5-6.0 | -1 | | | |
| | IIL(5) | $\overline{RES}$ | VIN=VSS | 4.5-6.0 | -1 | | | |
| | IIL(6) | Ports $\overline{74}$,75 | Using as port VIN=VSS | 4.5-6.0 | -1 | | | |
| Output high voltage | VOH(1) | Ports 0,1 of CMOS output | IOH=-1.0mA | 4.5-6.0 | VDD-1 | | | V |
| | VOH(2) | •Port 9 of CMOS output<br>•Ports A, B, C, D of CMOS output | IOH=-1.0mA | 4.5-6.0 | VDD-1 | | | |
| Output low voltage | VOL(1) | Ports 0, 1 | IOL=10mA | 4.5-6.0 | | | 1.5 | |
| | VOL(2) | | IOL=1.6mA | 4.5-6.0 | | | 0.4 | |
| | VOL(3) | Port 70 | IOL=1mA | 4.5-6.0 | | | 0.4 | |
| | VOL(4) | Port 9 | IOL=6mA | 4.5-6.0 | | | 1.5 | |
| | VOL(5) | | IOL=1.2mA | 4.5-6.0 | | | 0.4 | |
| | VOL(6) | Ports A, B, C, D of CMOS output | IOL=8mA | 4.5-6.0 | | | 1.5 | |
| | VOL(7) | | IOL=1.6mA | 4.5-6.0 | | | 0.4 | |

Continue.

| Parameter | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|
| LCD output regulation | VODLS | S0 to S13, S16 to S31 | •Deference voltage to ideal value •VLCD, 2/3VLCD, 1/3VLCD | 4.5-6.0 | 0 | | ±0.2 | V |
| | VODLC | COM0 to COM3 | •Deference voltage to ideal value •VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD | 4.5-6.0 | 0 | | ±0.2 | |
| LCD ladder resistor | RLCD(1) | | Resistance at a ladder resistor | 4.5-6.0 | | 60 | | kΩ |
| | RLCD(2) | | •Resistance at a ladder resistor •1/2R mode | 4.5-6.0 | | 30 | | |
| Pull-up MOS Tr. resistor | Rpu | •Ports 0, 1 •Ports A, B, C, D •Ports 70, 71, 72, 73 | VOH=0.9VDD | 4.5-6.0 | 15 | 40 | 70 | |
| Hysteresis voltage | VHIS | •Ports 0, 1 •Ports 70, 71, 72, 73 • $\overline{\text{RES}}$ | Output disable | 4.5-6.0 | | 0.1VDD | | V |
| Pin capacitance | CP | All pins | •f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C | 4.5-6.0 | | 10 | | pF |

4. Serial Input / Output Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | | | Symbol | Pins | Conditions | VDD[V] | Ratings min. | Ratings typ. | Ratings max. | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Cycle | tCKCY(1) | SCK0, SCK1 | Refer to figure 5. | 4.5-6.0 | 2 | | | tCYC |
| | | Low Level pulse width | tCKL(1) | | | 4.5-6.0 | 1 | | | |
| | | High Level pulse width | tCKH(1) | | | 4.5-6.0 | 1 | | | |
| | Output clock | Cycle | tCKCY(2) | SCK0, SCK1 | •Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5. | 4.5-6.0 | 2 | | | |
| | | Low Level pulse width | tCKL(2) | | | 4.5-6.0 | | 1/2 tCKCY | | |
| | | High Level pulse width | tCKH(2) | | | 4.5-6.0 | | 1/2 tCKCY | | |
| Serial input | Data set up time | | tICK | •SI0,SI1 •SB0,SB1 | •Data set-up to SCK0, 1 •Data hold from SCK0, 1 •Refer to figure 5. | 4.5-6.0 | 0.1 | | | μs |
| | Data hold time | | tCKI | | | 4.5-6.0 | 0.1 | | | |
| Serial output | Output delay time (Serial clock is external clock) | | tCKO(1) | •SO0, SO1 •SB0, SB1 | •Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1 •Refer to figure 5. | 4.5-6.0 | | | 7/12tCYC +0.2 | |
| | Output delay time (Serial clock is internal clock) | | tCKO(2) | | | 4.5-6.0 | | | 1/3tCYC +0.2 | |

5. Pulse Input Conditions at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | •INT0, INT1<br>•INT2/T0IN | •Interrupt acceptable<br>•Timer0-countable | 4.5-6.0 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3/T0IN<br>(The noise rejection clock is selected to 1/1.) | •Interrupt acceptable<br>•Timer0-countable | 4.5-6.0 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3/T0IN<br>(The noise rejection clock is selected to 1/16.) | •Interrupt acceptable<br>•Timer0-countable | 4.5-6.0 | 32 | | | |
| | tPIH(4)<br>tPIL(4) | INT3/T0IN<br>(The noise rejection clock is selected to 1/64.) | •Interrupt acceptable<br>•Timer0-countable | 4.5-6.0 | 128 | | | |
| | tPIL(5) | $\overline{\text{RES}}$ | Reset acceptable | 4.5-6.0 | 200 | | | μs |

6. AD Converter Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| Resolution | NAD | | | 4.5-6.0 | | 8 | | bit |
| Absolute precision (Note 2) | ETAD | | | 4.5-6.0 | | | ±1.5 | LSB |
| Conversion time | tCAD | | AD conversion time = 16 × tCYC (ADCR2=0) (Note 3) | 4.5-6.0 | 15.68 (tCYC= 0.98μs) | | 65.28 (tCYC= 4.08μs) | μs |
| | | | AD conversion time = 32 × tCYC (ADCR2=1) (Note 3) | | 31.36 (tCYC= 0.98μs) | | 130.56 (tCYC= 4.08μs) | |
| Analog input voltage range | VAIN | AN0 - AN11 | | 4.5-6.0 | VSS | | VDD | V |
| Analog port input current | IAINH | | VAIN=VDD | 4.5-6.0 | | | 1 | μA |
| | IAINL | | VAIN=VSS | 4.5-6.0 | -1 | | | |

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. DA Converter Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| Resolution | NDA | | | 4.5-6.0 | | 8 | | bit |
| Total error | | | 8 bit mode | 4.5-6.0 | | | 1.0 | % |
| | | | 9 bit mode | | | | 0.8 | |
| | | | 9.5 bit mode | | | | 0.7 | |
| Settling time | tSAD | | (Note 4) | 4.5-6.0 | | | 0.5 | μs |
| Analog output voltage range | VAOUT | DA0 to DA3 | 8 bit mode | 4.5-6.0 | VSS | | VDD | V |
| | | | 9 bit mode (1) | | VSS | | 1/2VDD | |
| | | | 9 bit mode (2) | | 1/2VDD | | VDD | |
| | | | 9.5 bit mode | | 1/3VDD | | 2/3VDD | |
| Output resistor | RODA | | (Note 5) | 4.5-6.0 | | 4 | | kΩ |

(Note 4) Settling time means the time from executing the DA conversion instruction to generating the analog voltage output corresponding to the digital data on the specific port.
(Note 5) DA data = 80H

8. Current Dissipation Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| Current dissipation during basic operation (Note 6) | IDDOP(1) | VDD1= VDD2= VDD3 | •FmCF=6MHz Ceramic resonator oscillation<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : CF oscillation<br>•Internal RC oscillation stops<br>•1/1 divided | 4.5-6.0 | | 15 | 30 | mA |
| | IDDOP(2) | | •FmCF=3MHz Ceramic resonator oscillation<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : CF oscillation<br>•Internal RC oscillation stops<br>•1/2 divided | 4.5-6.0 | | 6 | 15 | |
| | IDDOP(3) | | •FmCF=0Hz (when oscillation stops)<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : RC oscillation<br>•1/2 divided | 4.5-6.0 | | 4 | 13 | |
| | IDDOP(4) | | •FmCF=0Hz (when oscillation stops)<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : crystal oscillation<br>•Internal RC oscillation stops<br>•1/2 divided | 4.5-6.0 | | 4 | 9 | |

Continue.

| Parameter | Symbol | Pins | Conditions | Ratings | | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | VDD[V] | min. | typ. | max. | |
| Current dissipation in HALT mode (Note 6) | IDDHALT(1) | VDD1= VDD2= VDD3 | •HALT mode<br>•FmCF=6MHz Ceramic resonator oscillation<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : CF oscillation<br>•Internal RC oscillation stops<br>•1/1 divided | 4.5-6.0 | | 6 | 11 | mA |
| | IDDHALT(2) | | •HALT mode<br>•FmCF=3MHz Ceramic resonator oscillation<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : CF oscillation<br>•Internal RC oscillation stops<br>•1/2 divided | 4.5-6.0 | | 2.2 | 9 | |
| | IDDHALT(3) | | •HALT mode FmCF=0Hz (when oscillation stops)<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : RC oscillation<br>•1/2 divided | 4.5-6.0 | | 500 | 1700 | μA |
| | IDDHALT(4) | | •HALT mode FmCF=0Hz (when oscillation stops)<br>•FsXtal=32.768kHz crystal oscillation<br>•System clock : crystal oscillation<br>•Internal RC oscillation stops<br>•1/2 divided | 4.5-6.0 | | 25 | 100 | |
| | IDDHALT(5) | | | | | | | |
| Current dissipation in HOLD mode (Note 6) | IDDHOLD(1) | VDD1= VDD2= VDD3 | HOLD mode | 4.5-6.0 | | 0.05 | 30 | |

(Note 6) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

| Oscillation type | Maker | Oscillator | C1 | C2 |
|---|---|---|---|---|
| 6MHz ceramic resonator oscillation | Murata | CSA6.00MG | 33pF | 33pF |
| | | CST6.00MGW | on chip | |
| | Kyocera | KBR-6.0MSA | 33pF | 33pF |
| | | PBRC6.00A(chip type) | 33pF | 33pF |
| | | KBR-6.0MKS | on chip | |
| | | PBRC6.00B(chip type) | | |
| 3MHz ceramic resonator oscillation | Murata | CSA3.00MG | 33pF | 33pF |
| | | CST3.00MGW | on chip | |
| | Kyocera | KBR-3.0MS | 47pF | 47pF |

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

| Oscillation type | Maker | Oscillator | C3 | C4 |
|---|---|---|---|---|
| 32.768kHz crystal oscillation | | | | |
| | | | | |

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

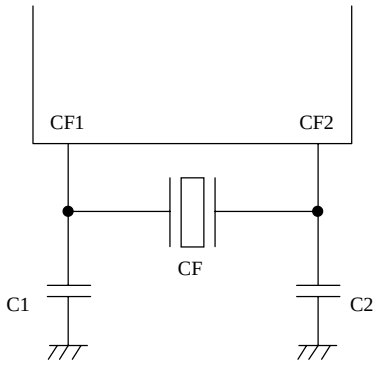



Figure 1 Ceramic oscillation circuit

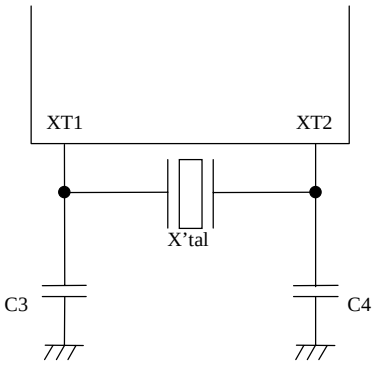
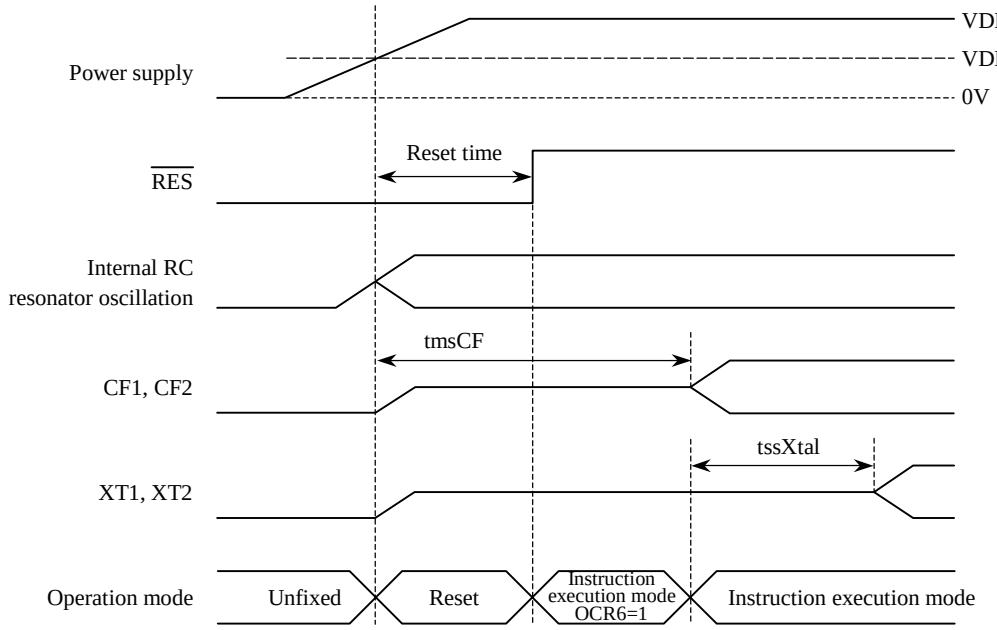
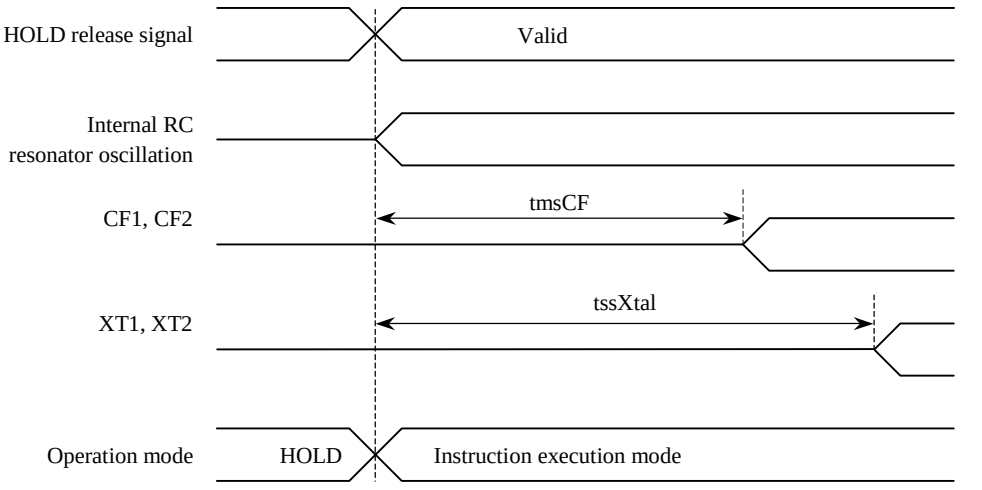



Figure 2 Crystal oscillation circuit

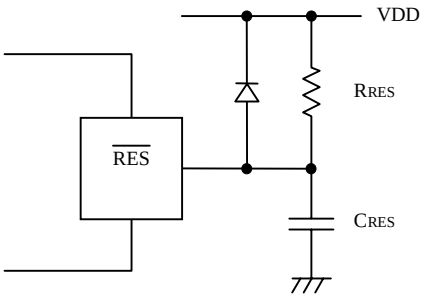



<Reset time and oscillation stable time>




<HOLD release signal and oscillation stable time>

Figure 3 Oscillation stable time




(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

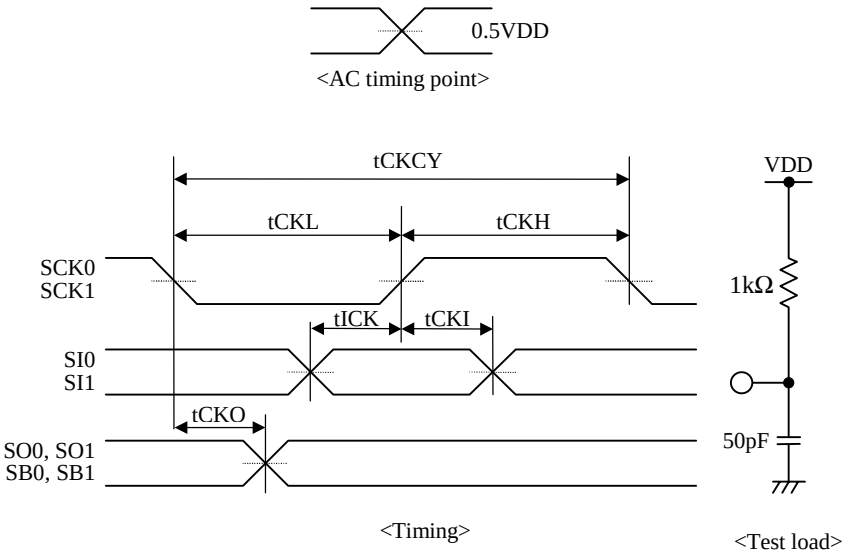



Figure 5 Serial input / output test condition

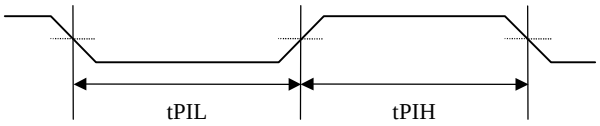



Figure 6 Pulse input timing condition