mosaic

Mosaic Semiconductor inc.

256K X 8 SRAM

MS8256SC-10/12/15

Issue 2.0 : September 1990

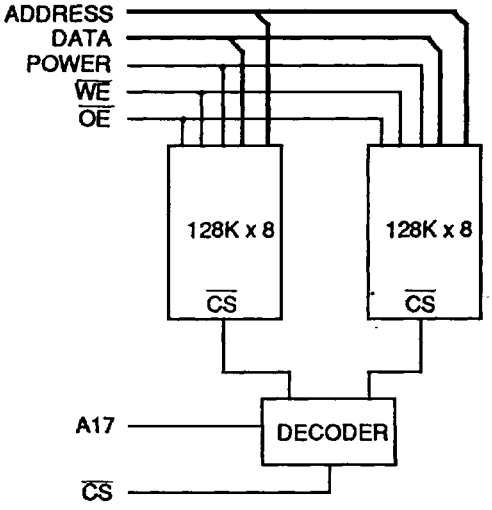
PRELIMINARY

262,144 x 8 CMOS High Speed Static RAM

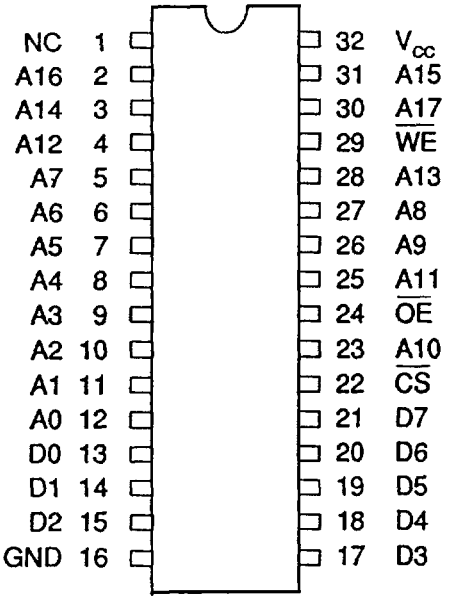
Features

Access Times of 100/120/150 ns
JEDEC Standard 32 pin DIL footprint
Operating Power 130 mW (typ.)
Low Power Standby 60 mW (typ.)
60 µW (typ.) - L
Operating Temp Range -55°C to +125°C
Equal Access and Cycle Times
Battery back-up capability
Completely Static Operation
Onboard Decoupling Capacitors

Block Diagram



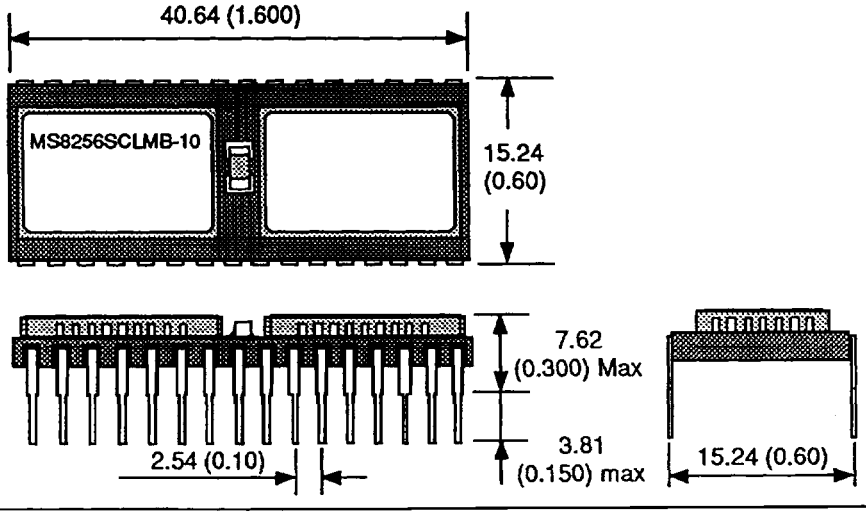
Pin Definition



Pin Functions

A0-A17	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



MOSCS064

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) V_t can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I)
	T_{AM}	-55	-	125	°C (M,MB)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI1}	$0V \le V_{IN} \le V_{CC}$	-	-	8	µA
(A17, A18, $\overline{CS}$)	I_{LI2}	$0.5V \le V_{IN} \le 2.7V$	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	-	-	8	µA
Operating Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA, I/P's static	-	26	43	mA
Average Current	I_{CC1}	Min. Cycle, $\overline{CS}=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH}, $I_{I/O}$=0 mA	-	55	82	mA
	I_{CC1}	Cycle =1µs, $\overline{CS} \ge V_{CC}$-0.2V, $0.2V \ge V_{IN} \ge V_{CC}$-0.2V	-	19	37	mA
Standby Current	I_{SB}	$\overline{CS}=V_{IH}$, $V_{IN}=V_{IL}$ or V_{IH}	-	12	16	mA
	I_{SB1}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2V \ge V_{IN} \ge V_{CC}$-0.2V	-	0.05	4	mA
-L Part	I_{SB2}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2V \ge V_{IN} \ge V_{CC}$-0.2V	-	12	960	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance ($\overline{CS}$, A17)	C_{IN1}	V_{IN} = 0V	6	pF
I/P Capacitance (other)	C_{IN2}	V_{IN} = 0V	16	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	20	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

* Input pulse levels: 0.8V to 2.4V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

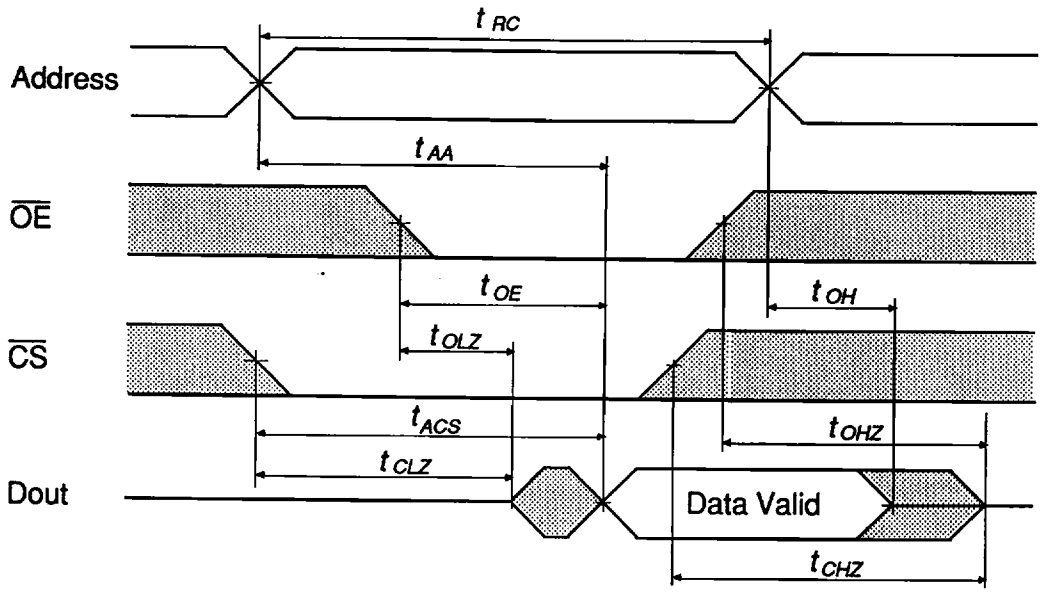
Read Cycle (1,2)

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	100	-	120	-	150	ns
Chip Select Access Time	t_{ACS}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	60	-	70	-	85	ns
Output Hold from Address Change	t_{OH}	15	-	15	-	15	-	ns
Chip Selection to Output in Low Z(2)	t_{CLZ}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z(2)	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z(2)	t_{CHZ}	0	35	0	45	0	55	ns
Output Disable to Output in High Z(2)	t_{OHZ}	0	35	0	45	0	55	ns

Notes: 1. $\overline{WE}$ is High for Read Cycle.

2. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

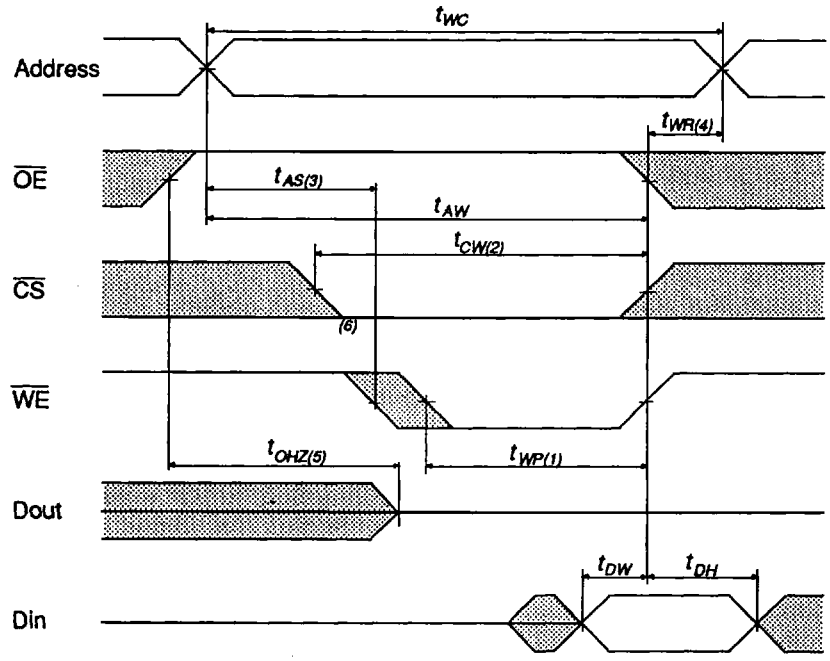
Read Cycle Timing Waveform (1,2)



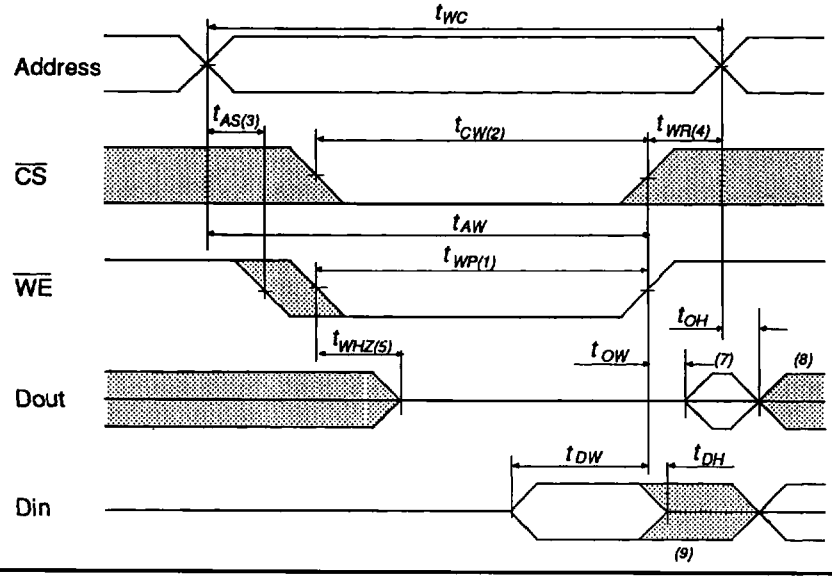
Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	90	-	100	-	110	-	ns
Address Valid to End of Write	t_{AW}	90	-	100	-	110	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	75	-	85	-	95	-	ns
Write Recovery Time	t_{WR}	5	-	10	-	15	-	ns
Write to Output in High Z(10)	t_{WHZ}	0	40	0	45	0	30	ns
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output active from end of Write(10)	t_{OW}	10	-	10	-	10	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



AC Characteristics Notes

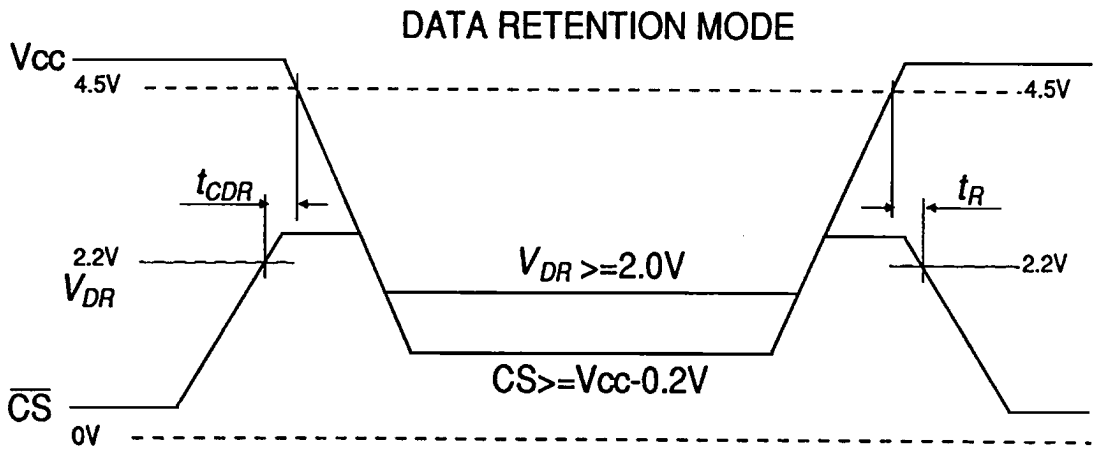
(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{CW} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) T_{AS} is measured from the address valid to the beginning of write.
(4) T_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write.
(5) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(6) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low , outputs remain in a high impedance state.
(7) D_{OUT} is in the same phase as written data of this write cycle.
(8) D_{OUT} is the read data of next address.
(9) If $\overline{CS}$ is low during this period, I/O pins are in the output state, and inputs out of phase must not be applied to I/O pins.
(10) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*[1]	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$	2.0	-	-	V
Data Retention Current		$V_{CC}=3.0V$, $\overline{CS} \geq V_{CC}-0.2V$				
	I_{CCDR1}	$T_{OP}=T_A$	-	10	180	µA
	I_{CCDR2}	$T_{OP}=T_{AI}$	-	-		µA
	I_{CCDR3}	$T_{OP}=T_{AM}$	-	-	760	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes : (1) Typical figures measured at 25°C

Data Retention Waveform



Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at Ta = +25°C (optional)	100%
Burn-In	Method 1015, Codition D, Ta = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at Ta=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	

Ordering Information

MS8256SCLMB-10

Speed	10	= 100 ns
	12	= 120 ns
	15	= 150 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp
	MB	= May be screened in accordance with MIL-STD-883C.
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Package	SC	= Ceramic 32 pin DIL
Organization	8256	= 256K x 8, JEDEC Pinout

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