Signetics

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Status	Product Specification
FAST Products	

FAST 74F365, 74F366 74F367, 74F368 Buffers/Drivers

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer/Driver (3-State)

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **High speed**
- **Bus oriented**
- **3-state buffer outputs sink 64mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365, 74F367	5.0ns	36mA
74F366, 74F368	5.0ns	33mA

ORDERING INFORMATION

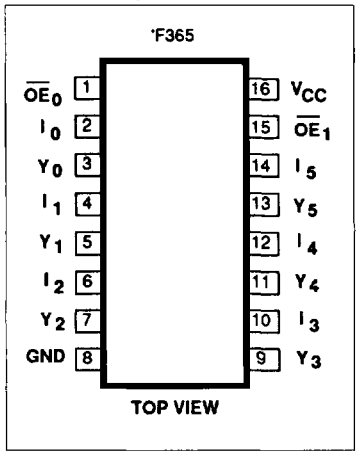
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F365N, N74F366N, N74F367N, N74F368N
16-Pin Plastic SO	N74F365D, N74F366D, N74F367D, N74F368D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

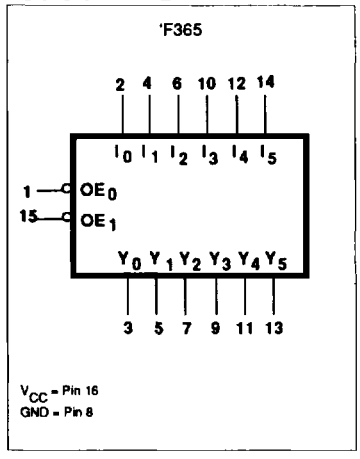
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_5	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$,$\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0-Y_5, $\overline{Y}_0$-$\overline{Y}_5$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

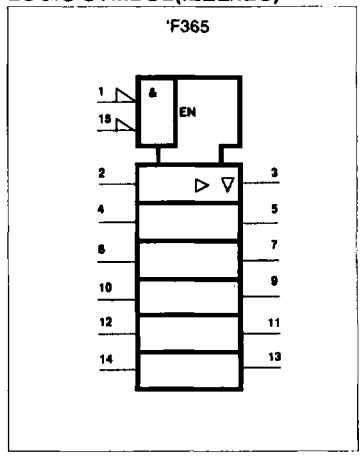
PIN CONFIGURATION



LOGIC SYMBOL



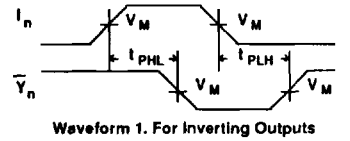
LOGIC SYMBOL(IEEE/IEC)



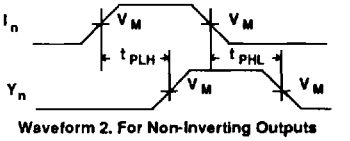
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F366, 'F368	Waveform 1	3.0 2.0	5.0 3.0	6.5 5.0	3.0 1.5	7.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F365, 'F367	Waveform 2	2.5 2.5	4.5 5.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F365, 'F366	Waveform 3 Waveform 4	2.5 2.5	4.0 5.0	6.5 8.0	2.5 2.5	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F367, 'F368	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	6.5 6.5	2.0 2.0	7.0 7.0	ns

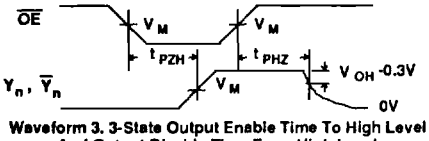
AC WAVEFORMS



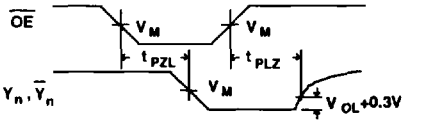
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



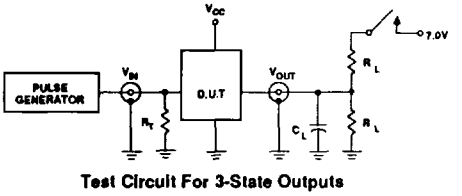
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

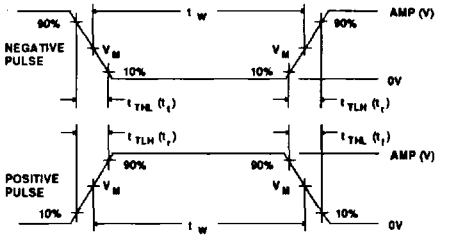
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns