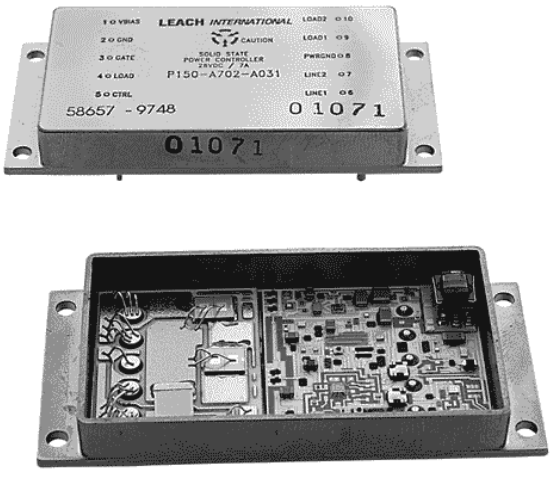
ENGINEERING DATA SHEET

P150 SERIES

SOLID STATE POWER CONTROLLER
28 VDC, 1PNO-WITH CURRENT OR VOLTAGE STATUS OUTPUT
UP TO 30 AMP RATING



SIZE: 69.6 x 34 x 9.65 mm

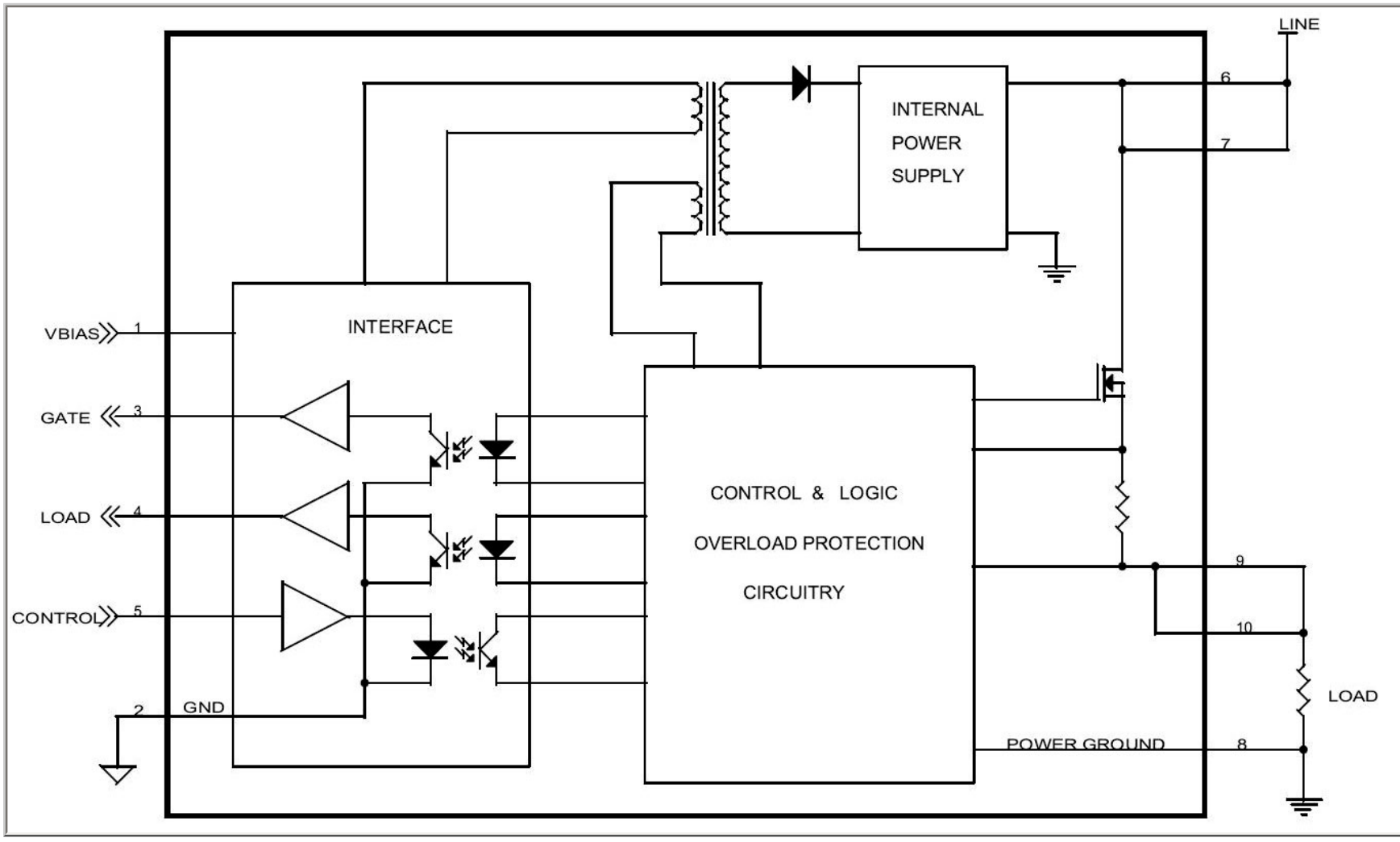
DESCRIPTION

The P150 Series of Solid State Power Controllers (SSPC) is rated from 2 to 30 Amperes. These LEACH SSPC's feature reliable, trouble free switching together with real short circuit protection. Employing a power FET output stage, and built using thick film technology, they offer low on state resistance and low on state voltage drop. They react to fault condition and can shutdown within microseconds, if required. Two status signals, derived from the load current value or voltage and from the device gate, are reported via optical isolators. Designed to operate in 28 VDC systems, these devices do not require derating for any load type. They are hermetically sealed, in a metal package.

FEATURES

- Fast acting
- Built-in overload and short circuit protection
- Load current or voltage status
- FET Gate status or trip status
- Very low voltage drop
- No derating up to 105° C
- Trip free
- Fully isolated bias, control and status
- No derating for non-resistive loads
- Exceeds MIL-P-81653C requirements
- Very low voltage drop output stage

BLOCK DIAGRAM



Esterline Power Systems

Featuring LEACH© power and control solutions
www.leachintl.com

AMERICAS
6900 Orangethorpe Ave.
P.O. Box 5032
Buena Park, CA 90622 USA
Tel: (01) 714-736-7599
Fax: (01) 714-670-1145

EUROPE
2 Rue Goethe
57430 Sarralbe
France
Tel: (33) 3 87 97 31 01
Fax: (33) 3 87 97 96 86

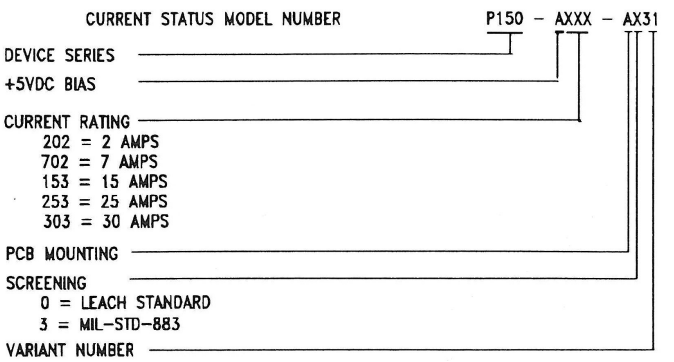
ASIA
Room 501, 5/F, The Centre Mark
287 - 299 Queen's Road Central
Hong Kong
Tel: (852) 2 191 3830
Fax: (852) 2 389 5803

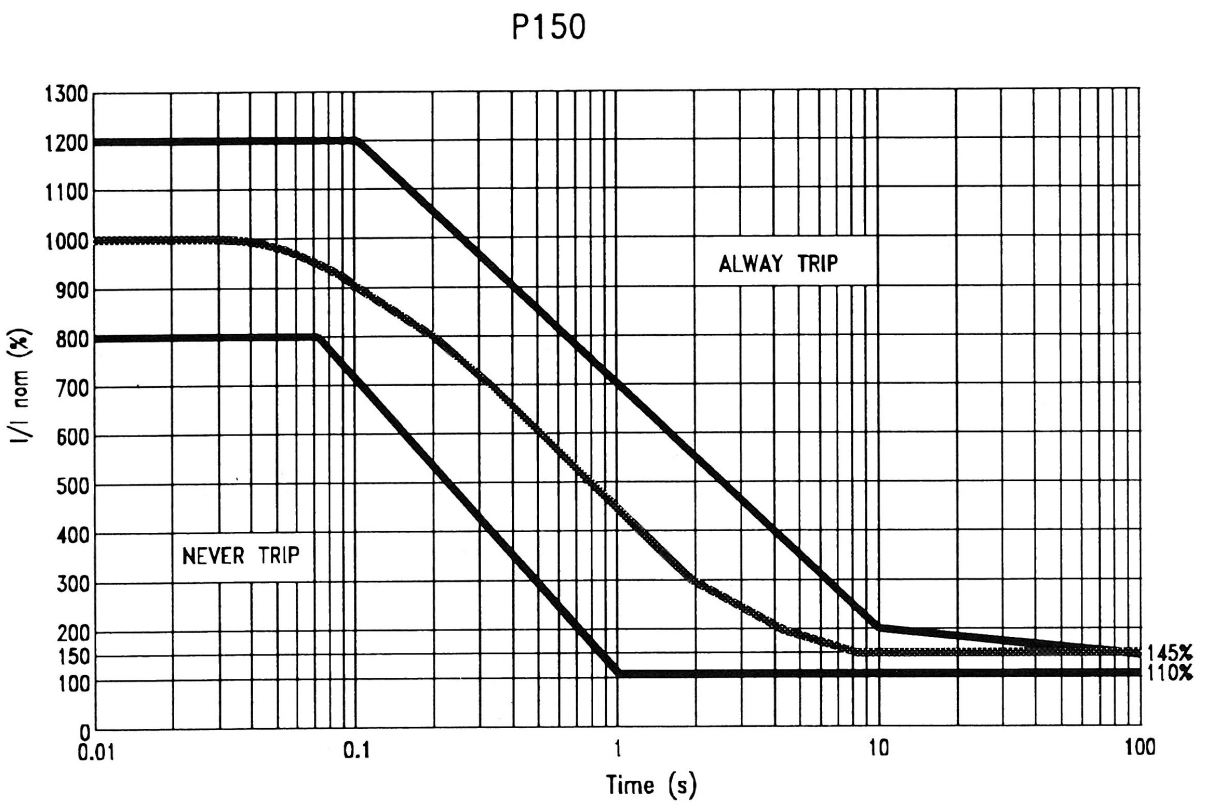
Typical values are at 25 ± 5° C **INPUT**	**DEVICE WITH CURRENT STATUS**					
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
BIAS On Voltage	V_{IHB}	4.5		5.5	V	1,2
BIAS On current	I_{IHB}			10	mA	3
BIAS Off current	I_{ILB}			1	mA	3
CONTROL voltage on	V_{IHC}	2.4			V	
CONTROL voltage off	V_{ILC}	-0.8		0.8	V	
CONTROL current on	I_{IHC}			50	µA	4
CONTROL current off	I_{ILC}			-10	µA	5
Transients (BIAS input)	V_{TB}			+50	V	6

Notes:
1. BIAS voltage must be a step function.
2. No reverse polarity protection.
3. BIAS voltage is 5.0 V.
4. Control voltage at 2.4 vdc.
5. Control voltage at 0.4 vdc.
6. Max. Duration 50 ms, Duty Cycle 1%, Repetition Rate 1 Hz.

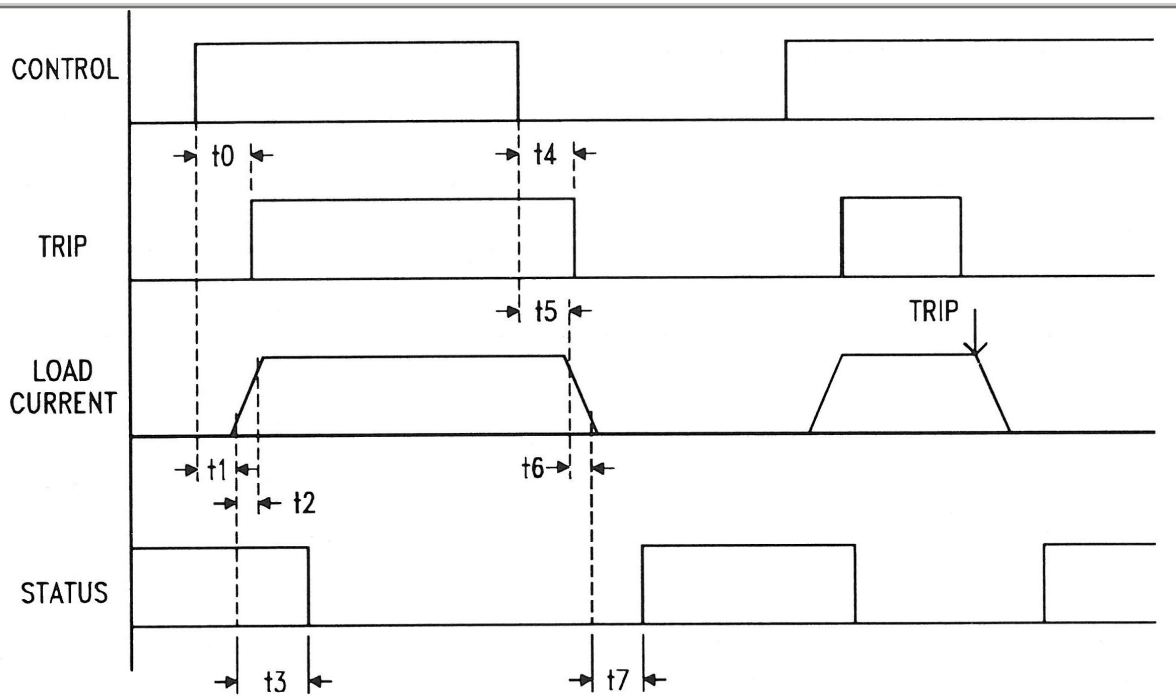
OUTPUT						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Load current	I_L	0		100	%I rated	1
On state voltage drop	V_{LD}			200	mV	2
Off state line voltage	V_L			32	V	3
Gate high voltage	V_{OHS}	2.4			V	
Gate high current	I_{OHS}			50	µA	
Gate low voltage	V_{OLS}			0.8	V	
Gate low current	I_{OLS}			0.2	mA	
Load pick up	I_{SON}			15	%I rated	
Load drop out	I_{SOFF}	5			%I rated	
Leakage current	I_{LL}			1	mA	4
Transient voltage	V_T			+50	V	5
Spikes	V_S	-600		+600	V	6
Trip current	I_{TR}	110	130	145	%I rated	7
Isolation voltage	V_{ISO}			750	VRMS	
Insulation resistance	R_{INS}	100		1000	MΩ	8

Notes:
1. Load current is subject to thermal derating.
2. At load current I_L=100% rated value.
3. Reverse polarity is not blocked and may damage the SSPC.
4. At V_L=28V, Case temperature = 105° C.
5. Duration 12.5 ms max. per MII-STD-704D.
6. Duration 10 µs max. per Mil-STD-704D.
7. See Trip Characteristics.
8. 500 Vdc, ± 10%





TIMING DIAGRAM (CURRENT STATUS)



TIMING

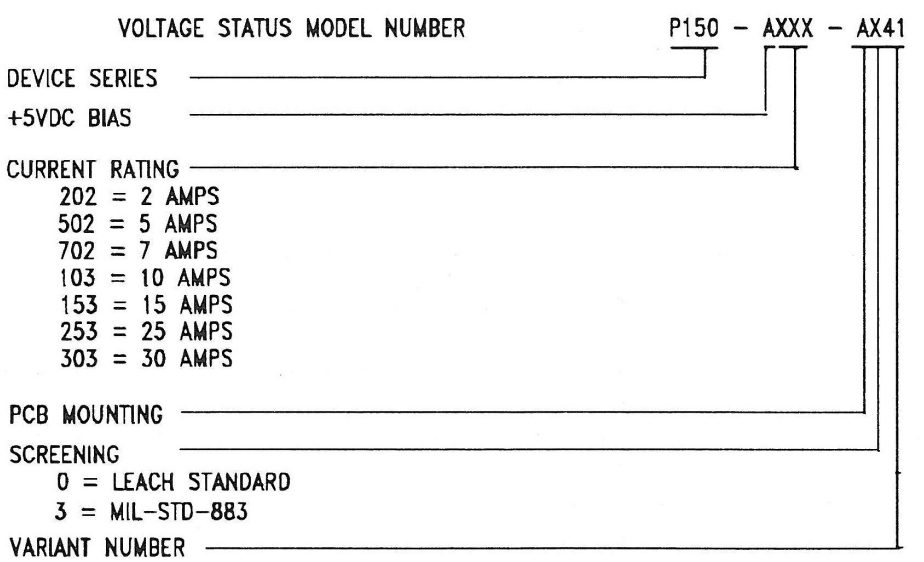
Parameter	Symbol	Typ.	Max.	Unit	Note
CONTROL to GATE delay	t_0	300	1000	µs	
Turn on delay	t_1	150	200	µs	
Load current rise time	t_2	30	1000	µs	
Turn on to LOAD delay	t_3	75	1000	µs	
CONTROL to GATE	t_4	150	1000	µs	
Turn off delay	t_5	150	200	µs	
Load current fall time	t_6	20	1000	µs	2
Turn off to LOAD delay	t_7	400	1000	µs	

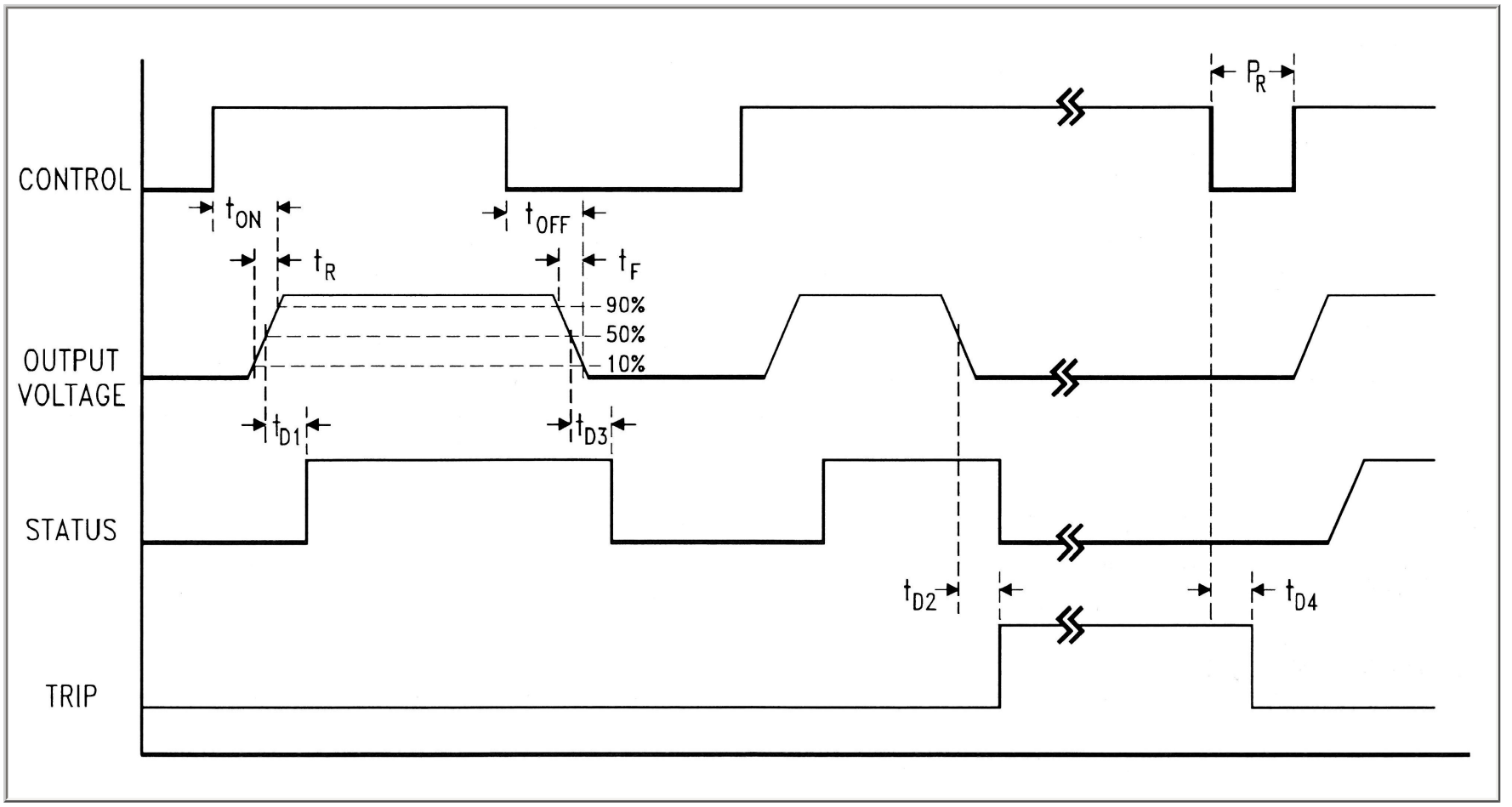
Notes:
1. All timing measurements taken at 10% and 90% points into resistive rated load.
2. Current fall time from trip dependant on overload condition.

Typical values are at 25 ± 5° C INPUT	DEVICE WITH VOLTAGE STATUS		LIMITS		UNIT	NOTES
Parameter	Symbol	CONDITIONS -55°C to +105°C (1)	MIN	MAX		
Logic supply voltage	V_{CC}		4.5	5.5	Vdc	
CONTROL voltage high	V_{IH}		2.0		Vdc	
CONTROL voltage low	V_{IL}			0.8	Vdc	
Transient		Pulse width = 12.5 msec max. per MIL-STD-704D		+50	Vdc	2
Spikes		Pulse width = 10 µsec max. per MIL-STD-704D	-600	+600	Vdc	2
REQUIREMENTS						
28 Vdc initialization spike voltage		During of output spike at 50% amplitude shall be 100µsec maximum		5	V_{PR}	
5 Vdc initialization control		Vline = 28 Vdc, Vcontrol = 0 Vdc, Vbias = 0 to 5 Vdc, rated at <1 msec				3
Logic supply current	I_{CC}	V_{CC}=5.5 Vdc		50	mA	4
Load current continuous	I_{LOAD}			100	%I	
"ON" state voltage drop	V_O			200	mV	5
Leakage current	I_L			1	mA	
STATUS & TRIP voltage high	V_{OH}	IOH=5mA	2.4		Vdc	
STATUS & TRIP voltage low	V_{OL}	IOL=1mA		0.4	Vdc	
CONTROL current high	I_{IH}	VI=2.4 Vdc		50	µA	
CONTROL current low	I_{IL}	VI=0.4 Vdc		10	µA	
Output "ON" sense voltage	V_{ON}	See Timing Diagram (Voltage Status)	30	70	%	5,6,7

Notes:

1. Unless specified otherwise, test conditions shall be at Vcc=5.0 ±0.25Vdc and Vline=28±0.5Vdc. The design shall be capable of meeting all requirements with Vcc=4.5 to 5.5Vdc.
2. The transient and spike requirements apply only to the 28Vdc power lines.
3. The device output shall remain off when 5V bias is raised from 0 to 5Vdc.
4. Without any load connected to the STATUS or TRIP outputs.
5. At 100% rated current.
6. Rated resistive load; measurements taken between 10% and 90% points.
7. Percent of actual applied Vline.





TIMING

Parameter	Symbol	Conditions -55°C to +105°c	Min.	Max.	Unit	Notes
Turn-on time	t_{on}	See Timing Diagram		1000	µsec	1,3
Turn-off time	t_{off}			1000	µsec	1,3
Load voltage rise time	t_R		20	200	µsec	1,3
Load voltage fall time	t_F			200	µsec	1,3
STATUS on delay	t_{D1}			2000	µsec	1
STATUS of delay	t_{D3}			2000	µsec	1
TRIP on delay	t_{D2}			150	µsec	2
TRIP of delay	t_{D4}			150	µsec	2
CONTROL pulse width for device reset	P_R		50		msec	

Notes:
1. At 100% rated current.
2. At 250% rated current.
3. Rated resistive load; measurements taken between 10% and 90% points.

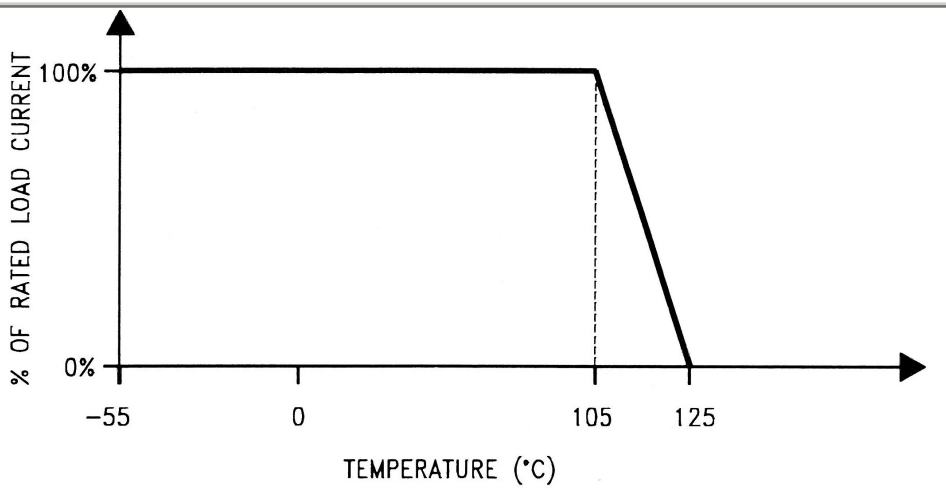
ENVIRONMENTAL DATA

P150 SERIES

Parameter	Symbol	Min.	Max.	Unit	Notes
Operational Temp. Range	T_{op}	-55	125	° C	1,2
Storage Temp. Range	T_{st}	-55	125	° C	
Thermal resistance junction to case	θ_{jc}		15	° C/W	
Max. Junction Temperature of Output Stage	$T_{j(max)}$		150	° C	
Vibration			20	G	3
Acceleration			3000	G	4
Shock			1500	G	5
Seal (Hermetic)					7
Altitude			80000	ft	
MTBF			1.1	hours	6

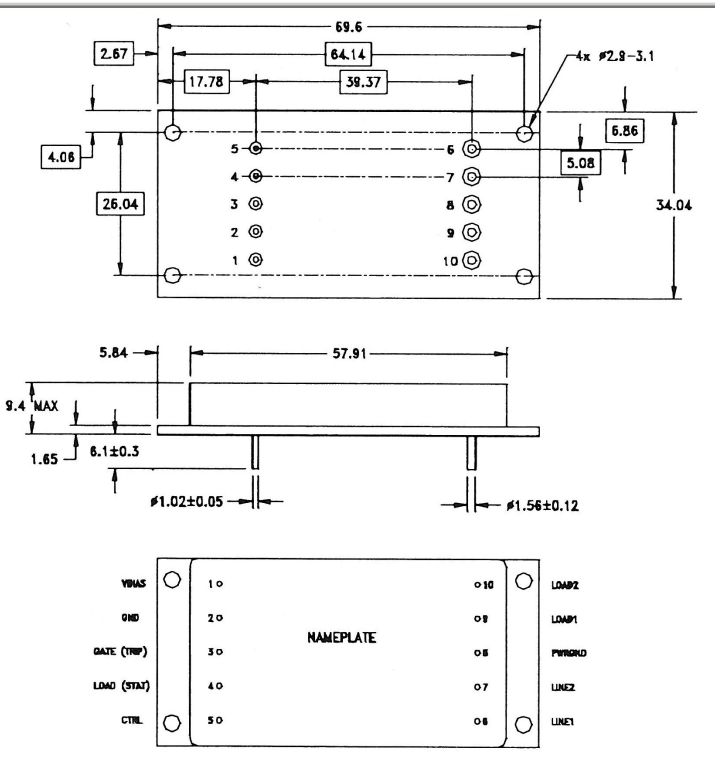
Notes:
1. Case temperature.
2. See thermal derating curve.
3. MIL-P-883C, Method 2007, test condition A; 20-2000 Hz.
4. MIL-P-883C, Method 2001, test condition A.
5. MIL-P-883C, Method 2002, test condition B, 0.5 ms.
6. Per MIL-HBK-217E, Quality level B-1, AUT environment at 25°C.
7. Meets the leakage levels in accordance with MIL-STD-883, Method 1014, test condition A1.

THERMAL DERATING



PHYSICAL DATA (in mm)

- Case Finish: Tin Plated.
- Terminals: Gold Plated.
- Mass: 65 grams max.



This engineering data sheet is designed for initial selection and comparison of products. While every effort is made to ensure the accuracy of all data, each part number, and its application, must be controlled by a Product Control Drawing (PCD). Please contact PowerCom, a Leach International Company, for further information.