NEC

MOS INTEGRATED CIRCUIT
μPD16422

120-OUTPUT TFT-LCD GATE DRIVER

The μPD16422 is a 120-output TFT-LCD gate driver. Since it is provided with a level shift circuit to input logic, it can output +20 V and −5 V in response to input of 5 V CMOS level. The output enable function (OE) allows two drivers to be installed at both sides of an LCD.

FEATURES

- High voltage output (V_{DD} - V_{EE} amplitude, 28 V max.)
- 5 V CMOS level interface
- Output enable function
- High output-pin count (120)
- High-density mounting possible (TCP)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD16422N-×××	TCP (TAB package)	Standard

The shape of TCP can be customized. Consult NEC for details.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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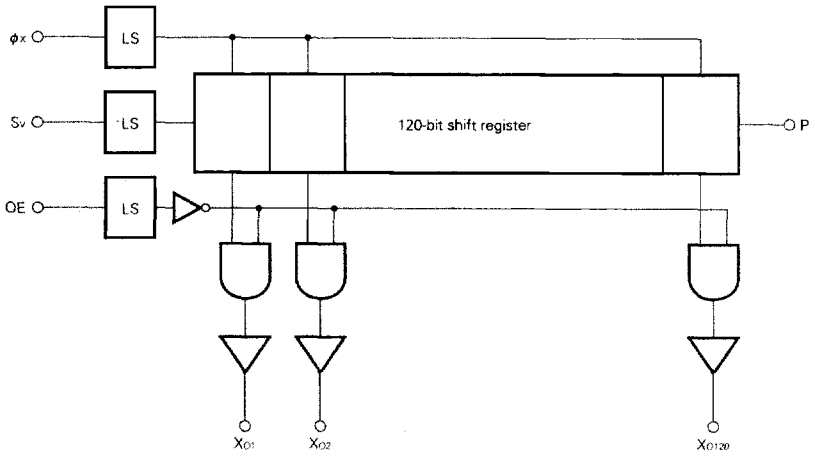
BLOCK DIAGRAM



LS: 5 V CMOS level → V_{EE} – V_{DD}

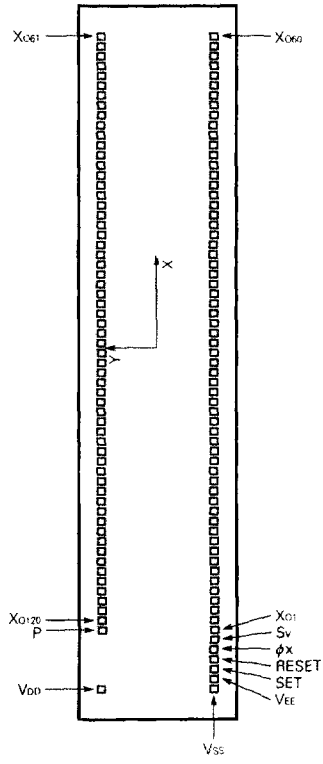
PIN FUNCTION

PAD No.	Symbol	Pin Name	Function Description
5 to 124	X_{O1} to X_{O120}	Driver output	Scan signal output pins that drive the vertical direction of the TFT- LCD (gate line). Signals output from these pins change in synchronization with rising edge of the shift clock φx. Output amplitude of the driver is V_{DD} – V_{EE}.
4	Sv	Vertical start pulse input	Input pin of the internal shift register. Input data is read at the rising edge of the shift clock φx, and is output from X_{O1}. Input level is 5 V CMOS level or V_{EE} – V_{DD}.
125	P	Next stage start pulse output	Start pulse output to next stage when two or more μPD16422s are connected in cascade. Pulse is output at the falling edge of 120th clock of shift clock φx, and is cleared at the falling edge of 121st clock.
3	φx	Shift clock input	Shift clock input to the internal shift register. Shift operation is performed at the rising edge of this clock.
2	OE	Output enable input	Driver output is fixed to L level when this pin is H. However, the shift register is not cleared. Internal logic operates even when OE = H.
1	DUMMY	Dummy pin	Fix this pin to V_{EE}.
126	V_{DD}	Driver positive power	10 to 20 V typ.
127	V_{SS}	Ground	Connect this pin to system ground.
128	V_{EE}	Driver negative power	–15 to –5 V typ.

When two drivers are installed at the both sides of an LCD, OE should be used to enable alternately one of the two drivers. Note, however, that a symmetric mirror TCP (available separately) is necessary for this purpose. Apply power in the order of V_{EE}, V_{DD}, and logic input. Turn off power in the reverse order.

PAD LOCATION

Chip size: 10.31 × 1.84 mm²



Pad size: 120 μm□
(in Al opening section. 120 × 116 μm for V_{DD} pad)

PAD COORDINATES (UNIT: μm) (1/2)

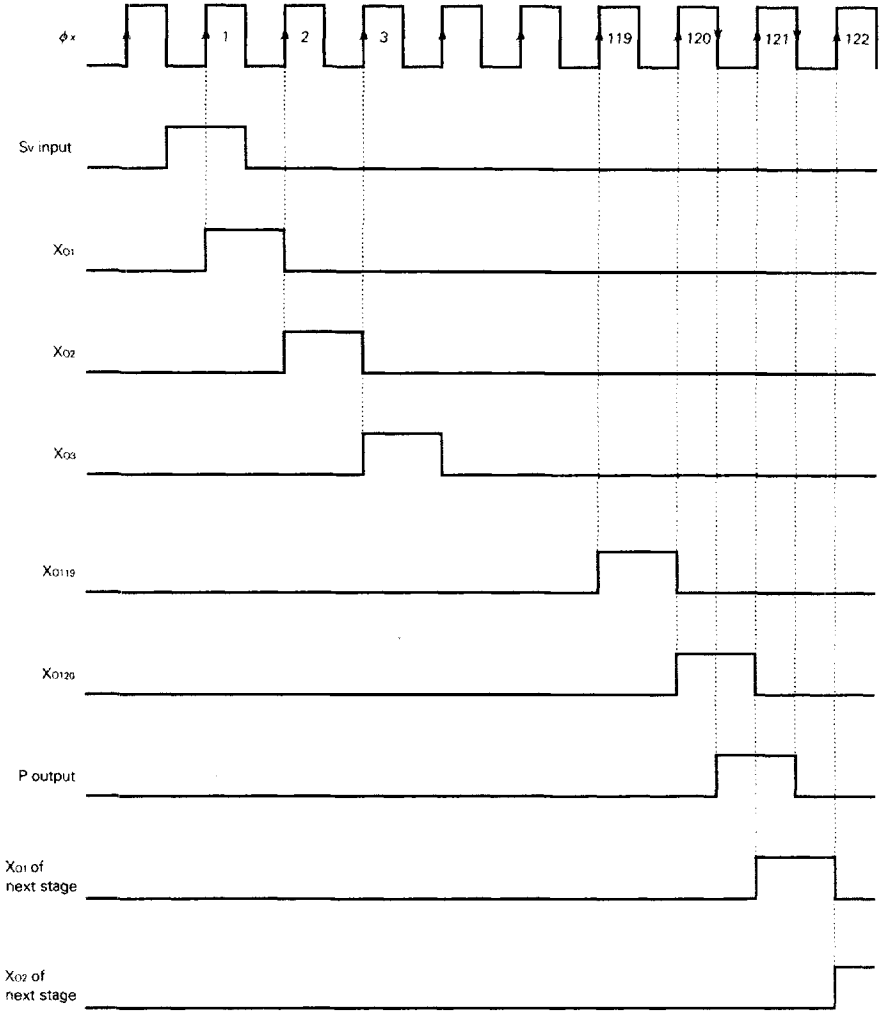
PAD No.	Symbol	X coordinate	Y coordinate	PAD No.	Symbol	X coordinate	Y coordinate
1	DUMMY	-4705.00	-681.50	46	X_{O42}	+2045.00	-681.50
2	OE	-4555.00	-681.50	47	X_{O43}	+2195.00	-681.50
3	ϕ_X	-4405.00	-681.50	48	X_{O44}	+2345.00	-681.50
4	S_V	-4255.00	-681.50	49	X_{O45}	+2495.00	-681.50
5	X_{O1}	-4105.00	-681.50	50	X_{O46}	+2645.00	-681.50
6	X_{O2}	-3955.00	-681.50	51	X_{O47}	+2795.00	-681.50
7	X_{O3}	-3805.00	-681.50	52	X_{O48}	+2945.00	-681.50
8	X_{O4}	-3655.00	-681.50	53	X_{O49}	+3095.00	-681.50
9	X_{O5}	-3505.00	-681.50	54	X_{O50}	+3245.00	-681.50
10	X_{O6}	-3355.00	-681.50	55	X_{O51}	+3395.00	-681.50
11	X_{O7}	-3205.00	-681.50	56	X_{O52}	+3545.00	-681.50
12	X_{O8}	-3055.00	-681.50	57	X_{O53}	+3695.00	-681.50
13	X_{O9}	-2905.00	-681.50	58	X_{O54}	+3845.00	-681.50
14	X_{O10}	-2755.00	-681.50	59	X_{O55}	+3995.00	-681.50
15	X_{O11}	-2605.00	-681.50	60	X_{O56}	+4145.00	-681.50
16	X_{O12}	-2455.00	-681.50	61	X_{O57}	+4295.00	-681.50
17	X_{O13}	-2305.00	-681.50	62	X_{O58}	+4445.00	-681.50
18	X_{O14}	-2155.00	-681.50	63	X_{O59}	+4595.00	-681.50
19	X_{O15}	-2005.00	-681.50	64	X_{O60}	+4745.00	-681.50
20	X_{O16}	-1855.00	-681.50	65	X_{O61}	+4765.00	+681.50
21	X_{O17}	-1705.00	-681.50	66	X_{O62}	+4615.00	+681.50
22	X_{O18}	-1555.00	-681.50	67	X_{O63}	+4465.00	+681.50
23	X_{O19}	-1405.00	-681.50	68	X_{O64}	+4315.00	+681.50
24	X_{O20}	-1255.00	-681.50	69	X_{O65}	+4165.00	+681.50
25	X_{O21}	-1105.00	-681.50	70	X_{O66}	+4015.00	+681.50
26	X_{O22}	-955.00	-681.50	71	X_{O67}	+3865.00	+681.50
27	X_{O23}	-805.00	-681.50	72	X_{O68}	+3715.00	+681.50
28	X_{O24}	-655.00	-681.50	73	X_{O69}	+3565.00	+681.50
29	X_{O25}	-505.00	-681.50	74	X_{O70}	+3415.00	+681.50
30	X_{O26}	-355.00	-681.50	75	X_{O71}	+3265.00	+681.50
31	X_{O27}	-205.00	-681.50	76	X_{O72}	+3115.00	+681.50
32	X_{O28}	-55.00	-681.50	77	X_{O73}	+2965.00	+681.50
33	X_{O29}	+95.00	-681.50	78	X_{O74}	+2815.00	+681.50
34	X_{O30}	+245.00	-681.50	79	X_{O75}	+2665.00	+681.50
35	X_{O31}	+395.00	-681.50	80	X_{O76}	+2515.00	+681.50
36	X_{O32}	+545.00	-681.50	81	X_{O77}	+2365.00	+681.50
37	X_{O33}	+695.00	-681.50	82	X_{O78}	+2215.00	+681.50
38	X_{O34}	+845.00	-681.50	83	X_{O79}	+2065.00	+681.50
39	X_{O35}	+995.00	-681.50	84	X_{O80}	+1915.00	+681.50
40	X_{O36}	+1145.00	-681.50	85	X_{O81}	+1765.00	+681.50
41	X_{O37}	+1295.00	-681.50	86	X_{O82}	+1615.00	+681.50
42	X_{O38}	+1445.00	-681.50	87	X_{O83}	+1465.00	+681.50
43	X_{O39}	+1595.00	-681.50	88	X_{O84}	+1315.00	+681.50
44	X_{O40}	+1745.00	-681.50	89	X_{O85}	+1165.00	+681.50
45	X_{O41}	+1895.00	-681.50	90	X_{O86}	+1015.00	+681.50

PAD COORDINATES (UNIT: μm) (2/2)

PAD No.	Symbol	X coordinate	Y coordinate
91	X_{O87}	+865.00	+681.50
92	X_{O88}	+715.00	+681.50
93	X_{O89}	+565.00	+681.50
94	X_{O90}	+415.00	+681.50
95	X_{O91}	+265.00	+681.50
96	X_{O92}	+115.00	+681.50
97	X_{O93}	-35.00	+681.50
98	X_{O94}	-185.00	+681.50
99	X_{O95}	-335.00	+681.50
100	X_{O96}	-485.00	+681.50
101	X_{O97}	-635.00	+681.50
102	X_{O98}	-785.00	+681.50
103	X_{O99}	-935.00	+681.50
104	X_{O100}	-1085.00	+681.50
105	X_{O101}	-1235.00	+681.50
106	X_{O102}	-1385.00	+681.50
107	X_{O103}	-1535.00	+681.50
108	X_{O104}	-1685.00	+681.50
109	X_{O105}	-1835.00	+681.50
110	X_{O106}	-1985.00	+681.50
111	X_{O107}	-2135.00	+681.50
112	X_{O108}	-2285.00	+681.50
113	X_{O109}	-2435.00	+681.50
114	X_{O110}	-2585.00	+681.50
115	X_{O111}	-2735.00	+681.50
116	X_{O112}	-2885.00	+681.50
117	X_{O113}	-3035.00	+681.50
118	X_{O114}	-3185.00	+681.50
119	X_{O115}	-3335.00	+681.50
120	X_{O116}	-3485.00	+681.50
121	X_{O117}	-3635.00	+681.50
122	X_{O118}	-3785.00	+681.50
123	X_{O119}	-3935.00	+681.50
124	X_{O120}	-4085.00	+681.50
125	P	-4235.00	+681.50
126	V_{DD}	-4950.00	+681.50
127	V_{SS}	-4981.00	-681.50
128	V_{EE}	-4846.00	-681.50

Note The pad size of V_{DD} is 120 × 116 μm. The size of all other pads are 120 μm□

TIMING CHART



Note Do not use a sequence in which all the outputs change at a time because it may cause a malfunction. Inserting a bypass capacitor of 0.1 μF or so between V_{DD} and V_{EE} is recommended. Fix the unused pins to the V_{EE} level.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	RATINGS	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	−0.5 to +22	V	
Supply Voltage	V_{DD}-V_{EE}	−0.5 to +28	V	
Supply Voltage	V_{EE}	−17 to +0.5	V	
Input Voltage	V_I	V_{EE} − 0.5 to V_{DD} + 0.5	V	
Input Current	I_I	±10	mA	
Output Current	I_O	±10	mA	
Operating Temperature	T_{opt}	−20 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10		20	V	
Supply Voltage	V_{EE}	−15		−5	V	
Supply Voltage	V_{DD}-V_{EE}	15		25	V	

ELECTRICAL CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 13 V, V_{EE} = −7 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
High-Level Input Voltage	V_{IH}	3.5		V_{DD}	V	
Low-Level Input Voltage	V_{IL}	V_{EE}		1.5	V	
High-Level Output Voltage	V_{OH}	V_{DD} − 0.05		V_{DD}	V	P pin, no load
Low-Level Output Voltage	V_{OL}	V_{EE}		V_{EE} + 0.05	V	P pin, no load
High-Level Output Current	I_{XOH}			−2.0	mA	Driver output, V_O = V_{DD} − 1 V
Low-Level Output Current	I_{XOL}	2.0			mA	Driver output, V_O = V_{EE} + 1 V
High-Level Output Current	I_{POH}			−2.0	mA	P pin, V_O = V_{DD} − 1 V
Low-Level Output Current	I_{POL}	2.0			mA	P pin, V_O = V_{EE} + 1 V
Input Leakage Current	I_{IL}			±1	μA	V_I = 0 V or 5 V
Dynamic Current Consumption	I_{DD}			600	μA	V_{DD} pin, f_{IN} = 15.7 kHz

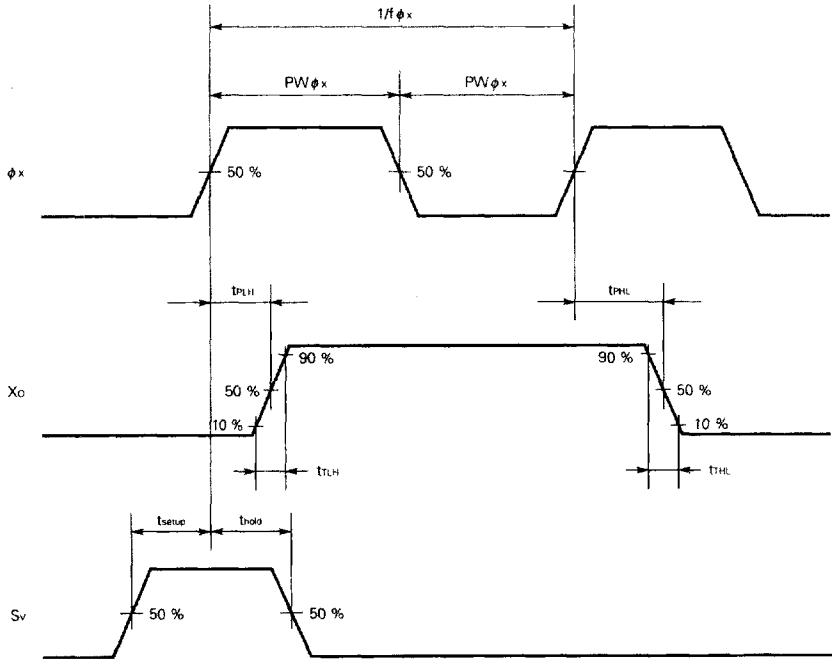
SWITCHING CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 13 V, V_{EE} = −7 V, V_{SS} = 0 V)

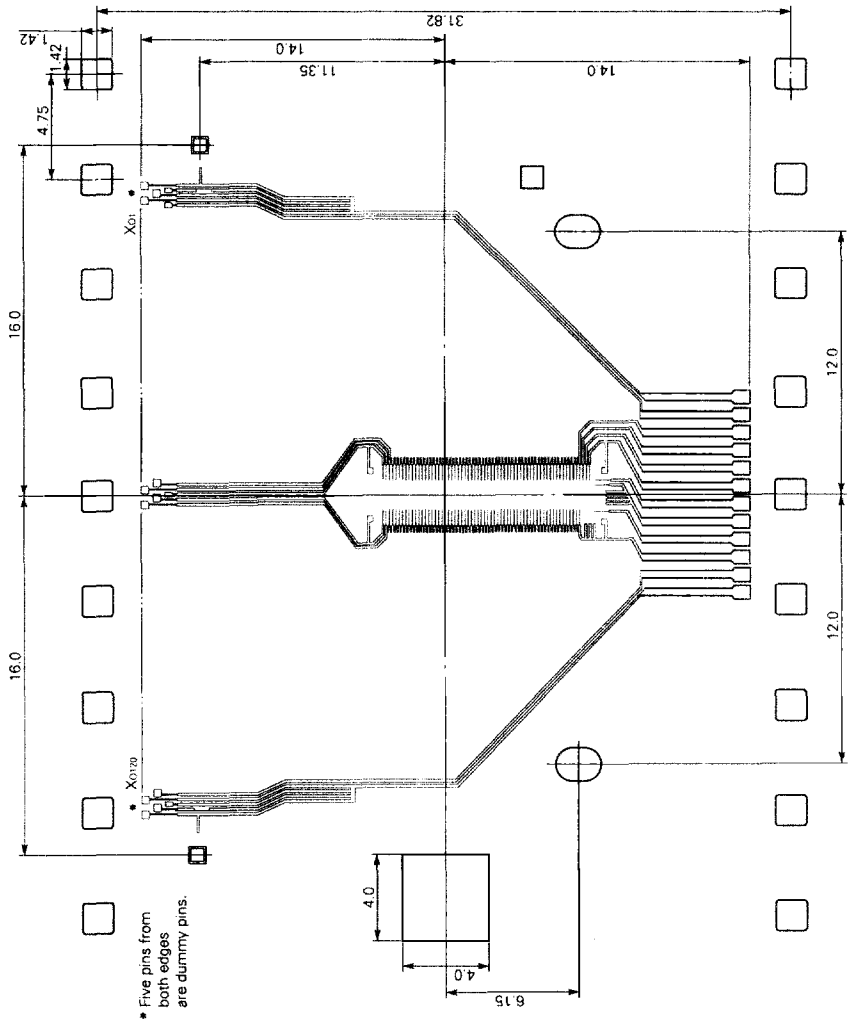
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
P Output Delay Time	t_{PHL}			400	ns	C_L = 20 pF
	t_{PLH}			400	ns	
Driver Output Delay Time	t_{PHL}			700	ns	C_L = 220 pF
	t_{PLH}			700	ns	
Output Fall Time	t_{PHL}			250	ns	C_L = 220 pF
Output Rise Time	t_{PLH}			250	ns	
Input Capacitance	C_I			15	pF	T_a = 25 °C
Maximum Clock Frequency	f_{MAX}	1.0			MHz	In cascade connection

TIMING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Clock Pulse Width	$PW\phi x$	500			ns	Duty = 50 %
Data Setup Time	t_{setup}	100			ns	
Data Hold Time	t_{hold}	100			ns	

SWITCHING CHARACTERISTIC WAVEFORMS




31.82
14.0
11.35
14.0
1.42
1.42
4.75
16.0
16.0
12.0
12.0
4.0
4.0
6.15
* Five pins from both edges are dummy pins.