INTEGRATED CIRCUITS
UNITRODE

UC1875/6/7/8
UC2875/6/7/8
UC3875/6/7/8

Phase Shift Resonant Controller

FEATURES

- Zero to 100% Duty Cycle Control
- Programmable Output Turn-On Delay
- Compatible with Voltage or Current Mode Topologies
- Practical Operation @ Switching Frequencies to 1MHz
- Four 2A Totem Pole Outputs
- 10MHz Error Amplifier
- Under Voltage Lockout
- Low Start-Up Current —150μA
- Outputs Active Low During UVLO
- Soft-Start Control
- Latched Over-Current Comparator With Full Cycle Restart
- Trimmed Reference

Device	UVLO Turn-On	UVLO Turn-Off	Delay Set
UC1875	10.75	9.25V	Yes
UC1876	15.25V	9.25V	Yes
UC1877	10.75V	9.25V	No
UC1878	15.25V	9.25V	No

DESCRIPTION

The UC1875 family of integrated circuits implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This family of circuits may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

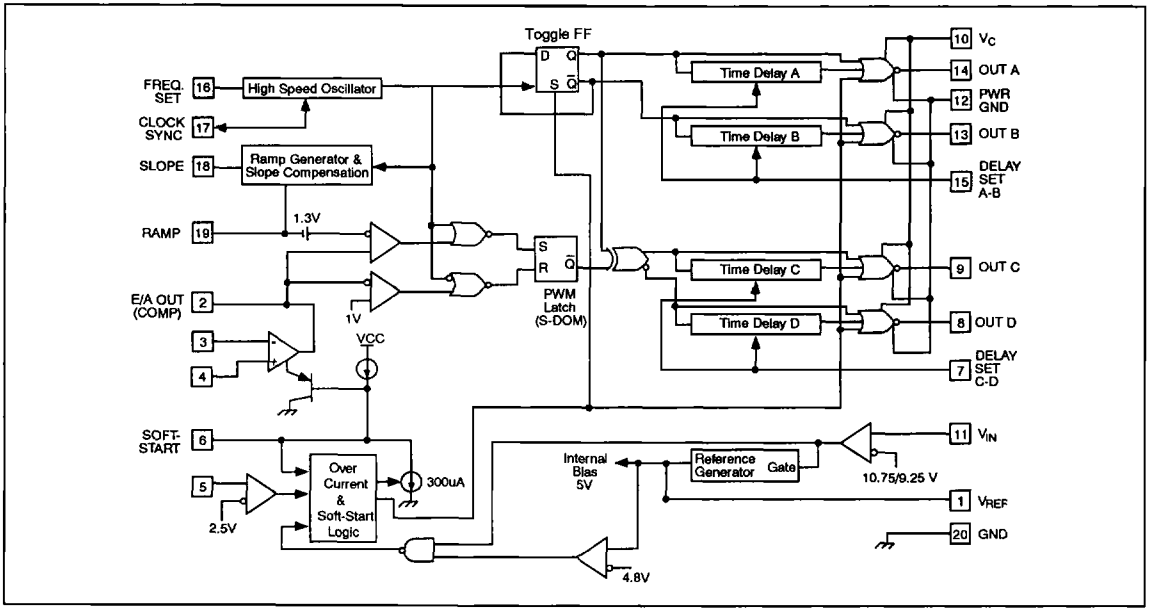
With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCK/SYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an under-voltage lock-out which maintains all outputs in an active-low state until the supply reaches a 10.75V threshold. 1.5V hysteresis is built in for reliable, boot-strapped chip supply. Over-current protection is provided , and will latch the outputs in the OFF state within 70nsec of a fault. The current-fault circuitry implements full-cycle restart operation.

Additional features include an error amplifier with bandwidth in excess of 7MHz, a 5V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

These devices are available in 20-pin DIP, 28-pin "bat-wing" SOIC and 28 lead power PLCC plastic packages for operation over both 0°C to 70°C and -25°C to +85°C temperature ranges; and in hermetically sealed cerdip, and surface mount packages for -55°C to +125°C operation.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_C, V_{IN}) 20V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 3A
Analog I/Os (Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19) ..... -0.3 to 5.3V
Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to + 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

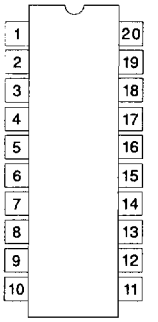
Note:
- Pin references are to 20 pin packages.
- All voltages are with respect to ground, DIL pin 20.
- Currents are positive into, negative out of, device terminals.
- Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

PACKAGE PIN FUNCTIONS

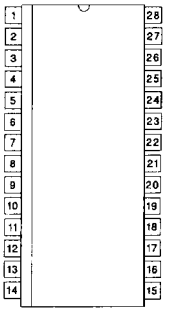
	PACKAGE TYPE and PIN NUMBER		
Function	**20-pin N, J**	**28-pin QP**	**28-pin DWP**
VREF	1	19	1
E/A OUT (COMP)	2	20	2
E/A (-)	3	21	3
E/A (+)	4	22	4
C/S (+)	5	23	5
SOFT-START	6	24	6
DELAY SET C/D	7	25	10
OUT D	8	26	12
OUT C	9	27	13
VC	10	28	14
VIN	11	1	15
PWR GND	12	2	16
OUT B	13	3	17
OUT A	14	4	18
DELAY SET A/B	15	7	23
FREQ SET	16	8	24
CLOCK/SYNC	17	9	25
SLOPE	18	10	26
RAMP	19	11	27
GND	20	12-18	7-9,11,19-22, 28

CONNECTION DIAGRAMS

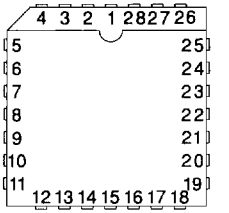
DIL-20 (TOP VIEW)
J or N PACKAGE



SOIC-28 (TOP VIEW)
DWP PACKAGE



PLCC-28 (TOP VIEW)
QP PACKAGE



Electrical Characteristics: Unless otherwise stated, V_C = V_{IN} = 12V, $R_{FREQ\ SET}$ = 12kΩ, $C_{FREQ\ SET}$ = 330pF, R_{SLOPE} = 12kΩ, C_{RAMP} = 200pF, $C_{DELAY\ SET\ A-B}$ = $C_{DELAY\ SET\ C-D}$ = 0.01µF, $I_{DELAY\ SET\ A-B}$ = $I_{DELAY\ SET\ C-D}$ = -500µA, -55°C<T_A<125°C for the UC1875/6/7/8 -25°C<T_A<85°C for the UC2875/6/7/8 and 0°C<T_A<70°C for the UC3875/6/7/8 T_A=T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Under-Voltage Lockout					
Start Threshold	UC1875/UC1877		10.75	11.75	V
	UC1876/UC1878		15.25		V
UVLO Hysteresis	UC1875/UC1877	0.5	1.25	2.0	V
	UC1876/UC1878		6.0		V
Supply Current					
IIN Startup	VIN = 8V, VC = 20V, RSLOPE open, IDELAY =0		150	600	µA
IC Startup	VIN = 8V, VC = 20V, RSLOPE open, IDELAY =0		10	100	µA
IIN			30	40	mA
IC			15	30	mA

Electrical Characteristics: Unless otherwise stated, $V_C = V_{IN} = 12V$, $R_{FREQ\ SET} = 12k\Omega$, $C_{FREQ\ SET} = 330pF$, $R_{SLOPE} = 12k\Omega$, $C_{RAMP} = 200pF$, $C_{DELAY\ SET\ A-B} = C_{DELAY\ SET\ C-D} = 0.01\mu F$, $I_{DELAY\ SET\ A-B} = I_{DELAY\ SET\ C-D} = -500\mu A$, $-55°C<T_A<125°C$ for the UC1875/6/7/8, $-25°C<T_A<85°C$ for the UC2875/6/7/8, and $0°C<T_A<70°C$ for the UC3875/6/7/8, $T_A=T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Voltage Reference					
Output Voltage	T_J = + 25°C	4.94	5	5.06	V
Line Regulation	$11<V_{IN}<20V$		1	10	mV
Load Regulation	I_{VREF} = -10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.9		5.1	V
Noise Voltage	10Hz to 10kHz		50		μVrms
Long Term Stability	T_J = 125°C, 1000 hours		2.5		mV
Short Circuit Current	V_{REF} = 0V, T_J = 25°C		60		mA
Error Amplifier					
Offset Voltage			5	15	mV
Input Bias Current			0.6	3	μA
AVOL	$1 < V_{COMP} < 4V$	60	90		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR	$11 < V_{IN} < 20V$	85	100		dB
Output Sink Current	V_{COMP}=1V	1	2.5		mA
Output Source Current	V_{COMP}=4V		-1.3	- 0.5	mA
Output Voltage High	I_{COMP} = -0.5mA	4	4.7	5	V
Output Voltage Low	I_{COMP} = 1mA	0	0.5	1	V
Unity Gain BW		7	11		MHz
Slew Rate		6	11		V/μsec
PWM Comparator					
Ramp Offset Voltage	TJ = 25°C, Note 3		1.3		V
Zero Phase Shift Voltage	Note 4	0.55	0.9		V
PWM Phase Shift	V_{COMP} > (Ramp Peak + Ramp Offset)	98	99.5	102	%
(Note 1)	V_{COMP} < Zero Phase Shift Voltage	0	0.5	2	%
Output Skew	V_{COMP} > Ramp Peak		5	±20	nsec
(Note 1)	V_{COMP} < 1V		5	±20	nsec
Ramp to Output Delay	Note 6		50	100	nsec
Oscillator					
Initial Accuracy	T_J = 25°	0.85	1	1.15	MHz
Voltage Stability	$11 < V_{IN} < 20V$		0.2	2	%
Total Variation	Line, Temperature	0.80		1.20	MHz
Sync Pin Threshold	T_J = 25°C		3.8		V
Clock Out Peak	T_J = 25°C		4.3		V
Clock Out Low	T_J = 25°C		3.3		V
Clock Out Pulse Width	$R_{CLOCK/SYNC} = 3.9k\Omega$		30	100	nsec
Maximum Frequency	$R_{FREQSET} = 5k\Omega$	2			MHz
Ramp Generator/Slope Compensation					
Ramp Current, Minimum	$I_{SLOPE} = 10\mu A$, $V_{FREQ\ SET} = V_{REF}$		-11	-14	μA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQ\ SET} = V_{REF}$	-0.8	-0.95		mA
Ramp Valley			0		V
Ramp Peak - Clamping Level	$R_{FREQ\ SET} = 100k\Omega$	3.8	4.1		V
Current Limit					
Input Bias	VC/S+ = 3V		2	5	μA

Electrical Characteristics: Unless otherwise stated, $V_C = V_{IN} = 12V$, $R_{FREQ\ SET} = 12k\Omega$, $C_{FREQ\ SET} = 330pF$, $R_{SLOPE} = 12k\Omega$, $C_{RAMP} = 200pF$, $C_{DELAY\ SET\ A\text{-}B} = C_{DELAY\ SET\ C\text{-}D} = 0.01\mu F$, $I_{DELAY\ SET\ A\text{-}B} = I_{DELAY\ SET\ C\text{-}D} = -500\mu A$, $-55°C<T_A<125°C$ for the UC1875/6/7/8, $-25°C<T_A<85°C$ for the UC2875/6/7/8, and $0°C<T_A<70°C$ for the UC3875/6/7/8, $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit (continued)					
Threshold Voltage		2.4	2.5	2.6	V
Delay to Output			70	125	nsec
Soft-Start/Reset Delay					
Charge Current	$V_{SOFT\text{-}START} = 0.5V$	-20	-9	-3	µA
Discharge Current	$V_{SOFT\ START} = 1V$	140	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level	$I_{OUT} = 50mA$		0.2	0.4	V
	$I_{OUT} = 500mA$		1.2	2.6	V
Output High Level	$I_{OUT} = -50mA$		1.5	2.5	V
	$I_{OUT} = -500mA$		1.7	2.6	V
Delay Set (UC1875 and UC1876 only)					
Delay Set Voltage	$I_{DELAY} = -500\mu A$	2.3	2.4	2.6	V
Delay Time	$I_{DELAY} = -250\mu A$ (NOTE 5)	150	250	400	nsec

Note 1: Phase shift percentage (0% = 0°, 100% = 180°) is defined as

$$\theta = \frac{200}{T}\ \Phi\ \%,$$

where θ is the phase shift, and Φ and T are defined in Figure1.
At 0% phase shift, Φ is the output skew.

Note 2: Delay time is defined as

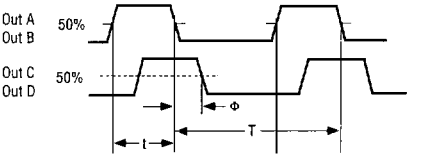
$$\text{delay} = T\left(\frac{1}{2}\text{-(duty cycle)}\right),$$

where T is defined in figure 1.

Note 3: Ramp offset voltage has a temperature coeffecient of about -4mV/°C.
Note 4: Zero phase shift voltage has a temperature coeffecient of about -2mV/°C.
Note 5: Delay time can be programmed via resistors from the delay set pins to ground. Delay time $\cong \frac{62.5 \times 10^{-12}}{I_{DELAY}}$ sec.

Where $I_{DELAY} = \frac{\text{Delay set voltage}}{R_{DELAY}}$ The recommended range for I_{DELAY} is $25\mu A \le I_{DELAY} \le 1mA$

Note 6: Ramp delay to output time is defined in figure 2.



Duty Cycle = $\frac{t}{T}$
Period = T
T_{DHL} (A to C) = T_{DHL} (B to D) = Φ

Phase Shift, Output Skew & Delay Time Definitions

FIGURE 1

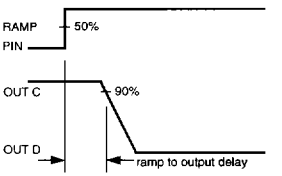


FIGURE 2

PIN FUNCTIONAL DESCRIPTION

GND (signal ground):
All voltages are measured with respect to GND. The timing capacitor, on the FREQ SET pin, any bypass capacitor on the V_{REF} pin, bypass capacitors on V_{IN} and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

PWR GND (power ground):
V_C should be bypassed with a ceramic capacitor from the Vc pin to the section of the ground plane that is connected to PWR GND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

Vc (output switch supply voltage):
This pin supplies power to the output drivers and their associated bias circuitry. Connect Vc to a stable source above 3V for normal operation, above 12V for best performance. This supply should be bypassed directly to the PWR GND pin with low ESR, low ESL capacitors.

V_{IN} (primary chip supply voltage):
This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect V_{IN}

PIN FUNCTIONAL DESCRIPTION (CONTINUED)

to a stable source above 12V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper under-voltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE: When VIN exceeds the UVLO threshold the supply current (IIN) will jump from about 100uA to a current in excess of 20mA. If the UC1875 is not connected to a well bypassed supply, it may immediately enter UVLO again.

FREQ SET (oscillator frequency set pin)
A resistor and a capacitor from FREQ SET to GND will set the oscillator frequency.

CLOCK/SYNC (bi-directional clock and synchronization pin):
Used as as output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCK/SYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

SLOPE (set ramp slope/slope compensation):
A resistor from this pin to Vcc will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

RAMP (voltage ramp):
This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{sense voltage}}{R_{SLOPE} \bullet C_{RAMP}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation - see the applications information section for further information.
Because of the 1.3V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of R_{SLOPE} and C_{RAMP}.

E/A OUT (COMP) (Error amplifier output):
This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

E/A - (Error Amplifier inverting input):
This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

E/A+ (Error Amplifier non-inverting input):
This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the E/A- pin.

SOFT-START:
SOFT-START will remain at GND as long as V_{IN} is below the UVLO threshold. SOFT-START will be pulled up to about 4.8V by an internal 9µA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (C/S+ voltage exceeding 2.5V), SOFT-START will be pulled to GND and them ramp to 4.8V. If a fault occurs during the SOFT-START cycle, the outputs will be immediately disabled and SOFT-START must charge fully prior to resetting the fault latch.
For paralleled controllers, the SOFT-START pins may be paralled to a single capacitor, but the charge currents will be additive.

C/S+ (current sense):
The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5V (separate from VREF). When the voltage at this pin exceeds 2.5V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled from switching and held in a low state until the C/S+ pin is brought below 2.5V. The outputs may begin switching at 0 degrees phase shift before the SOFT-START pin begins to rise -- this condition will not prematurely deliver power to the load.

OUT A-OUT D (outputs A-D):
The outputs are 2A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with recpect to the A-B outputs.

DELAY SET A-B, DELAY SET C-D (output delay control):
The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

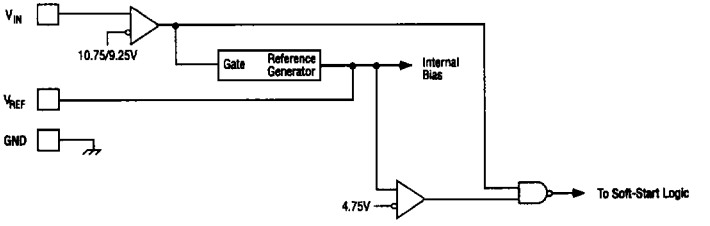
VREF:
This pin is an accurate 5V voltage reference. This output is capable of delivering about 60mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75V. For best results bypass VREF with a 0.1uF, low ESR, low ESL, capacitor to the GND pin.

APPLICATIONS INFORMATION

UNDER VOLTAGE LOCKOUT SECTION

When power is applied to the circuit and V_{IN} is below the upper UVLO threshold, I_{IN} will be below 600µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low.

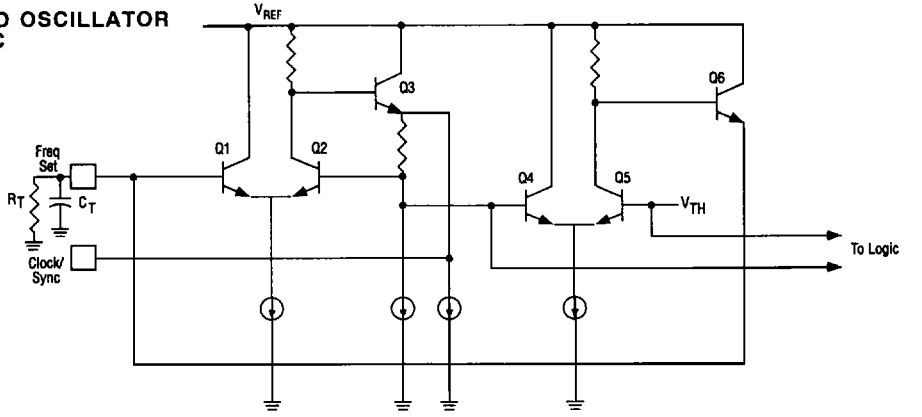
When V_{IN} exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, V_{REF}, exceeds 4.75V

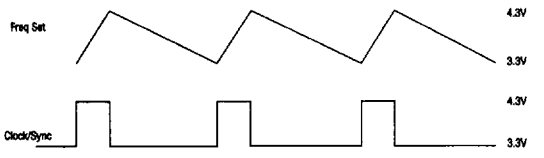


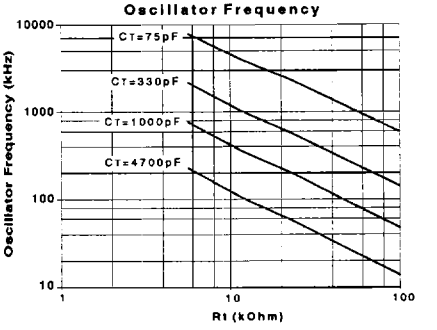
OSCILLATOR

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQ. SET pin.

SIMPLIFIED OSCILLATOR SCHEMATIC





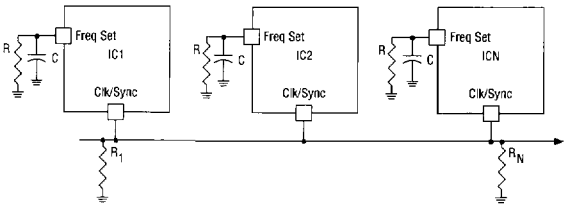


The CLOCK/SYNC pin of the oscillator may be used to synchronize multiple UC1875 devices simply by connecting the CLOCK/SYNC of each UC1875 to the others:

APPLICATIONS INFORMATION (CONTINUED)

SYNCHRONIZING THE OSCILLATOR

1875/6/7/8's only

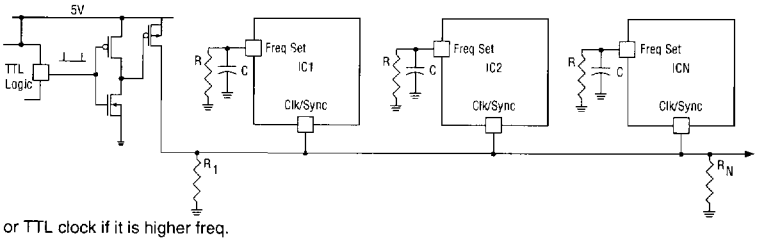


All ICs will sync to chip with the fastest local oscillator.

R_1 & R_N *may* be needed to keep sync pulse narrow due to capacitance on line.

R_1 & R_N *may* also be needed to properly terminate rsync line.

Syncing to external TTL/CMOS



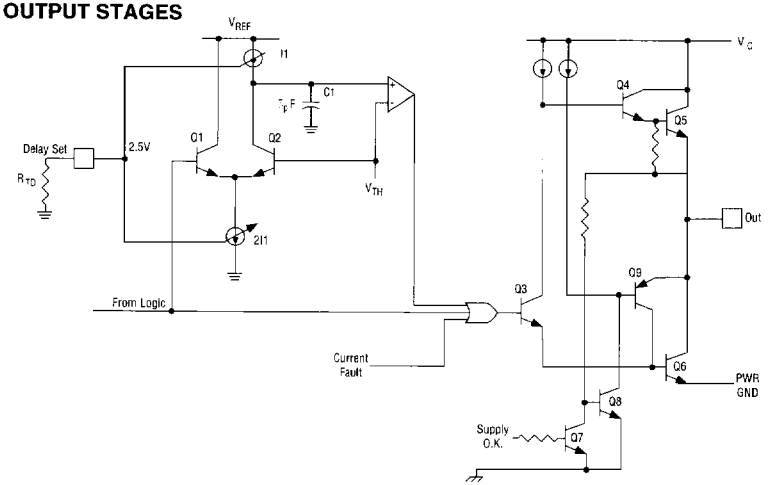
ICs will sync to fastest chip or TTL clock if it is higher freq.
R & R_N *may* be needed for same reasons as above

Although each UC1875/6/7/8 has a local oscillator frequency, the group of devices will synchronize to the fastest oscillator driving the CLOCK/SYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.
Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in the previous figure. Capacitive loading on the CLOCK/SYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCK/SYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R_T,RN.

DELAY BLOCKS AND OUTPUT STAGES

In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.

SIMPLIFIED OUTPUT STAGES

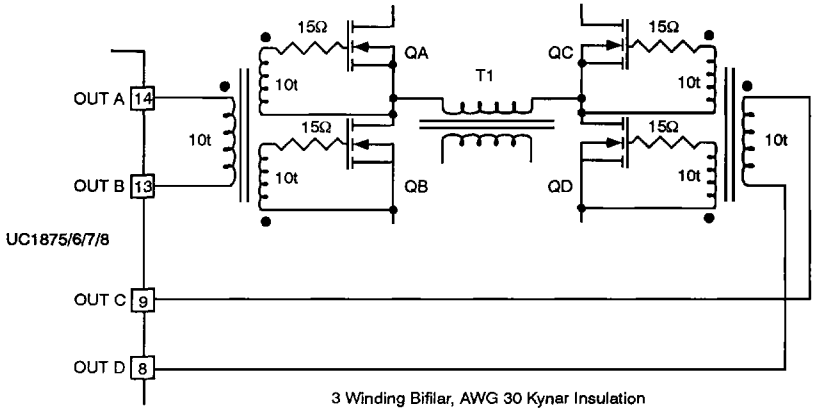


The delay providing the dead-time is accomplished with C1 which must discharge to Vth before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, RTD. The voltage on the Delay Set pins is internally regulated to 2.5V and the range of dead time control is from 50 to 200 nanoseconds. NOTE: There is no way to disable the delay circuitry, and the delay time must be programmed.

APPLICATIONS INFORMATION (CONTINUED)

OUTPUT SWITCH ORIENTATION

The four outputs of the UC1875/6/7/8 interace to the full bridge converter switches as shown below:



3 Winding Bifilar, AWG 30 Kynar Insulation

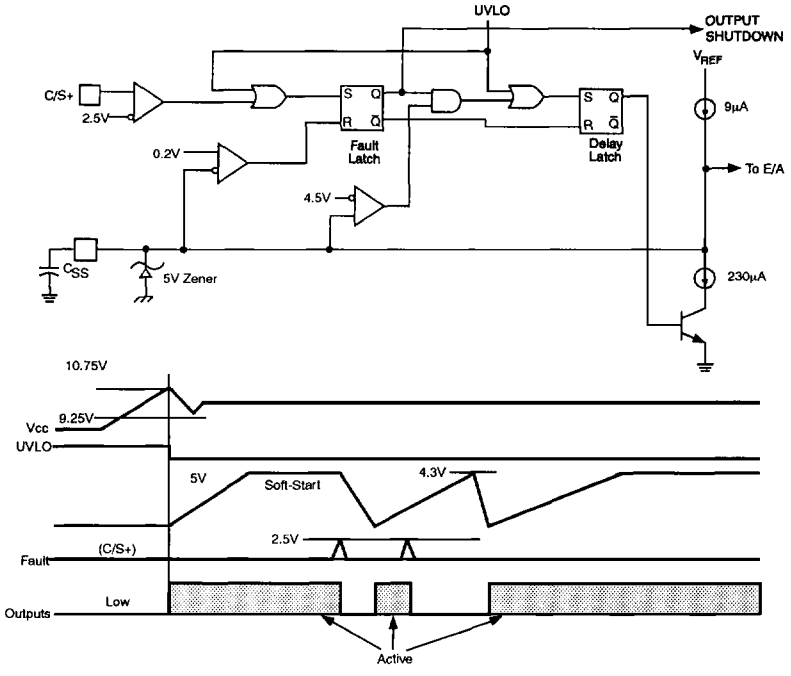
FAULT LOGIC

The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFT-START pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.
The fault logic insures that a continuous fault will institute a low frequency "hiccup" retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.

FAULT/SOFT-START



APPLICATIONS INFORMATION (CONTINUED)

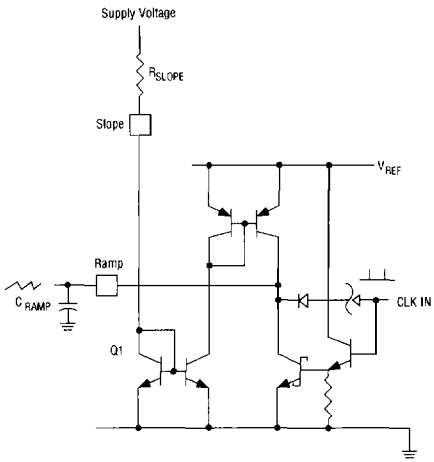
RAMP GENERATION

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

SLOPE/RAMP PINS

Voltage Mode Operation



1. Simple voltage mode operation achieved by placing RSLOPE between VIN & SLOPE

2. Voltage Feedforward achieved by placing RSLOPE between supply voltage and slope pin of UC1875.

$$\text{Ramp} \quad \frac{dV}{dT} \approx \frac{V_{RSLOPE}}{R_{SLOPE}\, C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

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7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460