PRELIMINARY

Delta39K™ ISR™ CPLD Family

CPLDs at FPGA Densities™

Features

- High density
  - 30K to 350K usable gates
  - 512 to 5376 macrocells
  - 136 to 520 maximum I/O pins
  - 12 Dedicated Inputs including 4 clock pins, 4 global I/O control signal pins and 4 JTAG interface pins for boundary scan & reconfigurability
- Embedded Memory
  - 80K to 840K bits embedded SRAM
    - 64K to 672K bits of (single port) Cluster memory
    - 16K to 168K bits of (dual port) Channel memory
- High speed – 233-MHz in-system operation
- AnyVolt™ interface
  - 3.3V, 2.5V, and 1.8V V_{CC} versions available
  - 3.3V, 2.5V, and 1.8V I/O capability on all versions
- Low Power Operation
  - 0.18-μm 6-layer metal SRAM-based logic process
  - Full-CMOS implementation of product term array
  - Standby current as low as 200 μA at 1.8V V_{CC}
- Simple timing model
  - No penalty for using full 16 product terms / macrocell
  - No delay for single product term steering or sharing
- Flexible clocking
  - 4 synchronous clocks per device
  - 1 spread-aware PLL drives all 4 clock networks
  - Locally generated Product Term clock
  - Clock polarity control at each register
- Carry-chain logic for fast and efficient arithmetic operations
- Multiple I/O standards supported
  - LVCMOS (3.3/3.0/2.5/1.8V), LVTTL, 3.3V PCI, SSTL2 (I-II), SSTL3 (I-II), HSTL (I-IV), and GTL+
- Compatible with NOBL™, ZBT™, and QDR™ SRAMs
- Programmable slew rate control on each I/O pin
- User-Programmable Bus Hold capability on each I/O pin
- Fully PCI compliant (to 66 MHz 64-bit PCI spec rev2.2)
- CompactPCI hot swap ready
- Multiple package/pinout offering across all densities
  - 208 to 676 pins in PQFP, BGA and FBGA packages
  - Same pinout for 3.3V/2.5V and 1.8V devices
  - Simplifies design migration across density
  - Self-Boot™ solution in BGA and FBGA packages
- In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
- IEEE1149.1 JTAG boundary scan

Development Software

- *Warp®*
  - IEEE 1076/1164 VHDL or IEEE 1364 Verilog context sensitive editing.
  - Active-HDL FSM graphical finite state machine editor
  - Active-HDL SIM post-synthesis timing simulator
  - Architecture Explorer for detailed design analysis
  - Static Timing Analyzer for critical path analysis
  - Available on Windows 95™, Windows 98™ & Windows NT™ for $99
  - Supports all Cypress programmable logic products

Delta39K™ ISR CPLD Family Members

Device	Typical Gates[1]	Macrocells	Cluster memory (Kbits)	Channel memory (Kbits)	Maximum I/O Pins	f_{MAX2} (MHz)	Speed - t_{PD} Pin-to-Pin (ns)	Standby I_{CC}[2] T_A=25°C	
								3.3/2.5V	1.8V
39K30	16K–48K	512	64	16	176	233	7.2	10 mA	200 μA
39K50	23K–72K	768	96	24	218	233	7.2	10 mA	300 μA
39K100	46K–144K	1536	192	48	302	222	7.5	10 mA	600 μA
39K165	77K–241K	2560	320	80	386	181	8.5	10 mA	1250 μA
39K200	92K–288K	3072	384	96	428	181	8.5	10 mA	1250 μA
39K250	115K–361K	3840	480	120	470	167	8.5	10 mA	1500 μA
39K350	161K–505K	5376	672	168	520	154	9.0	10 mA	2100 μA

Note:
1. Upper limit of typical gates is calculated by assuming only 10% of the channel memory is used.
2. Standby I_{CC} values are with PLL not utilized, no output load and stable inputs

Delta39K Speed Bins[3]

Device	233	200	181	167	154	125	83
39K30	X					X	X
39K50	X					X	X
39K100		X				X	X
39K165			X			X	X
39K200			X			X	X
39K250				X		X	X
39K350					X	X	X

Device Package Offering and I/O Count Including Dedicated Clock and Control Inputs

Device	208-EQFP 28X28 mm 0.5-mm pitch	256-FBGA 17x17 mm 1.0-mm pitch	484-FBGA 23x23 mm 1.0-mm pitch	676-FBGA 27x27 mm 1.0-mm pitch	Self-Boot Solution[5]			
					256-FBGA 17x17 mm 1.0-mm pitch	388-BGA 35x35 mm 1.27-mm pitch	484-FBGA 23x23 mm 1.0-mm pitch	676-FBGA 27x27 mm 1.0-mm pitch
39K30	136	176			176			
39K50	136	180				218	218	
39K100	136	180	302			294		302
39K165	136		356			294		386
39K200	136		368			294		428
39K250	136			470		294		470
39K350	136			520		294		520

Notes:

3. Speed bins shown here are for Commercial operating range. Please refer to Delta39K
4. Information on page 41 for Industrial range speed bins.
5. Self-Boot solution integrates the boot PROM (Flash Memory) with Delta39K die inside the same package.

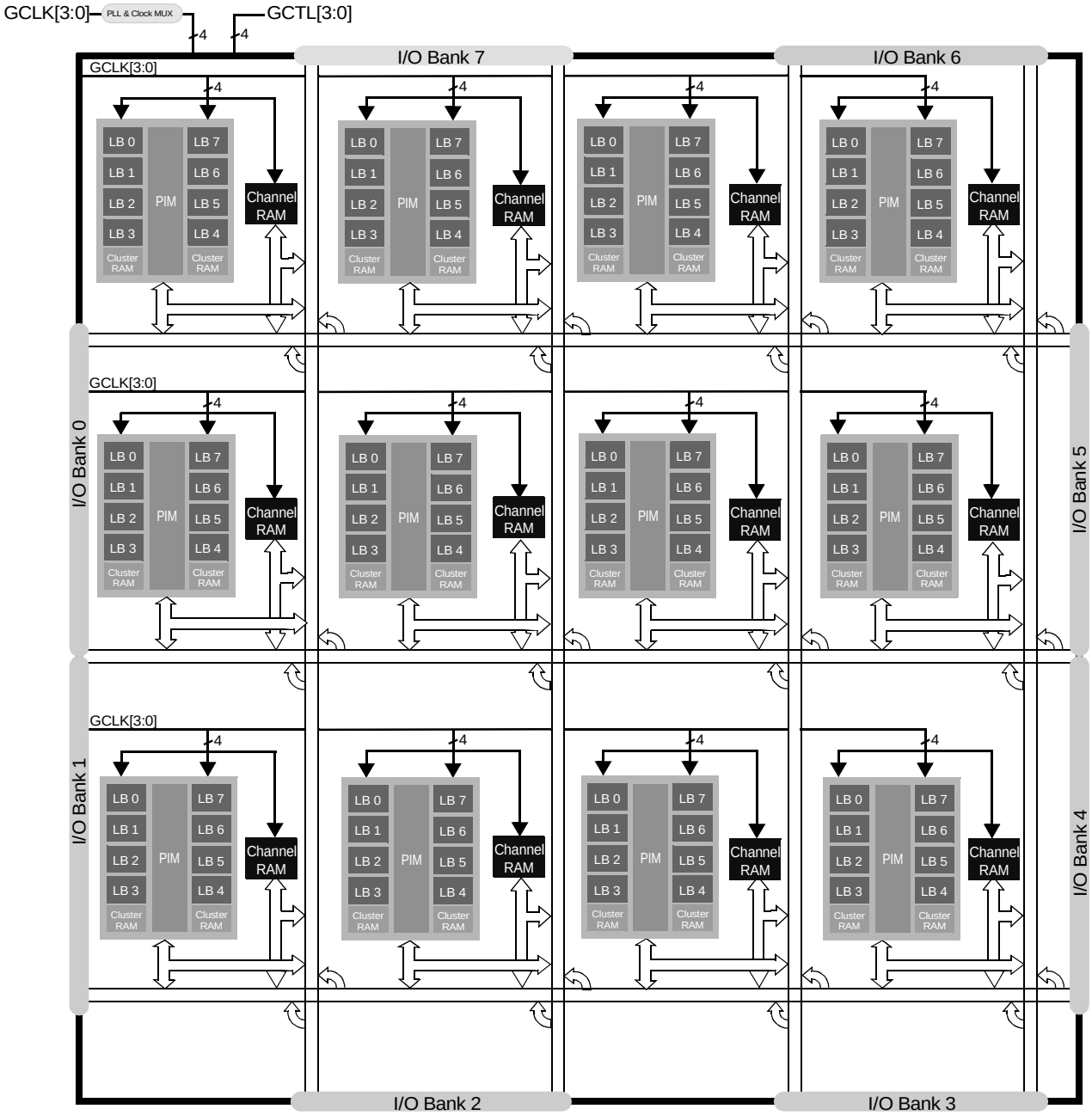


Figure 1. Delta39K100 Block Diagram (3 Rows x 4 Columns) with I/O Bank Structure

General Description

The Delta39K family, based on a 0.18-µm, 6-layer metal CMOS logic process, offers a wide range of high-density solutions at unparalleled system performance. The Delta39K family is designed to combine the high speed, predictable timing, and ease of use of CPLDs with the high densities and low power of FPGAs. With devices ranging from 15,000 to 350,000 usable gates, the family features devices ten times the size of previously available CPLDs. Even at these large densities, the Delta39K family is fast enough to implement a fully synthesizable 64-bit, 66-MHz PCI core.

The architecture is based on Logic Block Clusters (LBC) that are connected by Horizontal and Vertical (H&V) routing channels. Each LBC features eight individual Logic Blocks (LB) and two cluster memory blocks. Adjacent to each LBC is a channel memory block, which can be accessed directly from the I/O pins. Both types of memory blocks are highly configurable and can be cascaded in width and depth. See *Figure 1* for a block diagram of the Delta39K architecture.

All the members of the Delta39K family have Cypress's highly regarded In-System Reprogrammability (ISR) feature, which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes in most cases. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins respectively. Superior routability, simple timing, and the ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Delta39K family also features user programmable bus-hold and slew rate control capabilities on each I/O pin.

AnyVolt Interface

All Delta39KV devices feature an on-chip regulator, which accepts 3.3V or 2.5V on the V_{CC} supply pins and steps it down to 1.8V internally, the voltage level at which the core operates.

The Delta39KZ devices accept 1.8V on the V_{CC} supply pins directly. With Delta39K's AnyVolt technology, the I/O pins can be connected to either 1.8V, 2.5V, or 3.3V. All Delta39K devices are 3.3V tolerant regardless of V_{CCIO} or V_{CC} settings.

Device	V_{CC}	V_{CCIO}
39KV	3.3V or 2.5V	3.3V or 2.5V or 1.8V or 1.5V[6]
39KZ	1.8V	3.3V or 2.5V or 1.8V or 1.5V[6]

Global Routing Description

The routing architecture of the Delta39K is made up of horizontal and vertical (H&V) routing channels. These routing channels allow signals from each of the Delta39K architectural components to communicate with one another. In addition to the horizontal and vertical routing channels that interconnect the I/O banks, channel memory blocks, and logic block clusters, each LBC contains a Programmable Interconnect Matrix (PIM™), which is used to route signals among the logic blocks and the cluster memory blocks.

Figure 2 is a block diagram of the routing channels that interface within the Delta39K architecture. The LBC is exactly the same for every member of the Delta39K CPLD family.

Logic Block Cluster (LBC)

The Delta39K architecture consists of several logic block clusters, each of which have eight Logic Blocks (LB) and two cluster memory blocks connected via a Programmable Interconnect Matrix (PIM) as shown in *Figure 3*. Each cluster memory block consists of 8-Kbit single-port RAM, which is configurable as synchronous or asynchronous. The cluster memory blocks can be cascaded with other cluster memory blocks within the same LBC as well as other LBCs to implement larger memory functions. If a cluster memory block is not specifically utilized by the designer, Cypress's *Warp* software can automatically use it to implement large blocks of logic.

All LBCs interface with each other via horizontal and vertical routing channels.

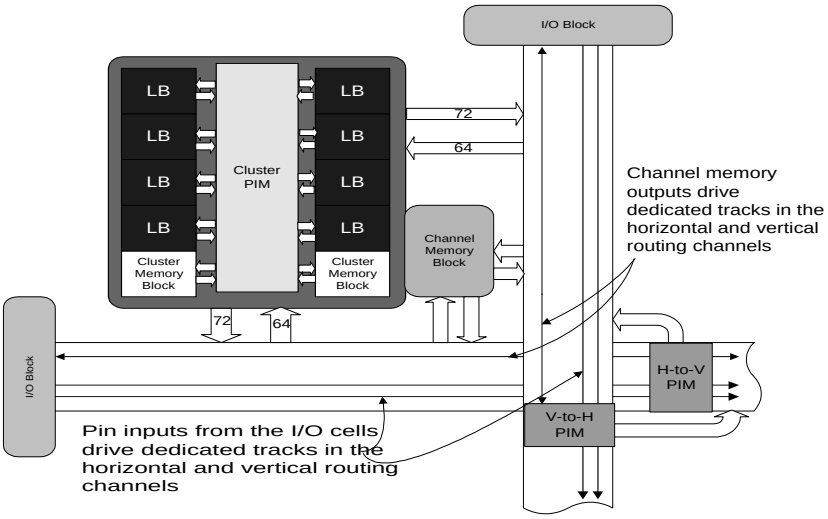


Figure 2. Delta39K Routing Interface

Note:
6. For HSTL only.

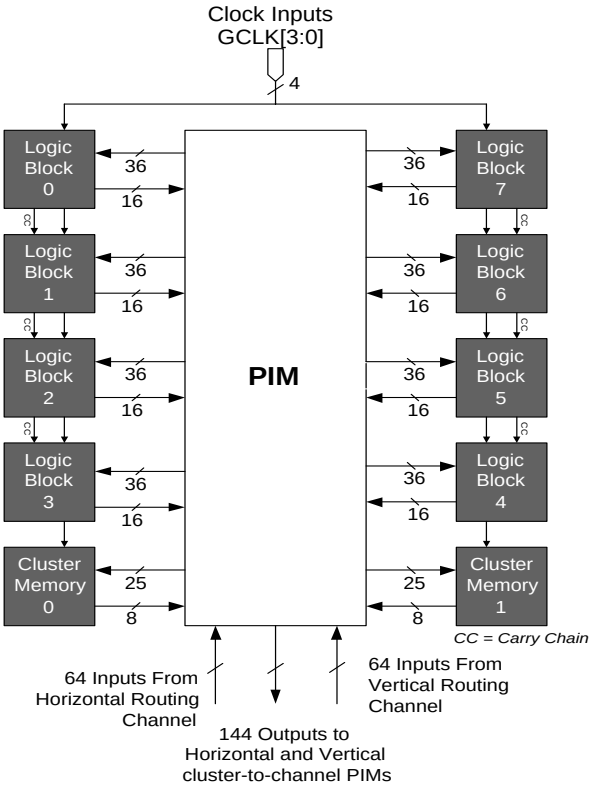


Figure 3. Delta39K Logic Block Cluster Diagram

Logic Block (LB)

The logic block is the basic building block of the Delta39K architecture. It consists of a product term array, an intelligent product-term allocator, and 16 macrocells.

Product Term Array

Each logic block features a 72 x 83 programmable product term array. This array accepts 36 inputs from the PIM. These inputs originate from device pins and macrocell feedbacks as well as cluster memory and channel memory feedbacks. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 83 product terms in the array can be created from any of the 72 inputs.

Of the 83 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Two of the remaining three product terms in the logic block are used as asynchronous set and asynchronous reset product terms. The final product term is the Product Term clock (PTCLK) and is shared by all 16 macrocells within a logic block.

Product Term Allocator

Through the product term allocator, *Warp* software automatically distributes the 80 product terms as needed among the 16 macrocells in the logic block. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Delta39K devices, product terms are steered on an individual basis. Any number between 1and 16 product terms can be steered to any macrocell.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one function has one or more product terms in its equation that are common to other functions, those product terms are only programmed once. The Delta39K product term allocator allows sharing across groups of four macrocells in a variable fashion. The software automatically takes advantage of this capability so that the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All steering and sharing configurations have been incorporated in the timing specifications for the Delta39K devices.

Macrocell

Within each logic block there are 16 macrocells. Each macrocell accepts a sum of up to 16 product terms from the product term array. The sum of these 16 product terms can be output in either registered or combinatorial mode. *Figure 4* displays the block diagram of the macrocell. The register can be asynchronously preset or asynchronously reset at the macrocell level with the separate preset and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be preset or reset based on an AND expression or an OR expression.

An XOR gate in the Delta39K macrocell allows for many different types of equations to be realized. It can be used as a polarity mux to implement the true or complement form of an equation in the product term array or as a toggle to turn the D flip-flop into a T flip-flop. The carry-chain input mux allows additional flexibility for the implementation of different types of logic. The macrocell can utilize the carry chain logic to implement adders, subtractors, magnitude comparators, parity tree, or even generic XOR logic. The output of the macrocell is either registered or combinatorial.

Carry Chain Logic

The Delta39K macrocell features carry chain logic which is used for fast and efficient implementation of arithmetic operations. The carry logic connects macrocells in up to 4 logic blocks for a total of 64 macrocells. Effective data path operations are implemented through the use of carry-in arithmetic, which drives through the circuit quickly. *Figure 4* shows that the carry chain logic within the macrocell consists of two product terms (CPT0 and CPT1) from the PTA and an input carry-in for carry logic. The inputs to the carry chain mux are connected directly to the product terms in the PTA. The output of the carry chain mux generates the carry-out for the next macrocell in the logic block as well as the local carry input that is connected to an input of the XOR input mux. Carry-in and a configuration bit are inputs to an AND gate. This AND gate provides a method of segmenting the carry chain in any macrocell in the logic block.

Macrocell Clocks

Clocking of the register is highly flexible. Four global synchronous clocks (GCLK[3:0]) and a Product Term clock (PTCLK) are available at each macrocell register. Furthermore, a clock polarity mux within each macrocell allows the register to be clocked on the rising or the falling edge (see macrocell diagram in *Figure 4*).

PRESET/RESET Configurations

The macrocell register can be asynchronously preset and reset using the PRESET and RESET mux. Both signals are active high and can be controlled by either of two Preset/Reset product terms (PRC[1:0] in *Figure 4*) or GND. In situations where the PRESET and RESET are active at the same time, RESET takes priority over PRESET.

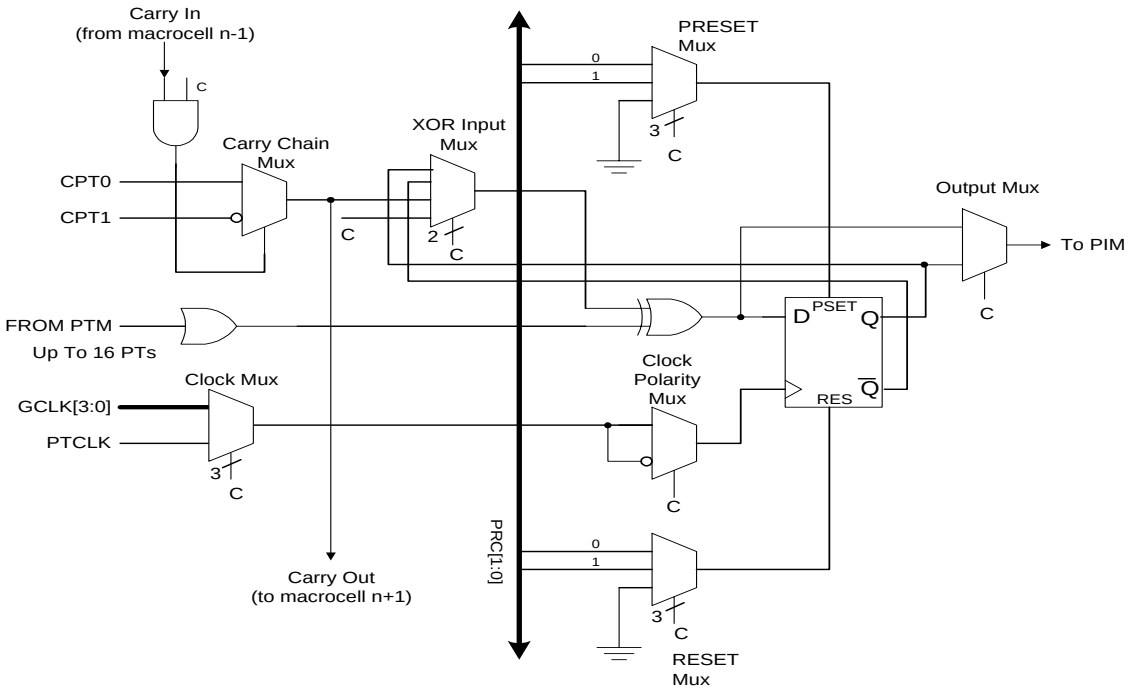


Figure 4. Delta39K Macrocell

Embedded Memory

Each member of the Delta39K family contains two types of embedded memory blocks. The channel memory block is placed at the intersection of horizontal and vertical routing channels. Each channel memory block is 4096 bits in size and can be configured as asynchronous or synchronous Dual-Port RAM, Single-Port RAM, Read-Only memory (ROM), or synchronous FIFO memory. The memory organization is configurable as 4Kx1, 2Kx2, 1Kx4 and 512x8. The second type of memory block is located within each LBC and is referred to as a cluster memory block. Each LBC contains two cluster memory blocks that are 8192 bits in size. Similar to the channel memory blocks, the cluster memory blocks can be configured as 8Kx1, 4Kx2, 2Kx4 and 1Kx8 asynchronous or synchronous Single-Port RAM or ROM.

Cluster Memory

Each logic block cluster of the Delta39K contains two 8192-bit cluster memory blocks. *Figure 5* is a block diagram of the cluster memory block and the interface of the cluster memory block to the cluster PIM.

The output of the cluster memory block can be optionally registered to perform synchronous pipelining or to register asynchronous read and write operations. The output registers contain an asynchronous RESET which can be used in any type of sequential logic circuits (e.g., state machines).

There are four global clocks (GCLK[3:0]) and one local clock available for the input and the output registers. The local clock for the input registers is independent of the one used for the output registers. The local clock is generated in the user design in a macrocell or comes from an I/O pin.

Cluster Memory Initialization

The cluster memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the cluster memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory

The Delta39K architecture includes an embedded memory block at each crossing point of horizontal and vertical routing channels. The channel memory is a 4096-bit embedded memory block that can be configured as asynchronous or synchronous Single-Port RAM, Dual-Port RAM, ROM, or synchronous FIFO memory.

Data, address, and control inputs to the channel memory are driven from horizontal and vertical routing channels. All data and FIFO logic outputs drive dedicated tracks in the horizontal and vertical routing channels. The clocks for the channel memory block are selected from four global clocks and pin inputs from the horizontal and vertical channels. The clock muxes also include a polarity mux for each clock so that the user can choose an inverted clock.

Dual-Port (Channel Memory) Configuration

Each port has distinct address inputs, as well as separate data and control inputs that can be accessed simultaneously. The inputs to the Dual-Port memory are driven from the horizontal and vertical routing channels. The data outputs drive dedicated tracks in the routing channels. The interface to the routing is such that Port A of the Dual-Port interfaces primarily with the horizontal routing channel and Port B interfaces primarily with the vertical routing channel.

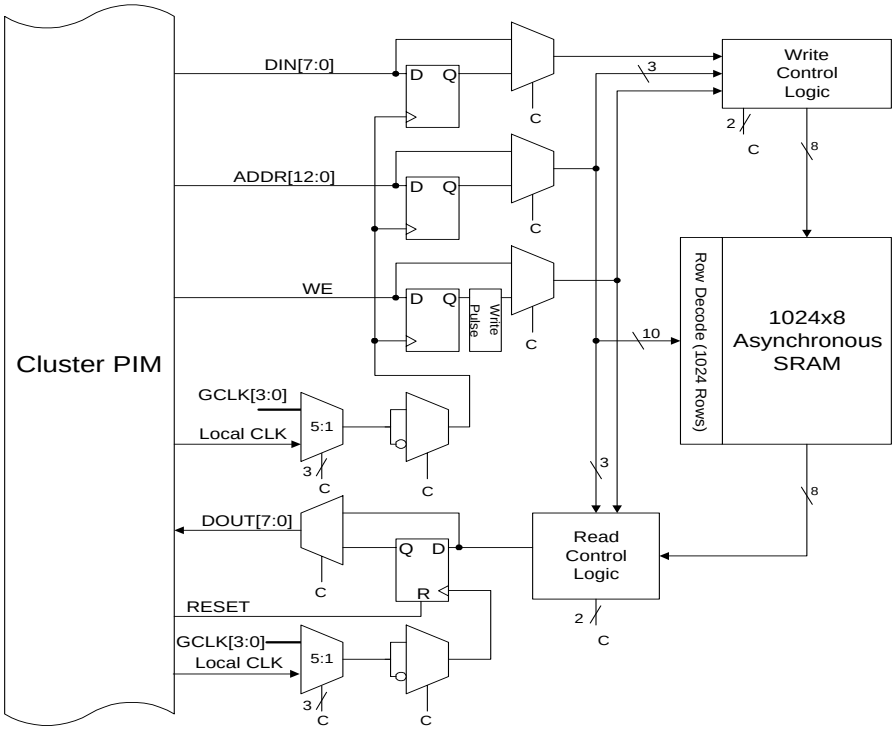


Figure 5. Block Diagram of Cluster Memory Block

The clocks for each port of the Dual-Port configuration are selected from four global clocks and two local clocks. One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs of the dual-port memory can also be registered. Clocks for the output registers are also selected from four global clocks and two local clocks. One clock polarity mux per port allows the use of true or complement polarity for input and output clocking purposes.

Arbitration

The Dual-Port configuration of the Channel Memory Block provides arbitration when both ports access the same address at the same time. Depending on the memory operation being attempted, one port always gets priority. See *Table 1* for details on which port gets priority for read and write operations. An active-LOW 'Address Match' signal is generated when an address collision occurs.

Table 1. Arbitration Result: Address Match Signal Becomes Active

Port A	Port B	Result of Arbitration	Comment
Read	Read	No arbitration required	Both ports read at the same time
Write	Read	Port A gets priority	If Port B requests first then it will read the current data. The output will then change to the newly written data by Port A
Read	Write	Port B gets priority	If Port A requests first then it will read the current data. The output will then change to the newly written data by Port B
Write	Write	Port A gets priority	Port B is blocked until Port A is finished writing

FIFO (Channel Memory) Configuration

The channel memory blocks are also configurable as synchronous FIFO RAM. In the FIFO mode of operation, the channel memory block supports all normal FIFO operations without the use of any general-purpose logic resources in the device.

The FIFO block contains all of the necessary FIFO flag logic, including the read and write address pointers. The FIFO flags include an empty/full flag ($\overline{EF}$), half-full flag ($\overline{HF}$), and programmable almost-empty/full ($\overline{PAEF}$) flag output. The FIFO configuration has the ability to perform simultaneous read and write operations using two separate clocks. These clocks may be tied together for a single operation or may run independently for asynchronous Read/Write (w.r.t. each other) applications. The data and control inputs to the FIFO block are driven from the horizontal or vertical routing channels. The data and flag outputs are driven onto dedicated routing tracks in both the horizontal and vertical routing channels. This allows the FIFO blocks to be expanded by using multiple FIFO blocks on the same horizontal or vertical routing channel without any speed penalty.

In FIFO mode, the write and read ports are controlled by separate clock and enable signals. The clocks for each port are selected from four global clocks and two local clocks.

One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs from the read port of the FIFO can also be registered. One clock polarity mux per port allows using true or complement polarity for read and write operations. The write operation is controlled by the clock and the write enable pin. The read operation is controlled by the clock and the read enable pin. The enable pins can be sourced from horizontal or vertical channels.

Channel Memory Initialization

The channel memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the channel memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory Routing Interface

Similar to LBC outputs, the channel memory blocks feature dedicated tracks in the horizontal and vertical routing channels for the data outputs and the flag outputs, as shown in *Figure 6*. This allows the channel memory blocks to be expanded easily. These dedicated lines can be routed to I/O pins as chip outputs or to other logic block clusters to be used in logic equations.

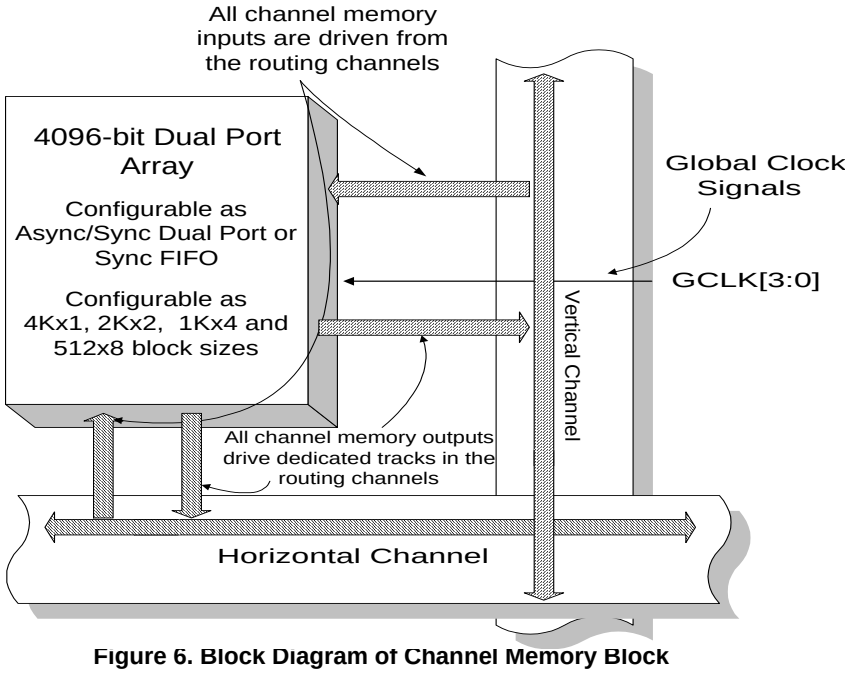


Figure 6. Block Diagram of Channel Memory Block

I/O Banks

The Delta39K interfaces the horizontal and vertical routing channels to the pins through I/O banks. There are 8 I/O banks per device as shown in *Figure 7*, and all I/Os from an I/O bank are located in the same section of a package for PCB layout convenience.

Delta39K devices support True Vertical Migration™ i.e. for each package type, Delta39K devices of different densities keep given pins in the same I/O banks. This allows for easy and simple implementation of multiple I/O standards during the design and prototyping phase, before a final density has been determined.

Each I/O bank contains several I/O cells, and each I/O cell contains an input/output register, an output enable register, programmable slew rate control and programmable bus hold control logic. Each I/O cell drives a pin output of the device; the cell also supplies an input to the device that connects to a dedicated track in the associated routing channel.

Each I/O bank can use any supported I/O standard by supplying appropriate V_{REF} and V_{CCIO} voltages. All the V_{REF} and V_{CCIO} pins in an I/O bank must be connected to the same V_{REF} and V_{CCIO} voltage respectively. This requirement restricts the number of I/O standards supported by an I/O bank at any given time.

The number of I/Os which can be used in each I/O bank depend on the type of I/O standards and the number of V_{CCIO} and GND pins being used. This restriction is derived from the electromigration limit of the V_{CCIO} and GND bussing on the chip. Please refer to the note on page 17 and the application note titled “Delta39K Family Device I/O Standards and Configurations” for details.

I/O Cell

Figure 8 is a block diagram of the Delta39K I/O cell. The I/O cell contains a three-state input buffer, an output buffer, and a register that can be configured as an input or output register. The output buffer has a slew rate control option that can be used to configure the output for a slower slew rate. The input of the device and the pin output can each be configured as registered or combinatorial; however, only one path can be configured as registered in a given design.

The output enable in an I/O cell can be selected from one of the four global control signals or from one of two Output Control Channel (OCC) signals. The output enable can be configured as always enabled or always disabled or it can be controlled by one of the remaining inputs to the mux. The selection is done via a mux that includes V_{CC} and GND as inputs

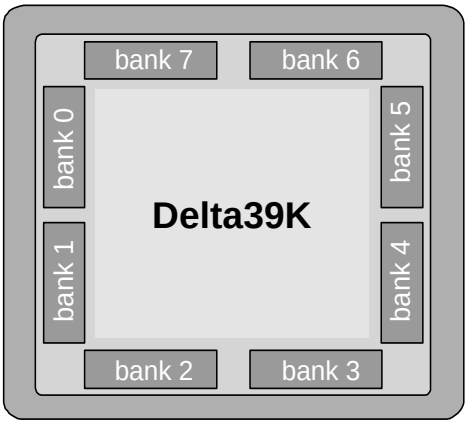


Figure 7. Delta39K I/O Bank Block Diagram

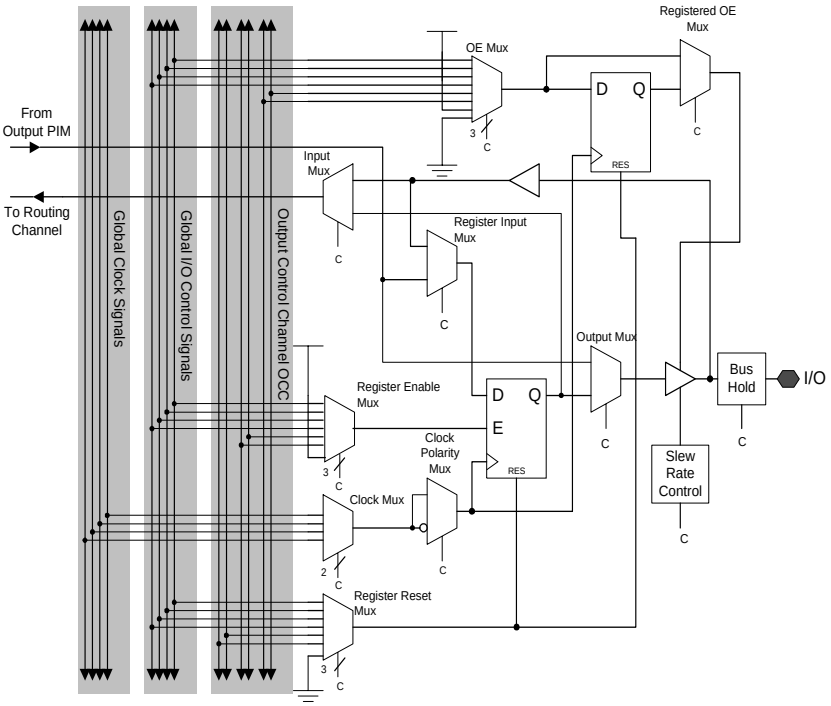


Figure 8. Block Diagram of I/O Cell

I/O Signals

There are four dedicated inputs (GCTL[3:0]) that are used as Global I/O Control Signals available to every I/O cell. These global I/O control signals may be used as output enables, register resets and register clock enables as shown in *Figure 8*. These global control signals, driven from 4 dedicated pins, can only be used as active-high signals and are available only to the I/O cells thereby implementing fast resets, register and output enables.

In addition, there are six Output Control Channel (OCC) signals available to each I/O cell. These control signals may be used as output enables, register resets and register clock enables as shown in *Figure 8*. Unlike global control signals, these OCC signal can be driven from internal logic or and I/O pin.

One of the four global clocks can be selected as the clock for the I/O cell register. The clock mux output is an input to a clock polarity mux that allows the input/output register to be clocked on either edge of the clock

Slew Rate Control

The ouput buffer has a slew rate control option. This allows the output buffer to slew at a fast rate (3 V/ns) or a slow rate (1 V/ns). All I/Os default to fast slew rate. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

I/O Standards

I/O Standard	V_{REF} (V)		V_{CCIO}	Termination Voltage (V_{TT})
	Min.	Max.		
LVTTL	N/A		3.3V	N/A
LVCMOS			3.3V	N/A
LVCMOS3			3.0V	N/A
LVCMOS2			2.5V	N/A
LVCMOS18			1.8V	N/A
3.3V PCI			3.3V	N/A
GTL+	0.9	1.1	N/A	1.5
SSTL3 I	1.3	1.7	3.3V	1.5
SSTL3 II	1.3	1.7	3.3V	1.5
SSTL2 I	1.15	1.35	2.5V	1.25
SSTL2 II	1.15	1.35	2.5V	1.25
HSTL I	0.68	0.9	1.5V	0.75
HSTL II	0.68	0.9	1.5V	0.75
HSTL III	0.68	0.9	1.5V	1.5
HSTL IV	0.68	0.9	1.5V	1.5

Programmable Bus Hold

On each I/O pin, user-programmable-bus-hold is included. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold

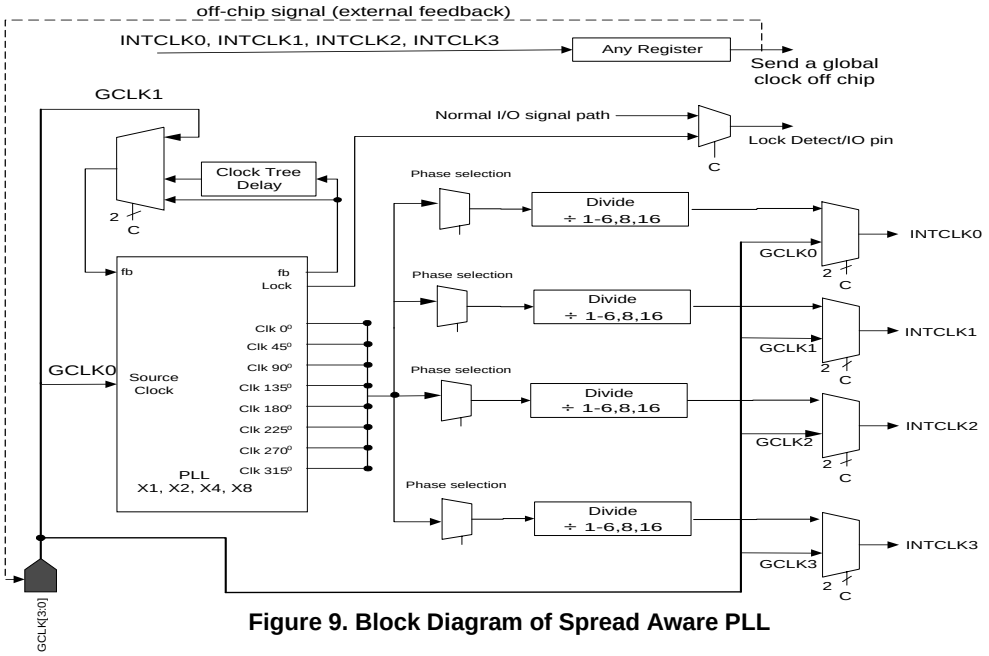


Figure 9. Block Diagram of Spread Aware PLL

maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note "Understanding Bus-Hold – A Feature of Cypress CPLDs."

Clocks

Delta39K has four dedicated clock input pins (GCLK[3:0]) to accept system clocks. One of these clocks (GCLK[0]) may be selected to drive an on-chip Phase-Locked Loop (PLL) for frequency modulation (see *Figure 9* for details).

The global clock tree for a Delta39K device can be driven by a combination of the dedicated clock pins and/or the PLL-derived clocks. The global clock tree consists of four global clocks that go to every macrocell, memory block, and I/O cell.

Clock Tree Distribution

The global clock tree performs two primary functions. First, the clock tree generates the four global clocks by multiplexing four dedicated clocks from the package pins and four PLL driven clocks. Second, the clock tree distributes the four global clocks to every cluster, channel memory, and I/O block on the die. The global clock tree is designed such that the clock skew is minimized while maintaining an acceptable clock delay.

Spread Aware™ PLL

Each device in the Delta39K family features an on-chip PLL designed using Spread Aware technology for low EMI applications. In general, PLLs are used to implement time-division-multiplex circuits to achieve higher performance with fewer device resources.

For example, a system that operates on a 32-bit data path that runs at 40 MHz can be implemented with 16-bit circuitry that runs internally at 80 MHz. PLLs can also be used to take advantage of the positioning of the internally generated clock edges to shift performance towards improved setup, hold or clock-to-out times.

There are several frequency multiply (X1, X2, X4, X8) and divide (/1, /2, /3, /4, /5, /6. /8, /16) options available to create a wide range of clock frequencies from a single clock input (GCLK[0]). For increased flexibility, there are seven phase shifting options which allow clock skew/de-skew by 45°, 90°, 135°, 180°, 225°, 270° or 315°.

The Spread Aware feature refers to the ability of the PLL to track a spread-spectrum input clock such that its spread is seen on the output clock with the PLL staying locked. The total amount of spread on the input clock should be limited to 0.6% of the fundamental frequency. Spread Aware feature is supported only with X1, X2 and X4 multiply options.

The Voltage Controlled Oscillator (VCO), the core of the Delta39K PLL is designed to operate within the frequency range of 100 MHz to 266 MHz. Hence, the multiply option combined with input (GCLK[0]) frequency should be selected such that this VCO operating frequency requirement is met. This is demonstrated in *Table 2* (columns 1, 2, and 3).

Another feature of this PLL is the ability to drive the output clock (INTCLK) off the Delta39K chip to clock other devices on the board, as shown in *Figure 9* above. This off-chip clock is half the frequency of the output clock as it has to go through a register (I/O register or a macrocell register).

Table 2. PLL Multiply and Divide Options—without External Feedback

Input Frequency (GCLK[0]) f_{PLLI} (MHz)	Valid Multiply Options		Valid Divide Options		
	Value	VCO Output Frequency (MHz)	Value	Output Frequency (INTCLK[3:0]) f_{PLLO} (MHz)	Off-chip Clock Frequency
12.5–25	8	100–200	1–6, 8, 16	6.25–200	3.12–100
25–33	8	200–266	1–6, 8, 16	12.5–266	6.25–133
	4	100–133	1–6, 8, 16	6.25–133	3.12–66
33–50	4	133–200	1–6, 8, 16	8.33–200	4.16–100
50–66	4	200–266	1–6, 8, 16	12.5–266	6.25–133
	2	100–133	1–6, 8, 16	6.25–133	3.12–66
66–100	2	133–200	1–6, 8, 16	8.3–200	4.16–100
100–133	2	200–266	1–6, 8, 16	12.5–266	6.25–133
	1	100–133	1–6, 8, 16	6.25–133	3.12–66

Table 3. PLL Multiply and Divide Options—with External Feedback

Input (GCLK) Frequency f_{PLLI} (MHz)	Valid Multiply Options		Valid Divide Options		
	Value	VCO Output Frequency (MHz)	Value	Output (INTCLK) Frequency f_{PLLO} (MHz)	Off-chip Clock Frequency
50–66	1	100–133	1	100–133	50–66
66–100	1	133–200	1	133–200	66–100
100–133	1	200–266	1	200–266	100–133

This PLL can also be used for board de-skewing purpose by driving a PLL output clock off-chip, routing it to the other devices on the board and feeding it back to the PLL's external feedback input (GCLK[1]). When this feature is used, only limited multiply, divide and phase shift options can be used.

Table 2 describes the valid multiply and divide options that can be used without an external feedback. *Table 3* describes the valid multiply & divide options that can be used with an external feedback.
Table 4 describes the valid phase shift options that can be used with or without an external feedback.

Table 5 is an example of the effect of all the available divide and phase shift options on a VCO output of 250 MHz. It also shows the effect of division on the duty cycle of the resultant clock. Note that the duty cycle is 50-50 when a VCO output is divided by an even number. Also note that the phase shift applies to the VCO output and not to the divided output.

Table 4. PLL Phase Shift Options—with and without External Feedback

Without External Feedback	With External Feedback
0°,45°, 90°, 135°, 180°, 225°, 270°, 315°	0°

The Spread Aware PLL operates as specified for Delta39KV devices (2.5V/3.3V), but not Delta39KZ devices (1.8V). For more details on the architecture and operation of this PLL please refer to the application note entitled "Delta39K PLL and Clock Tree.

Table 5. Timing of Clock Phases for all Divide Options for a VCO Output Frequency of 250 MHz

Divide Factor	Period (ns)	Duty Cycle%	0° (ns)	45° (ns)	90° (ns)	135° (ns)	180° (ns)	225° (ns)	270° (ns)	315° (ns)
1	4	40-60	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
2	8	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
3	12	33-67	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
4	16	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
5	20	40-60	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
6	24	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
8	32	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
16	64	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5

CompactPCI Hot Swap

CompactPCI Hot Swap specification allows the removal and insertion of cards into CompactPCI sockets without switching-off the bus. Delta39K CPLDs can be used as a CompactPCI host or target on these cards.

This feature is useful in telecommunication and networking applications as it allows implementation of high availability systems, where repairs and upgrades can be done without downtime.

Delta39K CPLDs are CompactPCI Hot Swap Ready per CompactPCI Hot Swap specification R1.0, with the following two exceptions:

- PCI buffers do not support the AC specifications for 5V signaling and
- The I/O cells do not provide bias voltage support
  External resistors can be used to achieve this per section 3.1.3.1 of the CompactPCI Hot Swap specification R1.0

Timing Model

One important feature of the Delta39K family is the simplicity of its timing. All combinatorial and registered/synchronous delays are worst case and system performance is static (as shown in the AC specs section) as long as data is routed through the same horizontal and vertical channels. *Figure 10* illustrates the true timing model for the 200-MHz devices. For synchronous clocking of macrocells, a delay is incurred from macrocell clock to macrocell clock of separate Logic Blocks within the same cluster, as well as separate Logic Blocks within different clusters. This is respectively shown as t_{SCS} and t_{SCS2} in *Figure 10.* For combinatorial paths, any input to any output (from corner to corner on the device), incurs a worst-case delay in the 39K100 regardless of the amount of logic or which horizontal and vertical channels are used. This is the t_{PD} shown in *Figure 10.* For synchronous systems, the input set-up time to the output macrocell register and the clock to output time are shown as the parameters t_{MCS} and t_{MCCO} shown in the *Figure 10.* These measurements are for any output and synchronous clock, regardless of the logic placement.

The Delta39K features:

- no dedicated vs. I/O pin delays
- no penalty for using 0–16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no output bypass delays

The simple timing model of the Delta39K family eliminates unexpected performance penalties.

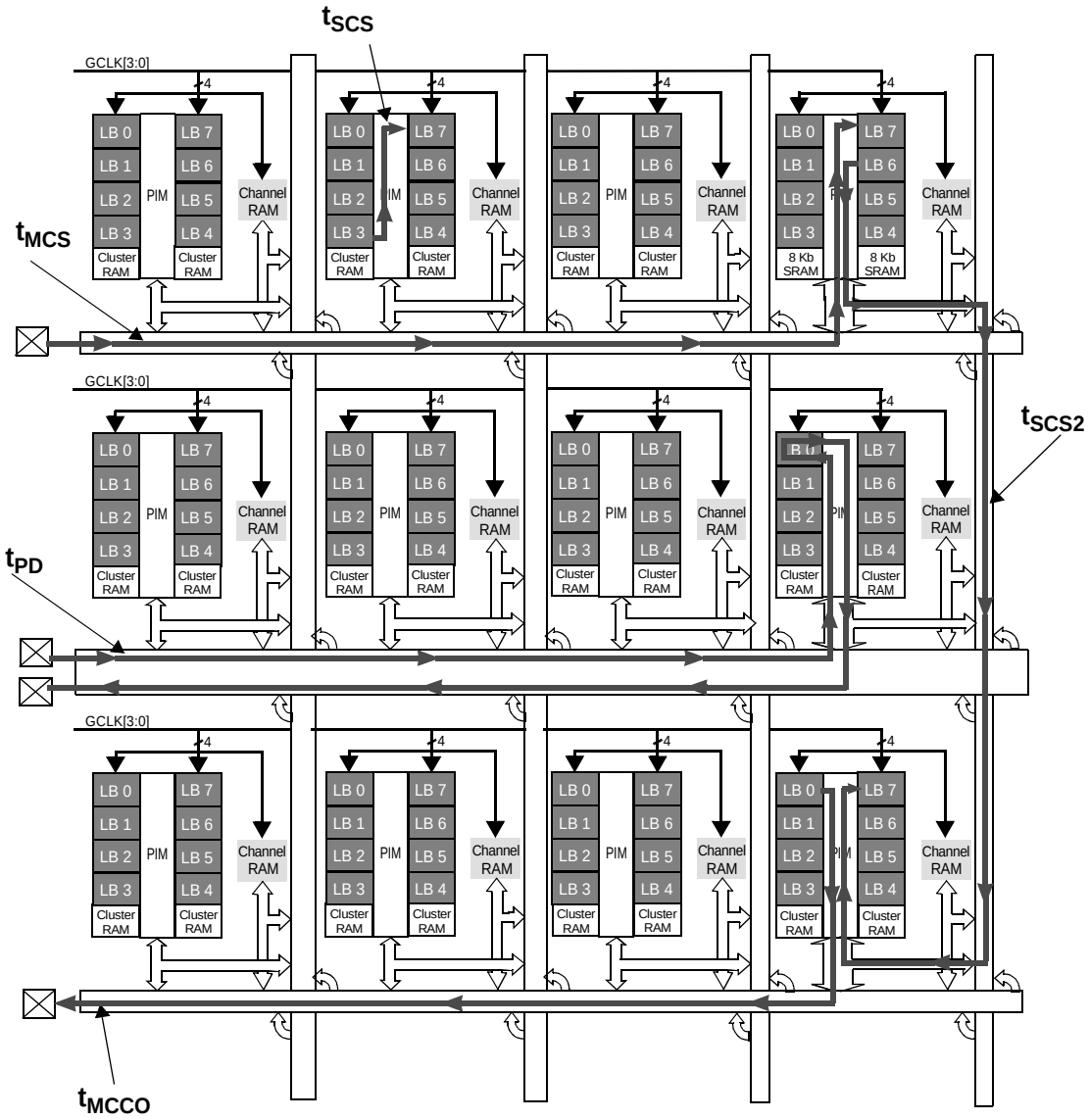


Figure 10. Timing Model for 39K100 Device

IEEE 1149.1 Compliant JTAG Operation

The Delta39K family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR operations.

Four dedicated pins are reserved on each device for use by the Test Access Port (TAP).

Boundary Scan

The Delta39K family supports Bypass, Sample/Preload, Extest, Intest, Idcode and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 11*.

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Delta39K family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Configuration

Each device of the Delta39K family is available in a volatile and a Self-Boot package. Cypress's CPLD boot EEPROM is used to store configuration data for the volatile solution and an embedded on-chip FLASH memory device is used for the Self-Boot solution.

For volatile Delta39K packages, programming is defined as the loading of a user's design into the external CPLD boot EEPROM. For Self-Boot Delta39K packages, programming is defined as the loading of a user's design into the on-chip

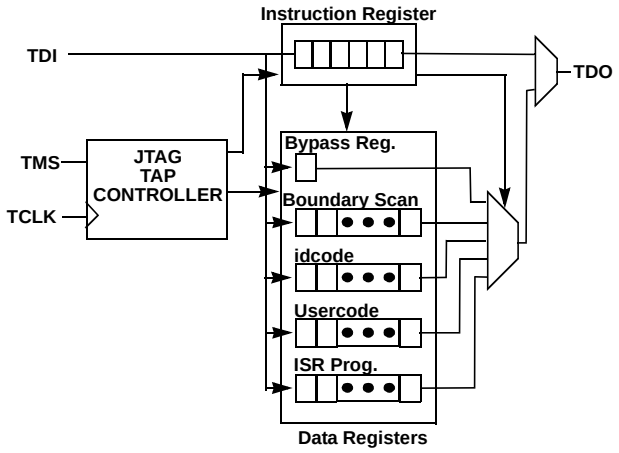


Figure 11. JTAG Interface

FLASH internal to the Delta39K package. Configuration is defined as the loading of a user's design into the Delta39K die.

Configuration can begin in two ways. It can be initiated by toggling the *Reconfig* pin from LOW to HIGH, or by issuing the appropriate IEEE std 1149.1 JTAG instruction to the Delta39K device via the JTAG interface. There are two IEEE std 1149.1 JTAG instructions that initiate configuration of the Delta39K. The *Self Config* instruction causes the Delta39K to (re)configure with data stored in the serial boot PROM or the embedded FLASH memory. The *Load Config* instruction causes the Delta39K to (re)configure according to data provided by other sources such as a PC, automatic test equipment (ATE), or an embedded micro-controller/processor via the JTAG interface. For more information on configuring Delta39K devices, refer to the application note titled "Configuring Delta39K/Quantum38K" at http://www.cypress.com.

There are two configuration options available for issuing the IEEE std 1149.1 JTAG instructions to the Delta39K. The first method is to use a PC with the C3ISR programming cable and software. With this method, the ISR pins of the Delta39K devices in the system are routed to a connector at the edge of the printed circuit board. The C3ISR programming cable is then connected between the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on the Delta39K devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish configuration, reading, verifying, and other ISR functions. For more information on the Cypress ISR interface, see the ISR Programming Kit data sheet (CY3900i).

The second configuration option for the Delta39K is to utilize the embedded controller or processor that already exists in the system. The Delta39K ISR software assists in this method by converting the device HEX file into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be configured. The embedded controller then simply directs this ISR stream to the chain of Delta39K devices to complete the desired reconfiguration or diagnostic operations. Contact your local sales office for information on availability of this option.

Programming

The on-chip FLASH device of the Delta39K Self-Boot package is programmed by issuing the appropriate IEEE std 1149.1 JTAG instruction to the internal FLASH memory via the JTAG interface. This can be done automatically using ISR/STAPL software. The configuration bits are sent from a PC through the JTAG port into the Delta39K via the C3ISR programming cable. The data is then internally passed from Delta39K to the on-chip FLASH. For more information on how to program the Delta39K through ISR/STAPL, please refer to the ISR/STAPL User Guide.

The external CPLD boot EEPROM used to store configuration data for the Delta39K volatile package is programmed through Cypress's CYDH2200E CPLD Boot PROM Programming Kit via a two-wire interface. For more information on how to program the CPLD boot EEPROM, please refer to the data sheet titled "CYDH2200E CPLD Boot PROM Programming Kit." For more information on the architecture and timing specification of the boot EEPROM, refer to the data sheet titled "CPLD Boot EEPROM."

Third-Party Programmers

Cypress support is available on a wide variety of third-party programmers. All major programmers (including BP Micro, System General, Hi-Lo) support the Delta39K family.

Development Software Support

Warp

Warp is a state-of-the-art design environment for designing with Cypress programmable logic. *Warp* utilizes a subset of IEEE 1076/1164 VHDL and IEEE 1364 as the Hardware Description Language (HDL) for design entry. *Warp* accepts VHDL or Verilog input, synthesizes and optimizes the entered design, and outputs a configuration bitstream for the desired Delta39K device. For simulation, *Warp* provides a graphical waveform simulator as well as VHDL and Verilog Timing Models.

VHDL and Verilog are open, powerful, non-proprietary Hardware Description Languages (HDLs) that are standards for behavioral design entry and simulation. HDL allows designers to learn a single language that is useful for all facets of the design process.

Third-Party Software

Cypress products are supported in a number of third-party design entry and simulation tools. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third party vendors.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Soldering Temperature.....220°C

Ambient Temperature with Power Applied..... –40°C to +85°C

Junction Temperature.....135°C

V_{CC} to Ground Potential (39KZ device)..... .. –0.5V to 2.5V

V_{CC} to Ground Potential (39KV device) .....–0.5V to 4.6V

V_{CCIO} to Ground Potential.....–0.5V to 4.6V

DC Voltage Applied to Outputs in High Z State –0.5V to 4.5V

DC Input voltage..... .....–0.5V to 4.5V

DC Current into Outputs..... ....±20 mA[7]

Static Discharge Voltage (per JEDEC EIA./ JESD22-A114A).....>2001V

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature	Junction Temperature	Output Condition	V_{CCIO}	V_{CC}	V_{CCJTAG}/ V_{CCCNFG}	V_{CCPLL}	V_{CCPRG}
Commercial	0°C to +70°C	0°C to +85°C	3.3V	3.3V ± 0.3V	3.3V ± 0.3V or 2.5V ± 0.2V (39KV)	Same as V_{CCIO}	Same as V_{CC}	3.3V ± 0.3V
			2.5V	2.5V ± 0.2V				
			1.8V	1.8V ± 0.15V				
			1.5V	1.5V ± 0.1V[6]				
Industrial	–40°C to +85°C	–40°C to +100°C	3.3V	3.3V ± 0.3V	1.8V ± 0.15V (39KZ)			
			2.5V	2.5V ± 0.2V				
			1.8V	1.8V ± 0.15V				
			1.5V	1.5V ± 0.1V[6]				

DC Characteristics

Parameter	Description	Test Conditions	V_{CCIO} = 3.3 V		V_{CCIO} = 2.5 V		V_{CCIO} = 1.8 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DRINT}	Data Retention V_{CC} Voltage (config data may be lost below this)		1.5		1.5		1.5		V
V_{DRIO}	Data Retention V_{CCIO} Voltage (config data may be lost below this)		1.2		1.2		1.2		V
I_{IX}	Input Leakage Current	$GND \le V_I \le 3.6V$	–10	10	–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CCIO}$	–10	10	–10	10	–10	10	µA
I_{OS}[8]	Output Short Circuit Current	V_{CCIO} = Max., V_{OUT} = 0.5V		–160		–160		–160	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., $V_{PIN} = V_{IL}$	+40		+30		+25		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., $V_{PIN} = V_{IH}$	–40		–30		–25		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.		+250		+200		+150	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.		–250		–200		–150	µA
I_{CC0}	Standby Current	39K30 39K50 39K100 39K165 39K200		20 20 20 20 20		20 20 20 20 20		0.3 0.3 0.6 1.25 1.25	mA

Notes:

7. DC current into outputs is 36 mA with HSTL III, 48 mA with HSTL IV and 36 mA with GTL+ (with 25Ω pull-up resistor and V_{TT} = 1.5
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation. Tested initially and after any design or process changes that may affect these parameters.

Capacitance

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{in}=V_{CCIO}$ @ f=1 MHz 25°C		10	pF
C_{CLK}	Clock Signal Capacitance	$V_{in}=V_{CCIO}$ @ f=1 MHz 25°C	5	12	pF
C_{PCI}	PCI Compliant[9] Capacitance	$V_{in}=V_{CCIO}$ @ f=1 MHz 25°C		8	pF

DC Characteristics (IO)[10]

Input/ Output Standard	V_{REF} (V)		V_{CCIO} (V)	V_{OH} (V)		V_{OL} (V)		V_{IH} (V)		V_{IL} (V)	
	Min.	Max.		@ I_{OH} =	V_{OH} (min.)	@ I_{OL} =	V_{OL} (max.)	Min.	Max.	Min.	Max.
LVTTL -2mA	N/A		3.3	–2 mA	2.4	2 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL -4mA			3.3	–4 mA	2.4	4 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL -6mA			3.3	–6 mA	2.4	6 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL -8mA			3.3	–8 mA	2.4	8 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL -12mA			3.3	–12 mA	2.4	12 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL -16mA			3.3	–16 mA	2.4	16 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVTTL -24mA			3.3	–24 mA	2.4	24 mA	0.4	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS			3.3	–0.1 mA	V_{CCIO}–0.2v	0.1 mA	0.2	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS3			3.0	–0.1 mA	V_{CCIO}–0.2v	0.1mA	0.2	2.0 V	V_{CCIO}+0.3	–0.3V	0.8V
LVCMOS2			2.5	–0.1 mA	2.1	0.1 mA	0.2	1.7 V	V_{CCIO}+0.3	–0.3V	0.7V
				–1.0 mA	2.0	1.0 mA	0.4				
				–2.0 mA	1.7	2.0 mA	0.7				
LVCMOS18			1.8	– 2 mA	V_{CCIO}–0.45v	2.0 mA	0.45	0.65V_{CCIO}	V_{CCIO}+0.3	–0.3V	0.35V_{CCIO}
3.3V PCI			3.3	–0.5 mA	0.9V_{CCIO}	1.5 mA	0.1V_{CCIO}	0.5V_{CCIO}	V_{CCIO}+0.5	–0.5V	0.3V_{CCIO}
GTL+	0.9	1.1	[11]			36mA[12]	0.6	V_{REF}+0.2			V_{REF}–0.2
SSTL3 I	1.3	1.7	3.3	–8 mA	V_{CCIO}–1.1v	8 mA	0.7	V_{REF}+0.2	V_{CCIO}+0.3	–0.3V	V_{REF}–0.2
SSTL3 II	1.3	1.7	3.3	–16 mA	V_{CCIO}–0.9v	16 mA	0.5	V_{REF}+0.2	V_{CCIO}+0.3	–0.3V	V_{REF}–0.2
SSTL2 I	1.15	1.35	2.5	–7.6 mA	V_{CCIO}–0.62v	7.6 mA	0.54	V_{REF}+.18	V_{CCIO}+0.3	–0.3V	V_{REF}–0.18
SSTL2 II	1.15	1.35	2.5	–15.2 mA	V_{CCIO}–0.43v	15.2 mA	0.35	V_{REF}+.18	V_{CCIO}+0.3	–0.3V	V_{REF}–0.18
HSTL I	0.68	0.9	1.5	–8 mA	V_{CCIO}–0.4v	8 mA	0.4	V_{REF}+.10	V_{CCIO}+0.3	–0.3V	V_{REF}–0.1
HSTL II	0.68	0.9	1.5	–16 mA	V_{CCIO}–0.4v	16 mA	0.4	V_{REF}+0.1	V_{CCIO}+0.3	–0.3V	V_{REF}–0.1
HSTL III	0.68	0.9	1.5	–8 mA	V_{CCIO}–0.4v	24 mA	0.4	V_{REF}+0.1	V_{CCIO}+0.3	–0.3V	V_{REF}–0.1
HSTL IV	0.68	0.9	1.5	–8 mA	V_{CCIO}–0.4v	48 mA	0.4	V_{REF}+0.1	V_{CCIO}+0.3	–0.3V	V_{REF}–0.1

Notes:

9. PCI spec (rev 2.2) requires the IDSEL pin to have capacitance less than or equal to 8 pF. Document titled “Delta39K Pin Tables” identifies all the I/O pins, in a given package, which can be used as IDSEL in a PCI design. All other I/O pins meet the PCI requirement of capacitance less than or equal to 10 pf.
10. The number of I/Os which can be used in each I/O bank depends on the type of I/O standards and the number of V_{CCIO} and GND pins being used. Please refer to the application note titled “Delta39K and Quantum38K I/O Standards and Configurations” for details.
    - The source current limit per I/O bank per Vccio pin is 165 mA
    - The sink current limit per I/O bank per GND pin is 230 mA
11. See “Power-up Sequence Requirements” below for V_{CCIO} requirement.
12. 25Ω resistor terminated to termination voltage of 1.5V.

Configuration Parameters

Parameter	Description	Min.	Unit
$t_{RECONFIG}$	*Reconfig* pin LOW time before it goes HIGH	200	ns

Power-up Sequence Requirements

- Upon power-up, all the outputs remain three-stated until all the V_{CC} pins have powered-up to the nominal voltage and the part has completed configuration.
- The part will not start configuration until V_{CC}, V_{CCIO}, V_{CCJTAG}, V_{CCCNFG}, V_{CCPLL} and V_{CCPRG} have reached nominal voltage.
- V_{CC} pins can be powered up in any order. This includes V_{CC}, V_{CCIO}, V_{CCJTAG}, V_{CCCNFG}, V_{CCPLL} and V_{CCPRG}.
- All V_{CCIO}s on a bank should be tied to the same potential and powered up together.
- All V_{CCIO}s (even the unused banks) need to be powered up to at least 1.5V before configuration has completed.
- Maximum ramp time for all V_{CC}s should be 0V to nominal voltage in 100 ms.

Switching Characteristics - Parameter Descriptions Over the Operating Range [13]

Parameter	Description
Combinatorial Mode Parameters	
t_{PD}	Delay from any pin input, through any cluster on the channel associated with that pin input, to any pin output on the horizontal or vertical channel associated with that cluster
t_{EA}	Global control to output enable
t_{ER}	Global control to output disable
t_{PRR}	Asynchronous macrocell RESET or PRESET recovery time from any pin input on the horizontal or vertical channel associated with the cluster the macrocell is in
t_{PRO}	Asynchronous macrocell RESET or PRESET from any pin input on the horizontal or vertical channel associated with the cluster that the macrocell is in to any pin output on those same channels
t_{PRW}	Asynchronous macrocell RESET or PRESET minimum pulse width, from any pin input to a macrocell in the farthest cluster on the horizontal or vertical channel the pin is associated with
Synchronous Clocking Parameters	
t_{MCS}	Set-up time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCH}	Hold time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock
t_{MCCO}	Global clock to output of any macrocell to any output pin on the horizontal or vertical channel associated with the cluster that macrocell is in
t_{IOS}	Set-up time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOH}	Hold time of any input pin to the I/O cell register associated with that pin, relative to a global clock
t_{IOCO}	Clock to output of an I/O cell register to the output pin associated with that register
t_{SCS}	Macrocell clock to macrocell clock through array logic within the same cluster
t_{SCS2}	Macrocell clock to macrocell clock through array logic in different clusters on the same channel
t_{ICS}	I/O register clock to any macrocell clock in a cluster on the channel the I/O register is associated with
t_{OCS}	Macrocell clock to any I/O register clock on the horizontal or vertical channel associated with the cluster that the macrocell is in
t_{CHZ}	Clock to output disable (high-impedance)
t_{CLZ}	Clock to output enable (low-impedance)
f_{MAX}	Maximum frequency with internal feedback—within the same cluster
f_{MAX2}	Maximum frequency with internal feedback—within different clusters at the opposite ends of a horizontal or vertical channel
Product Term Clock	
t_{MCSPT}	Set-up time for macrocell used as input register, from input to product term clock
t_{MCHPT}	Hold time of macrocell used as an input register
t_{MCCOPT}	Product term clock to output delay from input pin
t_{SCS2PT}	Register to register delay through array logic in different clusters on the same channel using a product term clock
Channel Interconnect Parameters	
t_{CHSW}	Adder for a signal to switch from a horizontal to vertical channel and vice-versa
t_{CL2CL}	Cluster to Cluster delay adder (through channels and channel PIM)

Note:
13. Add t_{CHSW} to signals making a horizontal to vertical channel switch or vice-versa.

Switching Characteristics - Parameter Descriptions Over the Operating Range [13] (continued)

Parameter	Description
Miscellaneous Delays	
t_{CPLD}	Delay from the input of a cluster PIM, through a macrocell in the cluster, back to a cluster PIM input. This parameter can be added to the t_{PD} and t_{SCS} parameters for each extra pass through the AND/OR array required by a given signal path
t_{MCCD}	Adder for carry chain logic per macrocell
t_{IOD}	Delay from the input of the output buffer to the I/O pin
t_{IOIN}	Delay from the I/O pin to the input of the channel buffer
t_{CKIN}	Delay from the clock pin to the input of the clock driver
$t_{IOREGPIN}$	Delay from the I/O pin to the input of the I/O register
PLL Parameters	
t_{MCCJ}	Maximum cycle to cycle jitter time
t_{DWSA}	PLL zero phase delay with clock tree deskewed
t_{DWOSA}	PLL zero phase delay without clock tree deskewed
t_{LOCK}	Lock time for the PLL
f_{PLLO}	Output frequency of the PLL
f_{PLLI}	Input frequency of the PLL
JTAG Parameters	
t_{JCKH}	TCLK HIGH time
t_{JCKL}	TCLK LOW time
t_{JCP}	TCLK clock period
t_{JSU}	JTAG port setup time (TDI/TMS inputs)
t_{JH}	JTAG port hold time (TDI/TMS inputs)
t_{JCO}	JTAG port clock to output time (TDO)
t_{JXZ}	JTAG port valid output to high impedance (TDO)
t_{JZX}	JTAG port high impedance to valid output (TDO)

Cluster Memory Timing Parameter Descriptions Over the Operating Range

Parameter	Description
Asynchronous Mode Parameters	
t_{CLMAA}	Cluster memory access time. Delay from address change to read data out
t_{CLMPWE}	Write Enable pulse width
t_{CLMSA}	Address set-up to the beginning of Write Enable with both signals from the same I/O block
t_{CLMHA}	Address hold after the end of Write Enable with both signals from the same I/O block
t_{CLMSD}	Data set-up to the end of Write Enable
t_{CLMHD}	Data hold after the end of Write Enable
Synchronous Mode Parameters	
$t_{CLMCYC1}$	Clock cycle time for flow through read and write operations (from macrocell register through cluster memory back to a macrocell register in the same cluster)
$t_{CLMCYC2}$	Clock cycle time for pipelined read and write operations (from cluster memory input register through the memory to cluster memory output register)
t_{CLMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock
t_{CLMH}	Address, data, and WE hold time of pin inputs, relative to a global clock
t_{CLMDV1}	Global clock to data valid on output pins for flow through data
t_{CLMDV2}	Global clock to data valid on output pins for pipelined data
$t_{CLMMACS1}$	Cluster memory input clock to macrocell clock in the same cluster
$t_{CLMMACS2}$	Cluster memory output clock to macrocell clock in the same cluster
$t_{MACCLMS1}$	Macrocell clock to cluster memory input clock in the same cluster
$t_{MACCLMS2}$	Macrocell clock to cluster memory output clock in the same cluster
Internal Parameters	
$t_{CLMCLAA}$	Asynchronous cluster memory access time from input of cluster memory to output of cluster memory

Channel Memory Timing Parameter Descriptions Over the Operating Range

Parameter	Description
Dual Port Asynchronous Mode Parameters	
t_{CHMAA}	Channel memory access time. Delay from address change to read data out
t_{CHMPWE}	Write enable pulse width
t_{CHMSA}	Address set-up to the beginning of write enable with both signals from the same I/O block
t_{CHMHA}	Address hold after the end of write enable with both signals from the same I/O block
t_{CHMSD}	Data set-up to the end of write enable
t_{CHMHD}	Data hold after the end of write enable
t_{CHMBA}	Channel memory asynchronous dual port address match (busy access time)
Dual Port Synchronous Mode Parameters	
$t_{CHMCYC1}$	Clock cycle time for flow through read and write operations (from macrocell register through channel memory back to a macrocell register in the same cluster)
$t_{CHMCYC2}$	Clock cycle time for pipelined read and write operations (from channel memory input register through the memory to channel memory output register)
t_{CHMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock
t_{CHMH}	Address, data, and WE hold time of pin inputs, relative to a global clock
t_{CHMDV1}	Global clock to data valid on output pins for flow through data
t_{CHMDV2}	Global clock to data valid on output pins for pipelined data.
t_{CHMBDV}	Channel memory synchronous dual-port address match (busy, clock to data valid)
$t_{CHMMACS1}$	Channel memory input clock to macrocell clock in the same cluster
$t_{CHMMACS2}$	Channel memory output clock to macrocell clock in the same cluster
$t_{MACCHMS1}$	Macrocell clock to channel memory input clock in the same cluster
$t_{MACCHMS2}$	Macrocell clock to channel memory output clock in the same cluster
Synchronous FIFO Data Parameters	
t_{CHMCLK}	Read and write minimum clock cycle time
t_{CHMFS}	Data, read enable, and write enable set-up time relative to pin inputs
t_{CHMFH}	Data, read enable, and write enable hold time relative to pin inputs
$t_{CHMFRDV}$	Data access time to output pins from rising edge of read clock (read clock to data valid)
$t_{CHMMACS}$	Channel memory FIFO read clock to macrocell clock for read data
$t_{MACCHMS}$	Macrocell clock to channel memory FIFO write clock for write data
Synchronous FIFO Flag Parameters	
t_{CHMFO}	Read or write clock to respective flag output at output pins
$t_{CHMMACF}$	Read or write clock to macrocell clock with FIFO flag
t_{CHMFRS}	Master Reset Pulse Width
$t_{CHMFRSR}$	Master Reset Recovery Time
$t_{CHMFRSF}$	Master Reset to Flag and Data Output Time
$t_{CHMSKEW1}$	Read/Write Clock Skew Time for Full Flag
$t_{CHMSKEW2}$	Read/Write Clock Skew Time for Empty Flag
$t_{CHMSKEW3}$	Read/Write Clock Skew Time for Boundary Flags
Internal Parameters	
$t_{CHMCHAA}$	Asynchronous channel memory access time from input of channel memory to output of channel memory

Switching Characteristics - Parameter Values Over the Operating Range

Parameter	233		200		181		167		154		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters															
t_{PD}		7.2		7.5		8.5		8.5		9.0		10		15	ns
t_{EA}		4.5		5.0		5.6		6.5		7.5		9.0		10	ns
t_{ER}		4.5		5.0		5.3		6.5		7.5		9.0		10	ns
t_{PRR}	6.0		6.0		6.0		6.0		7.0		8.0		10		ns
t_{PRO}	9.5		10		10.5		11		12		13		15		ns
t_{PRW}	3.3		3.6		4.0		4.5		5.0		6.0		7.0		ns
Synchronous Clocking Parameters															
t_{MCS}	2.7		3.0		3.5		3.5		4.0		5.0		6.0		ns
t_{MCH}	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{MCCO}		5.8		6.0		7.0		7.5		8.5		10		12	ns
t_{IOS}	1.0		1.0		1.2		1.4		1.7		2.0		2.5		ns
t_{IOH}	0.9		1.0		1.2		1.4		1.7		2.0		2.5		ns
t_{IOCO}		3.8		4.0		4.5		5.0		6.0		7.0		8.0	ns
t_{SCS}	3.4		3.5		3.6		3.7		3.9		6.4		9.6		ns
t_{SCS2}	4.3		4.5		5.5		5.7		6.2		8.0		12		ns
t_{ICS}	4.5		5.0		5.5		6.0		6.5		8.0		12		ns
t_{OCS}	4.5		5.0		5.5		6.0		6.5		8.0		12		ns
t_{CHZ}		3.5		3.5		3.8		4.0		4.4		6.0		7.0	ns
t_{CLZ}	2.0		2.0		2.0		2.0		2.0		2.0		2.0		ns
f_{MAX}		294		286		278		270		256		156		104	MHz
f_{MAX2}		233		222		181		167		154		125		83	MHz
Product Term Clocking Parameters															
t_{MCSPT}	2.7		3.0		3.3		3.5		4.0		5.0		6.0		ns
t_{MCHPT}	0.9		1.0		1.4		1.4		1.7		2.0		2.5		ns
t_{MCCOPT}		7.5		8.0		8.8		9.0		10.0		11.0		15.0	ns
t_{SCS2PT}	6.0		6.5		7.2		7.5		9.0		10.0		15.0		ns
Channel Interconnect Parameters															
t_{CHSW}		0.9		1.0		1.2		1.2		1.4		1.7		2.0	ns
t_{CL2CL}		1.8		2.0		2.3		2.4		2.6		2.8		3.0	ns
Miscellaneous Parameters															
t_{CPLD}		2.8		3.0		3.3		3.5		3.8		4.0		5.0	ns
t_{MCCD}		0.22		0.25		0.28		0.30		0.32		0.35		0.38	ns
PLL Parameters															
t_{MCCJ}		0.5		0.50		0.50		0.55		0.58		0.60		0.65	ns
t_{DWSA}		±350		±350		±350		±390		±400		±420		±460	ps
t_{DWOSA}		±350		±350		±350		±390		±400		±420		±460	ps
t_{LOCK}		3.0		3.0		3.0		3.0		3.0		3.0		3.0	ms

Switching Characteristics - Parameter Values Over the Operating Range (continued)

Parameter	233		200		181		167		154		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{PLLO}[14]	6.2	266	6.2	266	6.2	266	6.2	266	6.2	266	6.2	200	6.2	200	MHz
f_{PLLI}[14]	12.5	133	12.5	133	12.5	133	12.5	133	12.5	133	12.5	100	12.5	100	MHz
JTAG Parameters															
t_{JCKH}	25		25		25		25		25		25		25		ns
t_{JCKL}	25		25		25		25		25		25		25		ns
t_{JCP}	50		50		50		50		50		50		50		ns
t_{JSU}	10		10		10		10		10		10		10		ns
t_{JH}	10		10		10		10		10		10		10		ns
t_{JCO}		20		20		20		20		20		20		20	ns
t_{JXZ}		20		20		20		20		20		20		20	ns
t_{JZX}		20		20		20		20		20		20		20	ns

Note:
14. Refer to page 11 and the application note titled “Delta39K PLL and Clock Tree” for details on the PLL operation & specification

Input & Output Standard Timing Delay Adjustments

All the timing specifications in this data sheet are specified based on LVCMOS compliant inputs and outputs (fast slew rates).[15] Apply following adjustments if the inputs and outputs are configured to operate at other standards.

Input/Output Standard	Output Delay Adjustments			Input Delay Adjustments		
	t_{IOD}	t_{EA}	t_{ER}	t_{IOIN}	t_{CKIN}	$t_{IOREGPIN}$
LVTTL – 2 mA	3.5	0	0	0	0	0
LVTTL – 4 mA	1.8	0	0	0	0	0
LVTTL – 6 mA	1.8	0	0	0	0	0
LVTTL – 8 mA	1.2	0	0	0	0	0
LVTTL – 12 mA	0.6	0	0	0	0	0
LVTTL – 16 mA	0.2	0	0	0	0	0
LVTTL – 24 mA	0.0	0	0	0	0	0
LVCMOS	0.0	0	0	0	0	0
LVCMOS3	0.2	0.05	0	0.1	0.1	0.2
LVCMOS2	0.3	0.1	0	0.2	0.2	0.4
LVCMOS18	1.6	0.7	0.1	0.5	0.4	0.3
3.3V PCI	-0.2	0	0	0	0	0
GTL+	0.1[16]	0.6[16]	0.9[16]	0.5	0.4	0.2
SSTL3 I	–0.2	0.3	0.1	0.5	0.3	0.3
SSTL3 II	–0.5	0.2	0	0.5	0.3	0.3
SSTL2 I	–0.2	0.4	0	0.9	0.5	0.6
SSTL2 II	–0.4	0.2	0	0.9	0.5	0.6
HSTL I	0.85	0.9	0.5	0.5	0.5	0.3
HSTL II	0.55	0.8	0.5	0.5	0.5	0.3
HSTL III	0.6	0.5	0.1	0.5	0.5	0.3
HSTL IV	0.5	0.6	0	0.5	0.5	0.3

Notes:

15. For “slow slew rate” output delay adjustments, refer to *Warp* software’s static timing analyzer results.
16. These delays are based on falling edge output. The rising edge delay depends on the size of pull-up resistor and termination voltage.

Cluster Memory Timing Parameter Values Over the Operating Range

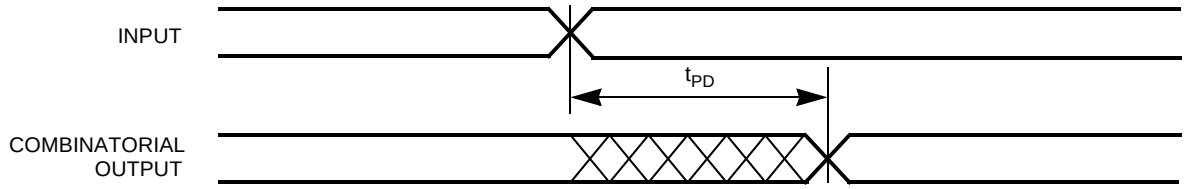
Parameter	233		200		181		167		154		125		83		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Asynchronous Mode Parameters															
t_{CLMAA}		10.2		11		12		13		15		17		20	ns
t_{CLMPWE}	5.5		6		6.5		7		8		10		12		ns
t_{CLMSA}	1.8		2.0		2.2		2.5		2.8		3.2		4.0		ns
t_{CLMHA}	0.9		1.0		1.1		1.2		1.5		1.8		2.0		ns
t_{CLMSD}	5.5		6.0		6.5		7.0		8.0		10		12		ns
t_{CLMHD}	0.4		0.5		0.6		0.7		0.8		0.9		1.0		ns
Synchronous Mode Parameters															
$t_{CLMCYC1}$	9.5		10		10.5		11		13		15		20		ns
$t_{CLMCYC2}$	5.0		5.0		5.5		6.0		7.0		8.0		10.0		ns
t_{CLMS}	2.8		3.0		3.8		3.5		3.8		4.0		5.0		ns
t_{CLMH}	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{CLMDV1}		10		11		12		13		15		17		20	ns
t_{CLMDV2}		7.0		7.5		8.0		8.5		9.0		10		15	ns
$t_{CLMMACS1}$	7.7		8.0		8.5		9.0		10		12		15		ns
$t_{CLMMACS2}$	4.5		5.0		5.5		6.0		7.0		8.0		10		ns
$t_{MACCLMS1}$	3.6		4.0		4.4		4.8		5.5		6.6		8.0		ns
$t_{MACCLMS2}$	6.0		6.5		7.0		7.5		8.5		10		12		ns
Internal Parameters															
$t_{CLMCLAA}$	6		6		6.5		7		8		10		12		ns

Channel Memory Timing Parameter Values

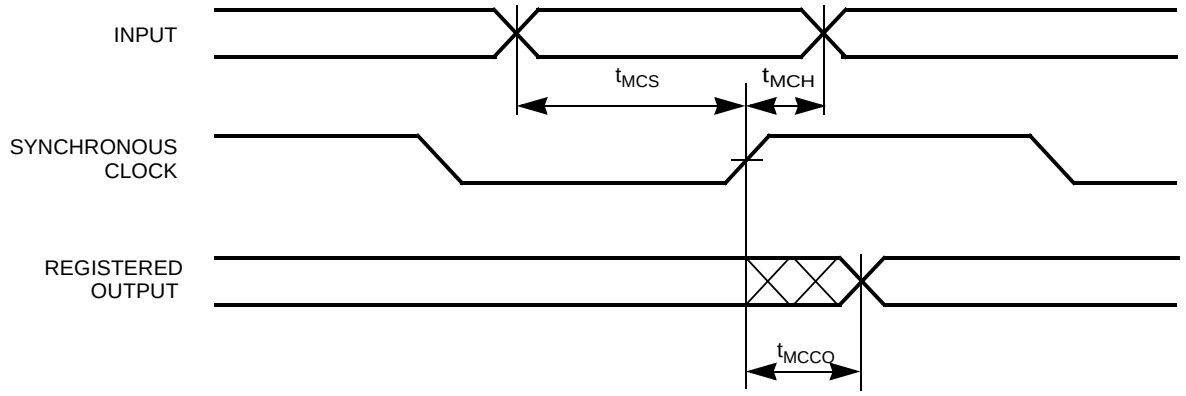
Parameter	233		200		181		167		154		125		83		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dual-Port Asynchronous Mode Parameters															
t_{CHMAA}		10		11		12		13		15		17		20	ns
t_{CHMPWE}	5.5		6.0		6.5		7.0		8.0		10		12		ns
t_{CHMSA}	1.8		2.0		2.2		2.5		2.8		3.2		4.0		ns
t_{CHMHA}	0.9		1.0		1.1		1.2		1.5		1.8		2.0		ns
t_{CHMSD}	5.5		6.0		6.5		7.0		8.0		10		12		ns
t_{CHMHD}	0.4		0.5		0.6		0.7		0.8		0.9		1.0		ns
t_{CHMBA}		8.5		9.0		10.0		11.0		12.0		14.0		16.0	ns
Dual-Port Synchronous Mode Parameters															
$t_{CHMCYC1}$	9.5		10		10		11		13		15		20		ns
$t_{CHMCYC2}$	4.8		5.0		5.4		5.8		6.2		7.4		10.6		ns
t_{CHMS}	3.0		3.3		3.9		4.0		4.5		5.0		6.0		ns
t_{CHMH}	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{CHMDV1}		10		11		12		13		15		17		20	ns
t_{CHMDV2}		7.0		7.5		8.0		8.5		9.0		10		15	ns
t_{CHMBDV}		8.5		9.0		10.0		11.0		12.0		14.0		16.0	ns
$t_{CHMMACS1}$	8.5		9.0		10.0		11.0		12.0		14.0		16.0		ns
$t_{CHMMACS2}$	4.8		5.0		5.5		6.0		7.0		8.0		10		ns
$t_{MACCHMS1}$	4.6		5.0		5.4		5.8		6.5		7.6		9.0		ns
$t_{MACCHMS2}$	7.3		7.3		7.7		8.0		9.0		10.0		13.0		ns
Synchronous FIFO Data Parameters															
t_{CHMCLK}	4.8		5.0		5.4		5.8		6.2		7.4		10.6		ns
t_{CHMFS}	3.7		4.0		4.3		4.5		5.0		6.0		7.0		ns
t_{CHMFH}	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{CHMFRDV}$		6.5		7.0		7.5		8.0		9.0		10.0		13.0	
$t_{CHMMACS}$	4.6		5.0		5.4		5.8		6.2		7.4		10.6		ns
$t_{MACCHMS}$	4.7		5.0		5.4		5.8		6.2		7.4		10.6		ns
Synchronous FIFO Flag Parameters															
t_{CHMFO}	10.5		11		11.5		12		13		15		20		ns
$t_{CHMMACF}$	8.5		9		9.5		10		11		13		17		ns
t_{CHMFRS}	4.5		5.0		5.5		6.0		7.0		8.0		10		ns
$t_{CHMFRSR}$		3.6		4.0		4.4		4.8		5.5		6.6		8.0	ns
$t_{CHMFRSF}$		9.5		10.0		11.0		12.0		13.0		15.0		18.0	ns
$t_{CHMSKEW1}$		1.8		2.0		2.2		2.4		2.6		3.2		4.0	ns
$t_{CHMSKEW2}$		1.8		2.0		2.2		2.4		2.6		3.2		4.0	ns
$t_{CHMSKEW3}$		4.6		5.0		5.4		5.8		6.2		7.4		10.6	ns
Internal Parameters															
$t_{CHMCHAA}$	6.5		7.0		7.5		8.0		9.0		10.0		13.0		ns

Switching Waveforms

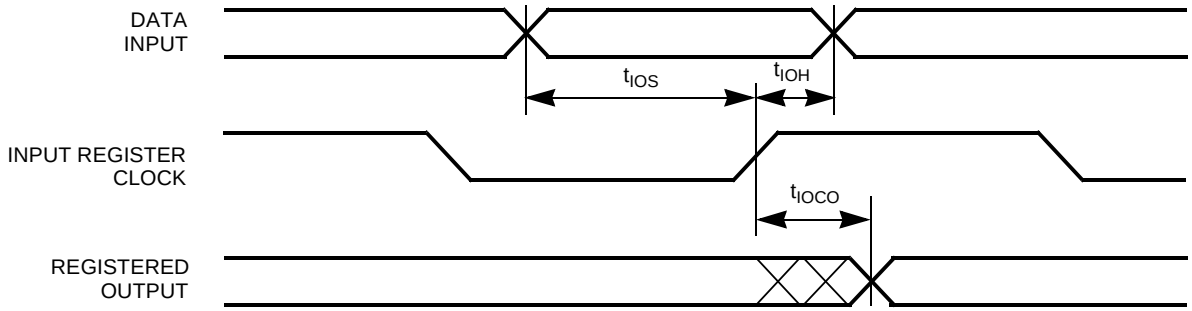
Combinatorial Output



Registered Output with Synchronous Clocking (Macrocell)

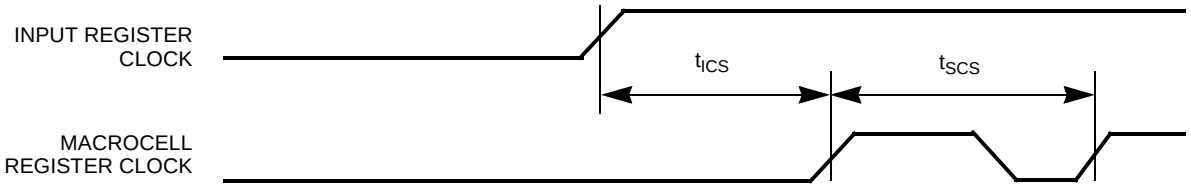


Registered Input in I/O Cell

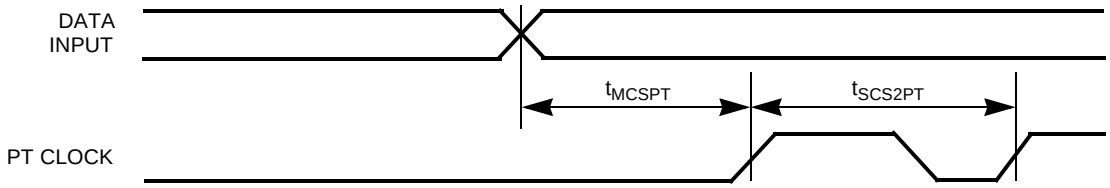


Switching Waveforms (continued)

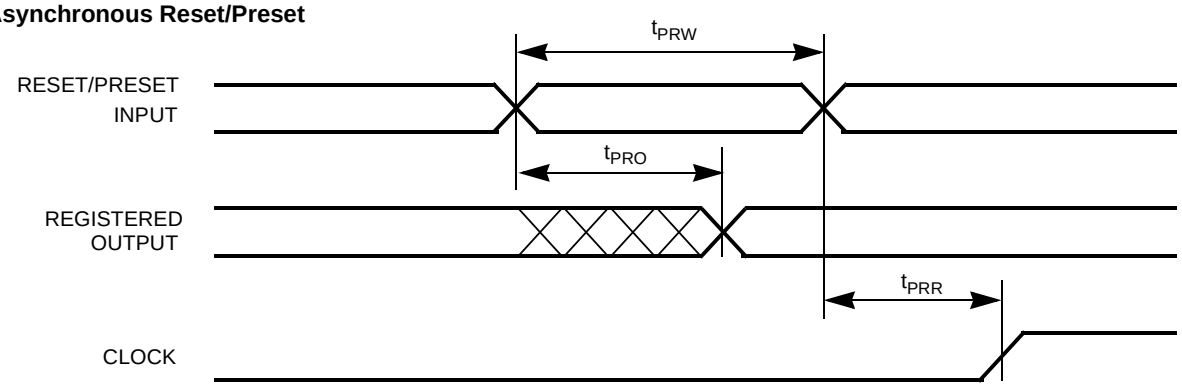
Clock to Clock



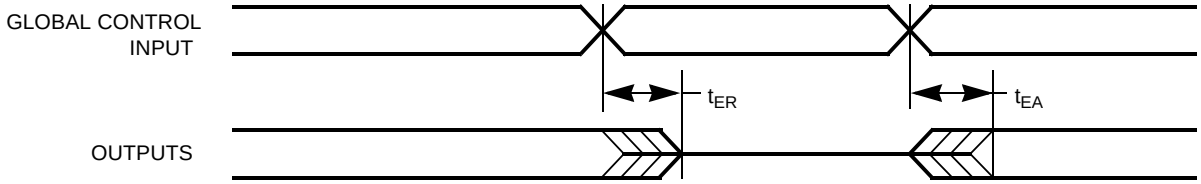
PT Clock to PT Clock



Asynchronous Reset/Preset

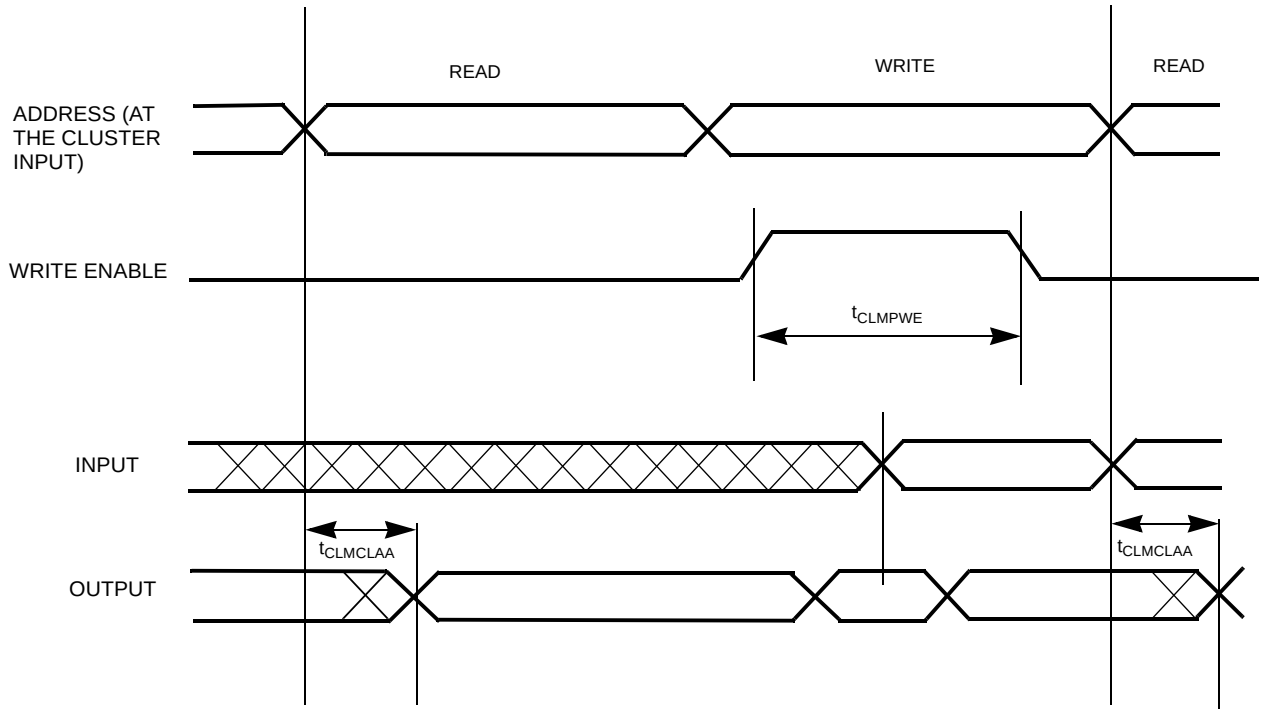


Output Enable/Disable

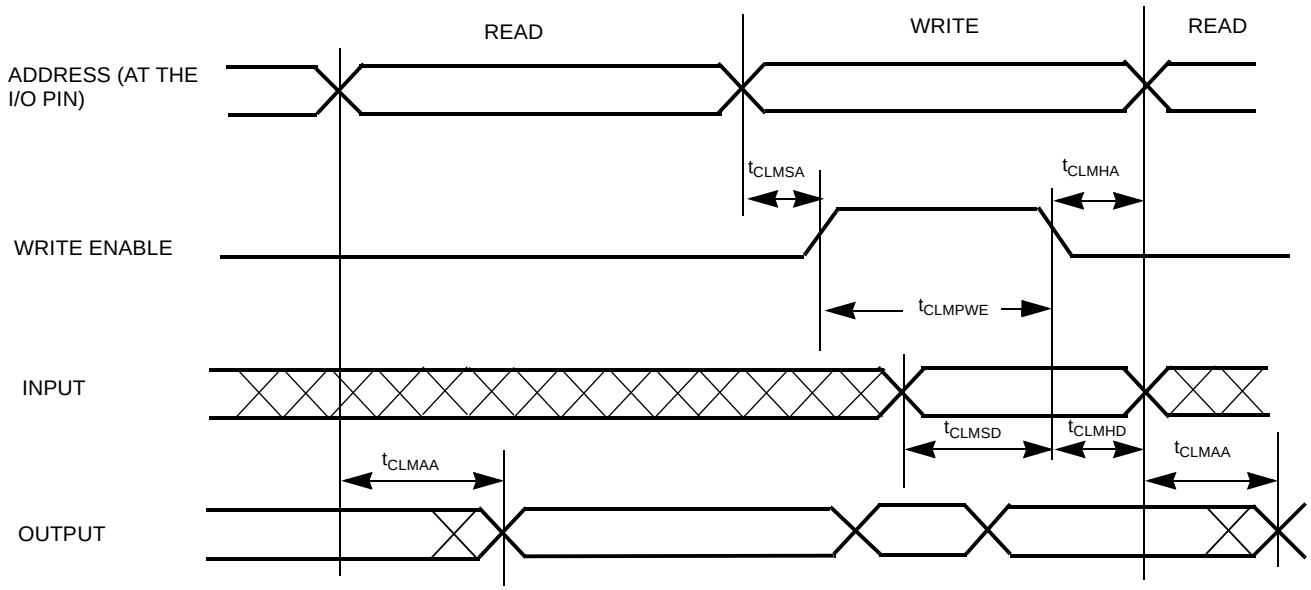


Switching Waveforms (continued)

Cluster Memory Asynchronous Timing

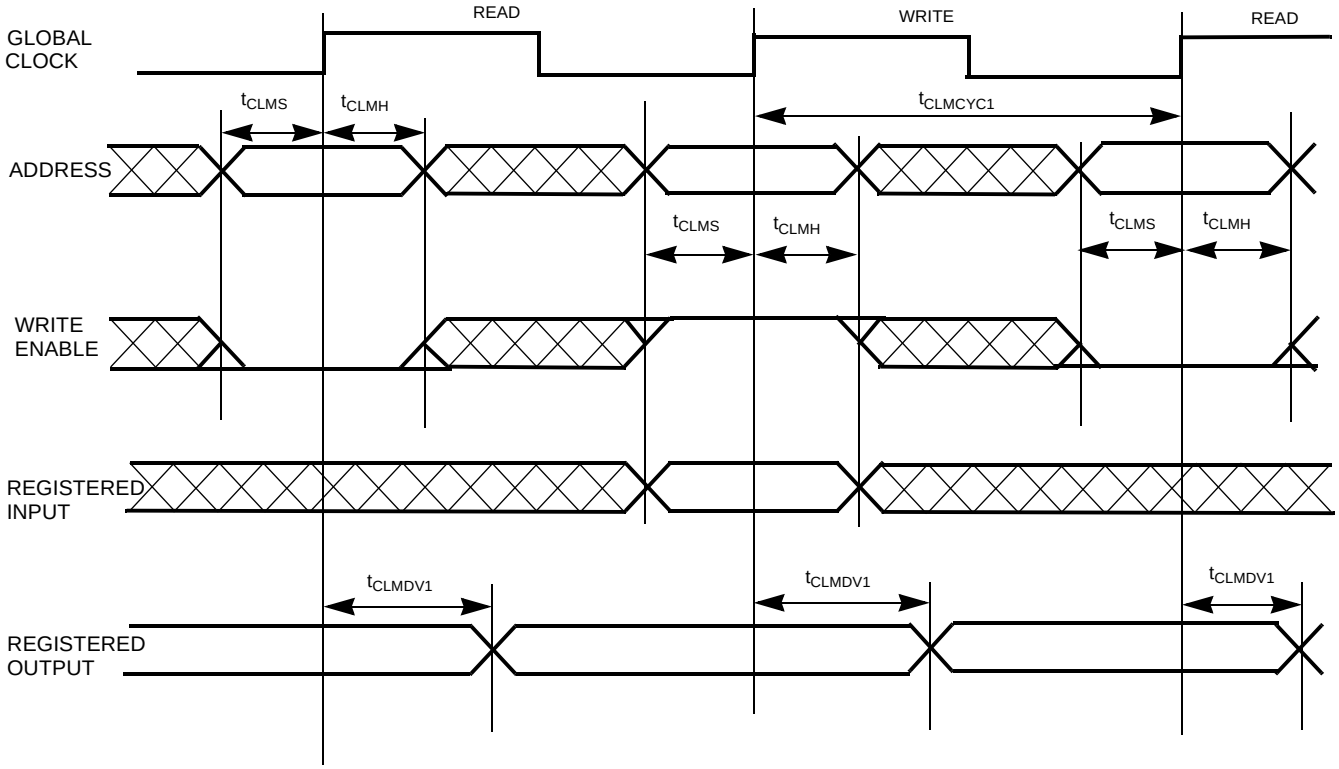


Cluster Memory Asynchronous Timing 2

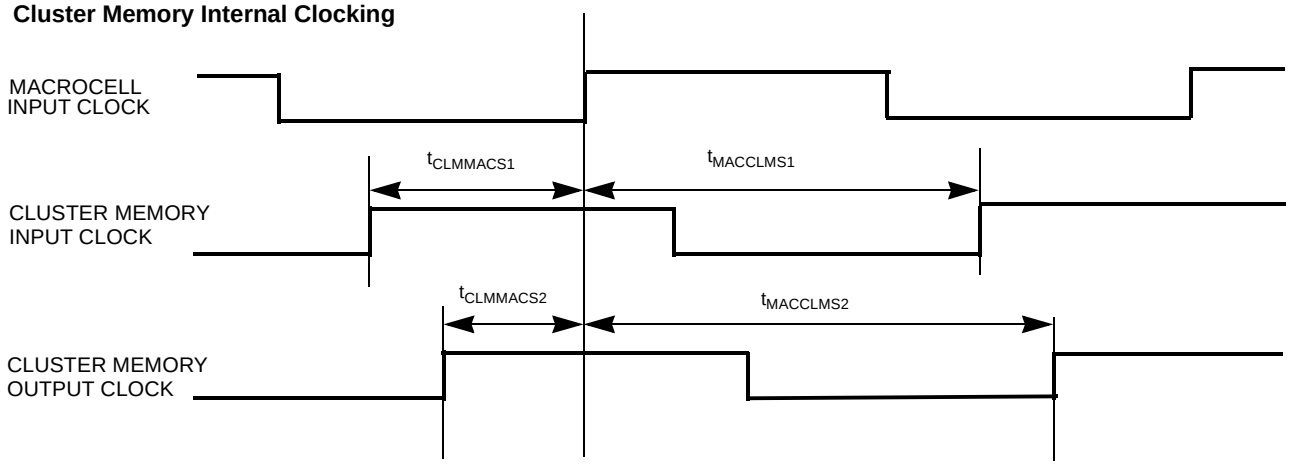


Switching Waveforms (continued)

Cluster Memory Synchronous Flow Through Timing

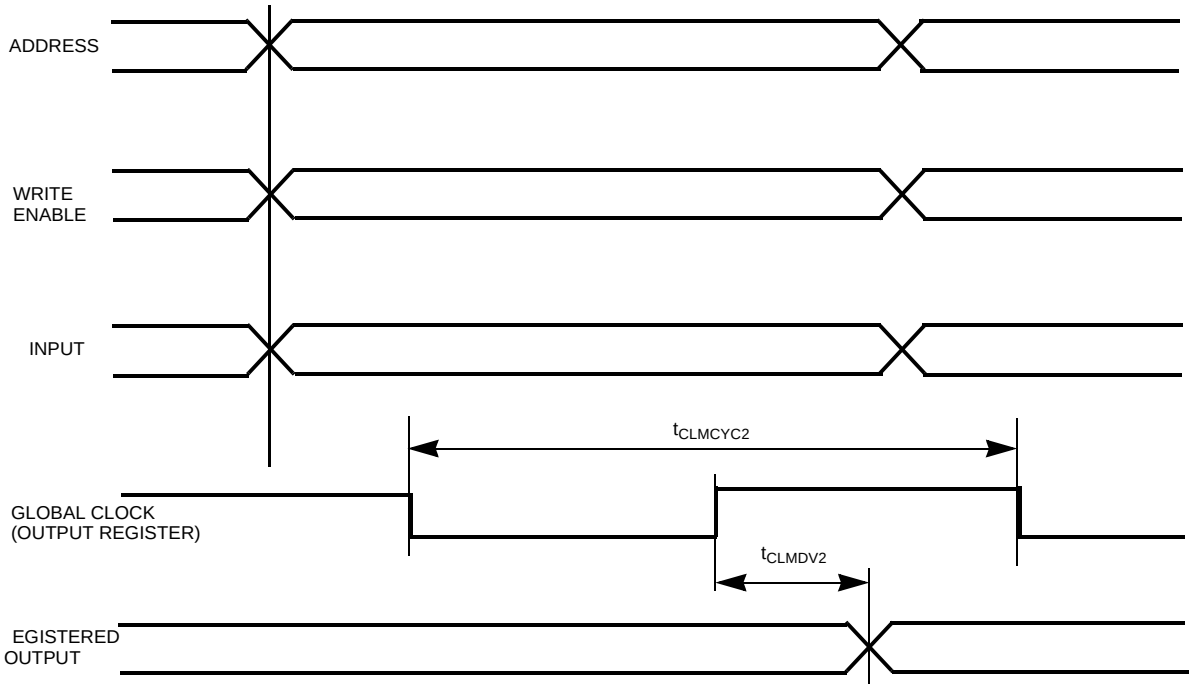


Cluster Memory Internal Clocking

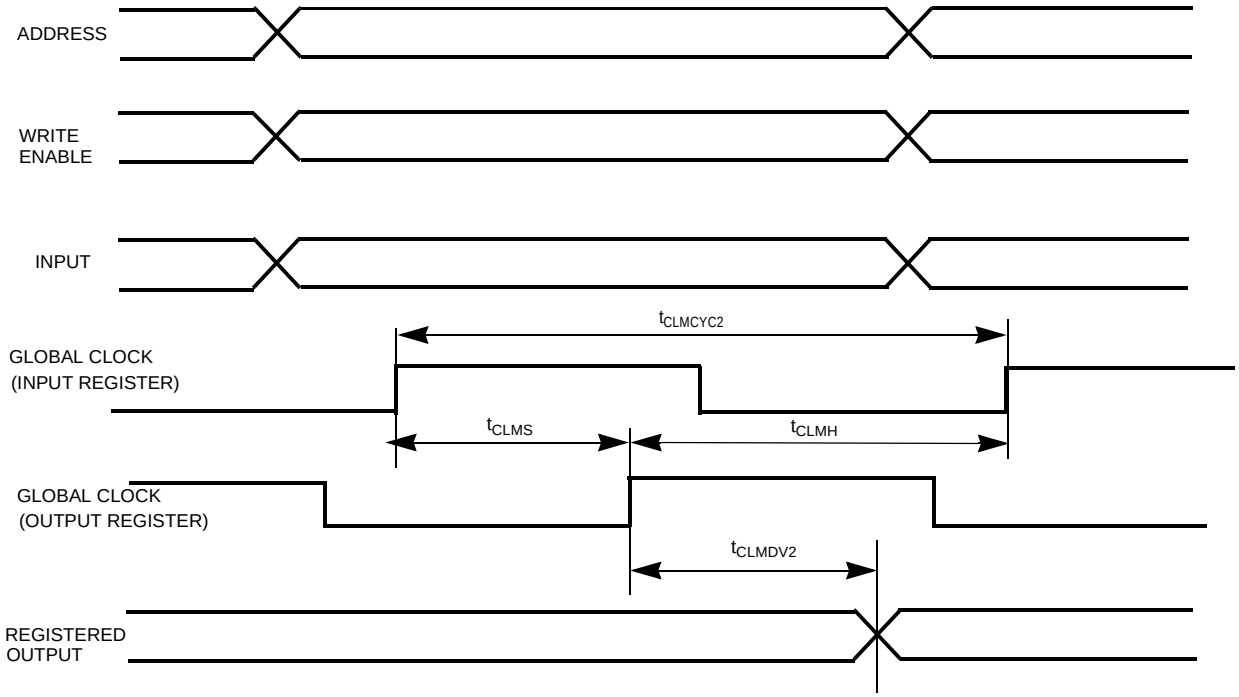


Switching Waveforms (continued)

Cluster Memory Output Register Timing (Asynchronous Inputs)

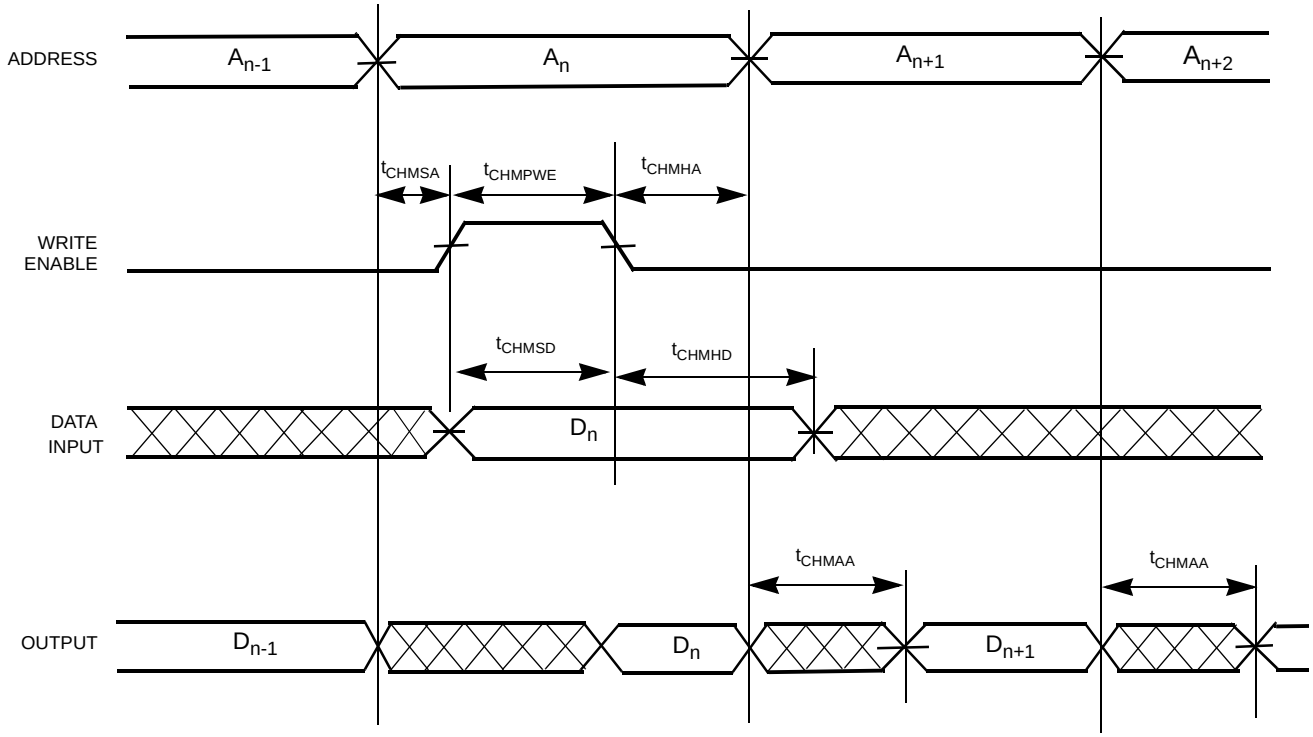


Cluster Memory Output Register Timing (Synchronous Inputs)

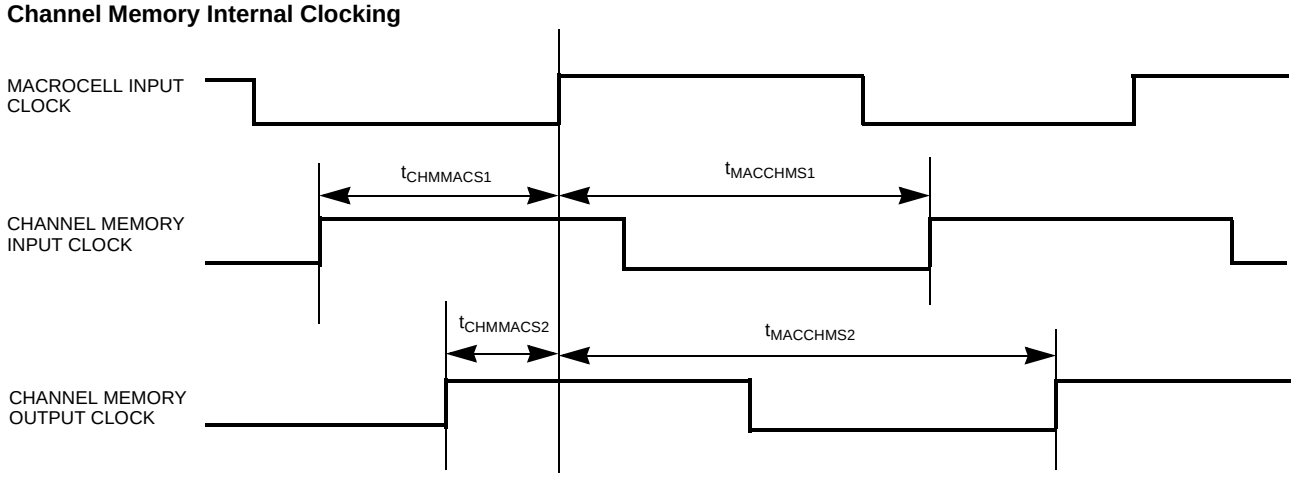


Switching Waveforms (continued)

Channel Memory DP Asynchronous Timing

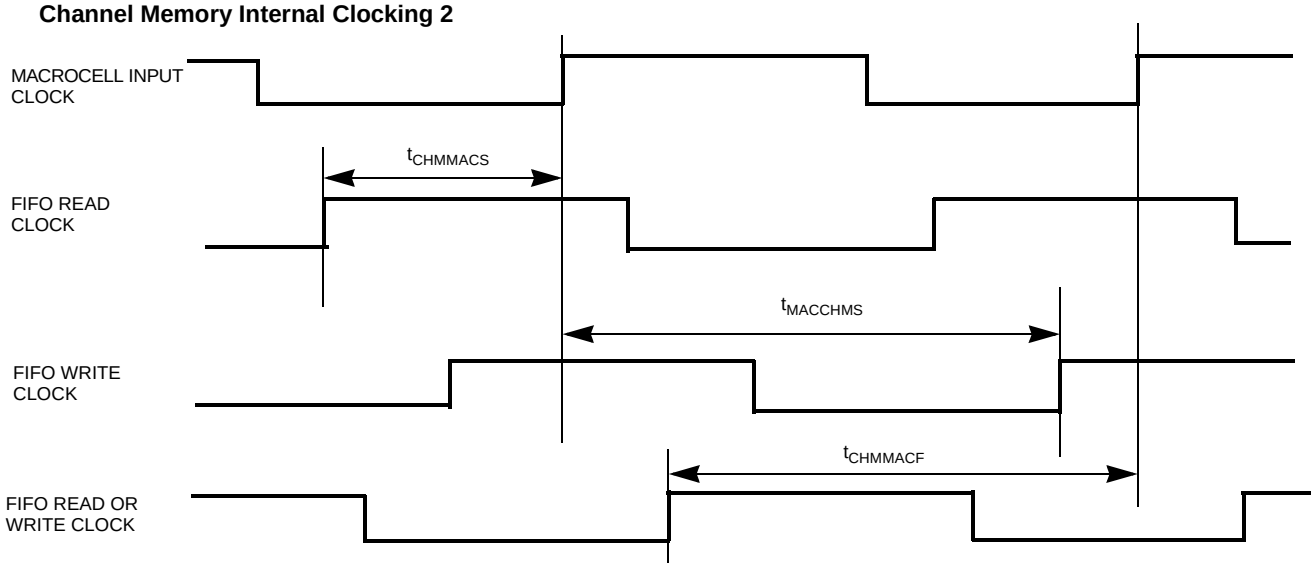


Channel Memory Internal Clocking

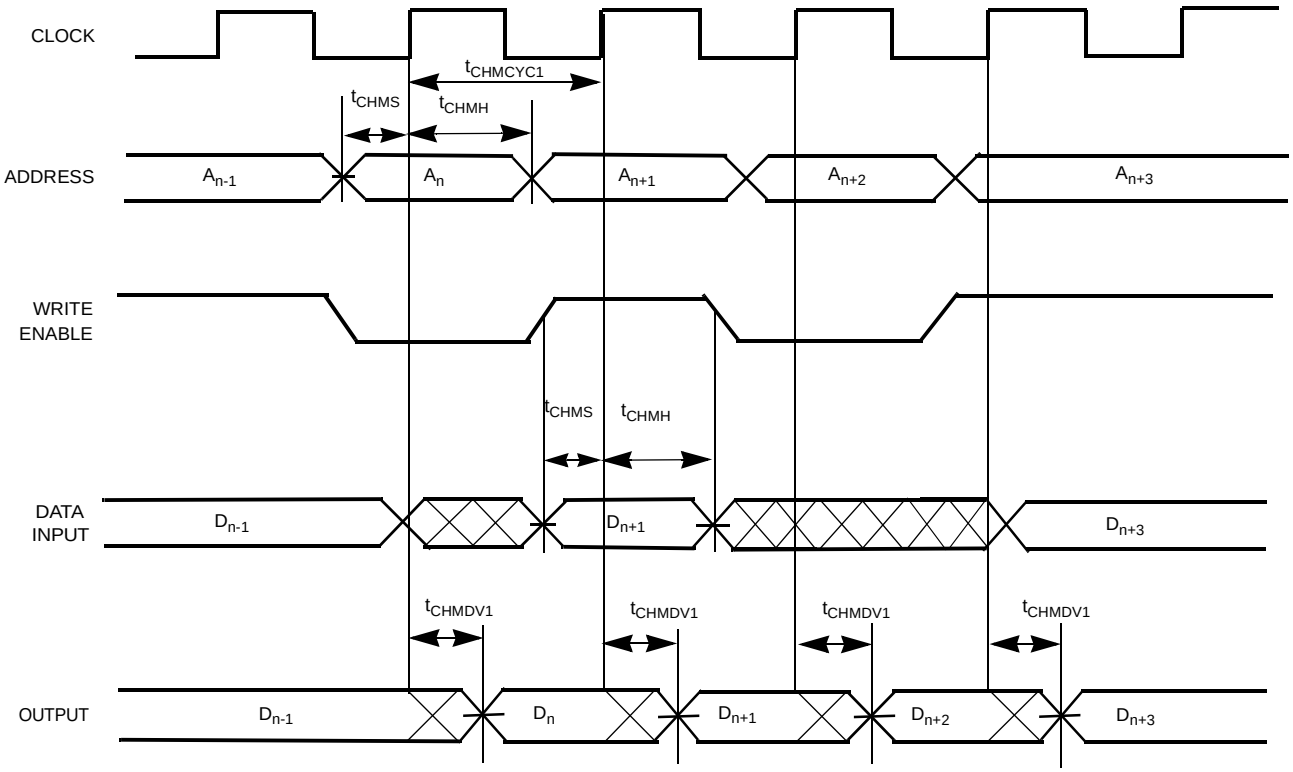


Switching Waveforms (continued)

Channel Memory Internal Clocking 2

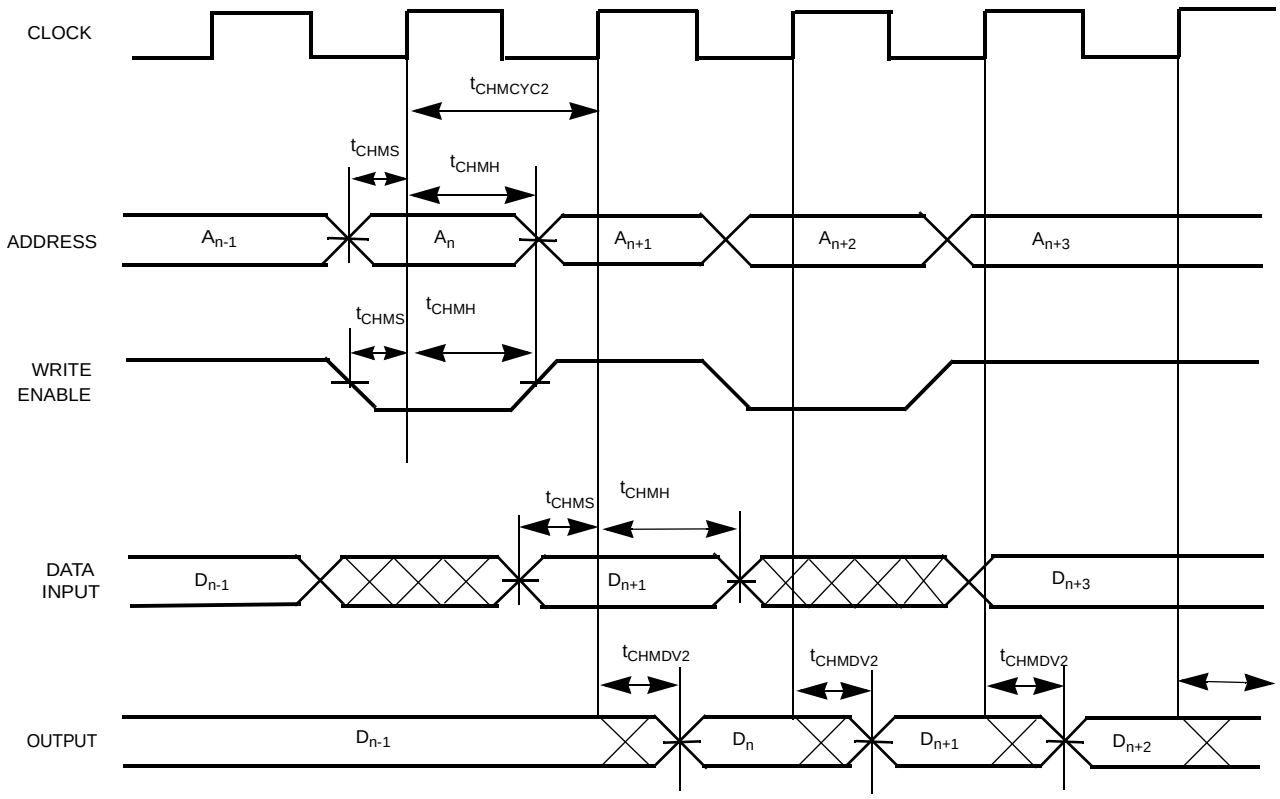


Channel Memory DP SRAM Flow Through R/W Timing

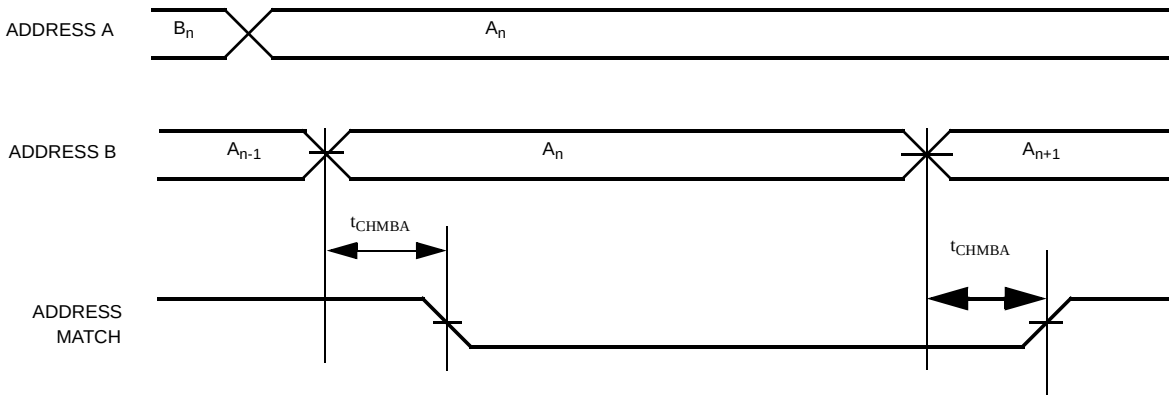


Switching Waveforms (continued)

Channel Memory DP SRAM Pipeline R/W Timing

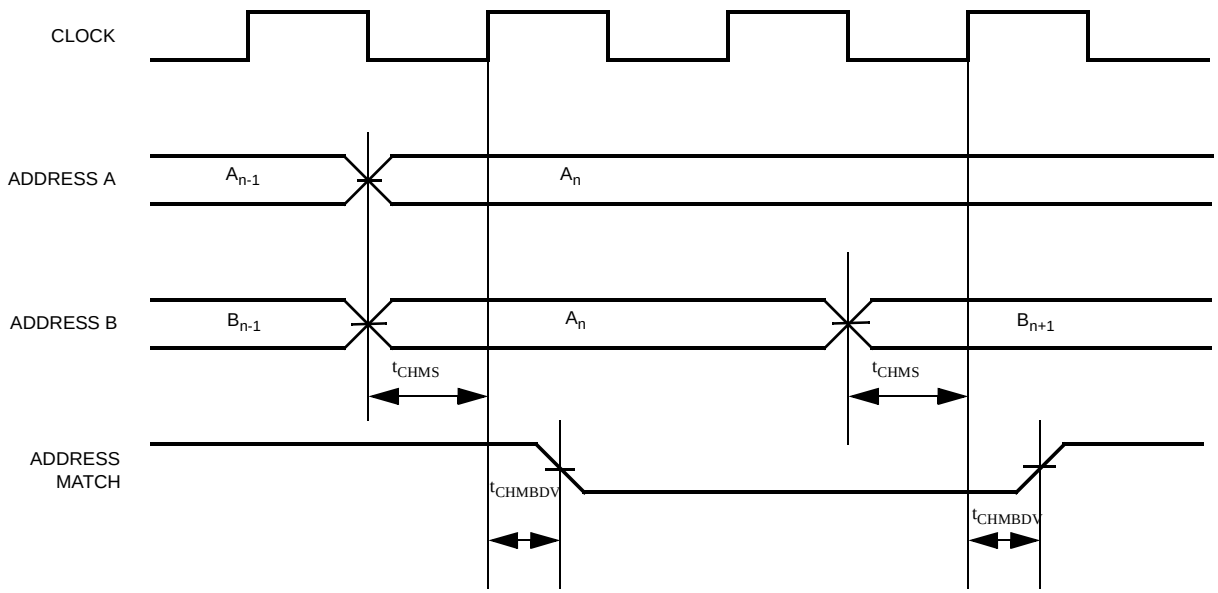


Dual-Port Asynchronous Address Match Busy Signal



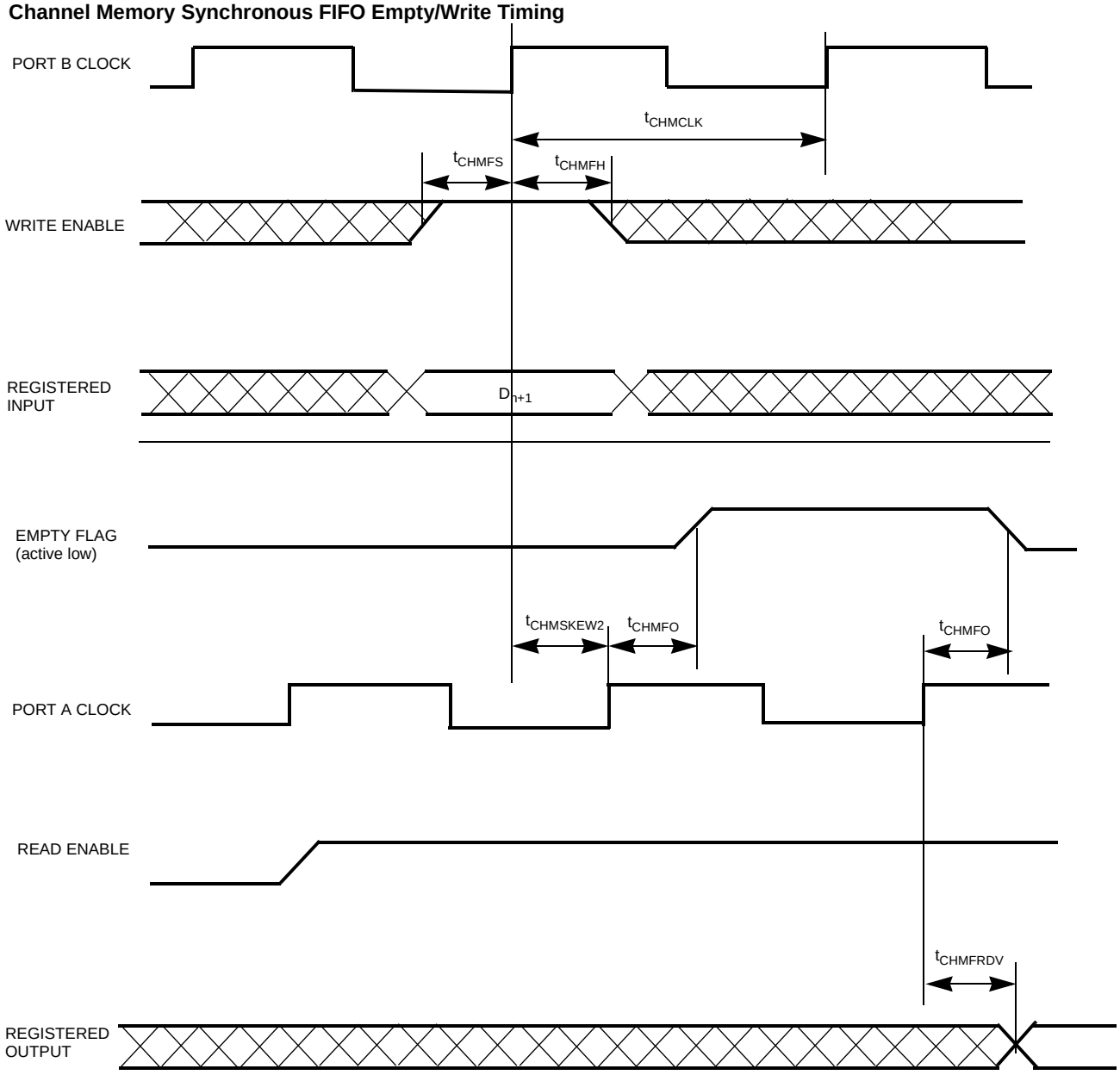
Switching Waveforms (continued)

Dual-Port Synchronous Address Match Busy Signal



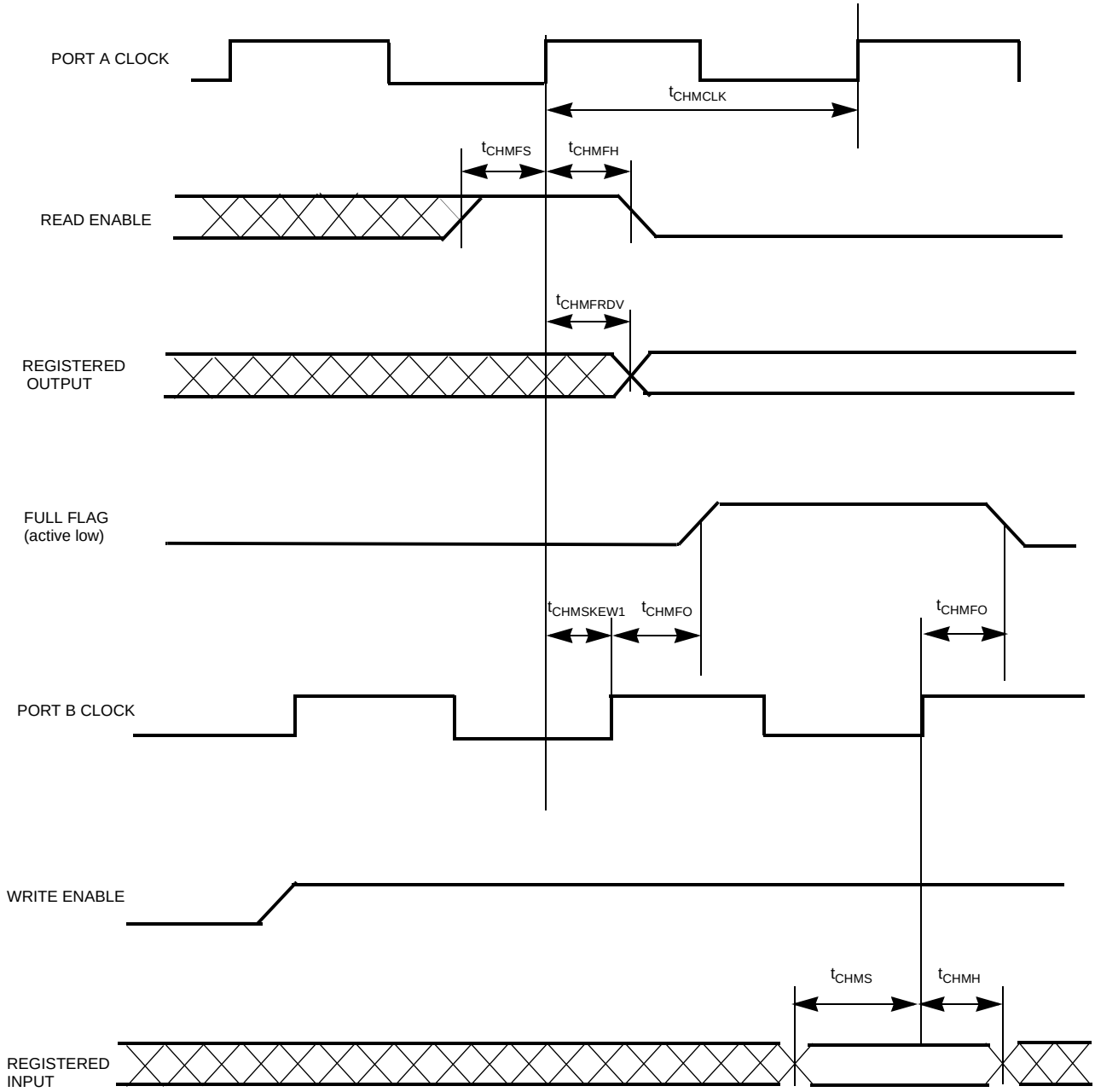
Switching Waveforms (continued)

Channel Memory Synchronous FIFO Empty/Write Timing



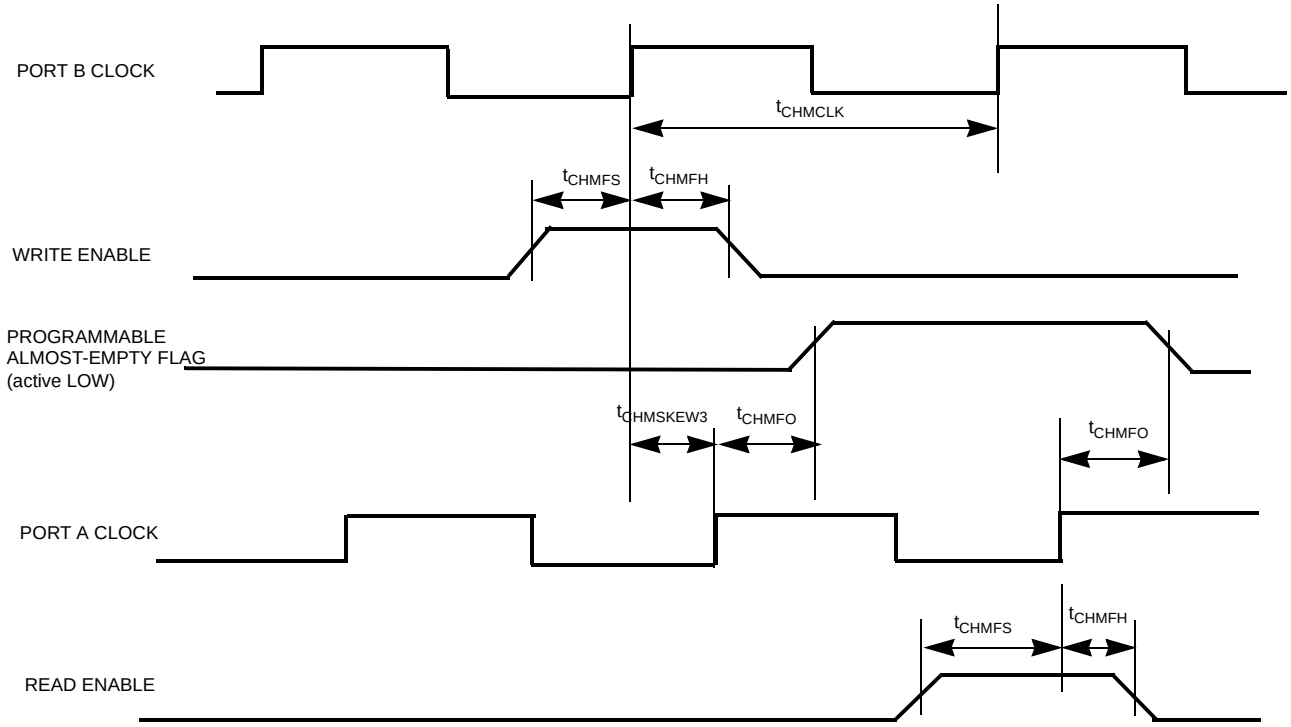
Switching Waveforms (continued)

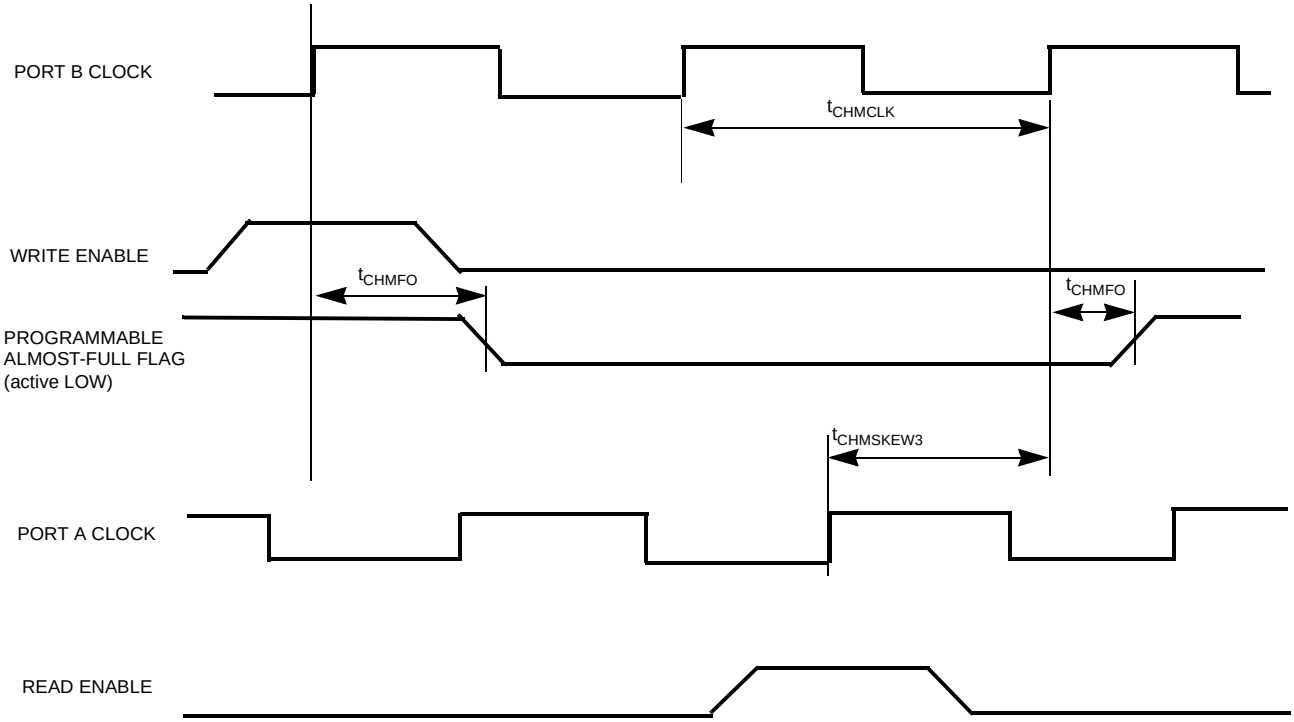
Channel Memory Synchronous FIFO Full/Read Timing



Switching Waveforms (continued)

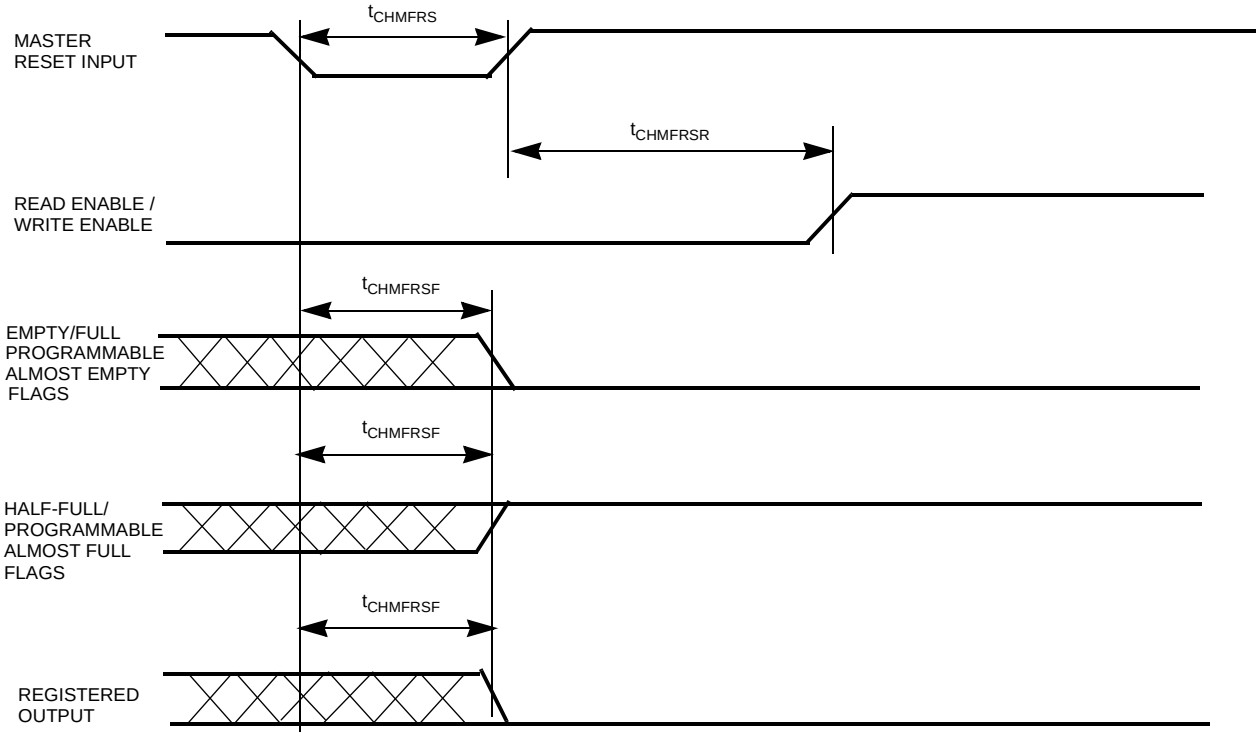
Channel Memory Synchronous FIFO Programmable Flag Timing





Switching Waveforms (continued)

Channel Memory Synchronous FIFO Master Reset Timing



CY 39 100 V 676 - 200 MB C

Cypress Semiconductor ID

Family Type
39 = Delta39K Family

Gate Density
30=30k Usable Gates
50=50k Usable Gates
100=100k Usable Gates
165=165k Usable Gates
200=200k Usable Gates
250=250k Usable Gates
350=350k Usable Gates

Operating Reference Voltage
V = 3.3V or 2.5V Supply Voltage
Z = 1.8V Supply Voltage

Pin Count
208 = 208 Leads
256 = 256 Balls
388 = 388 Balls
484 = 484 Balls
676 = 676 Balls

Operating Conditions
Commercial 0°C to +70°C
Industrial -40°C to +85°C

Package Type
N = Plastic Quad Flat Pack (PQFP)
NT = Thermally Enhanced Quad Flat Pack (EQFP)
BG = Ball Grid Array (BGA)
BB = Fine-Pitch Ball Grid Array (FBGA) 1.0-mm Lead Pitch
MG = Self-Boot Solution - Ball Grid Array
MB = Self-Boot Solution - Fine Pitch Ball Grid Array 1.0-mm Lead Pitch

Speed
233 = 233 MHz
200 = 200 MHz
181 = 181 MHz
167 = 167 MHz
154 = 154 MHz
125 = 125 MHz
83 = 83 MHz

Delta39K Pin Table

Please refer to document titled “Delta39K Pin Tables” for pinouts of all the packages of all Delta39K family members. You can access this document on the internet at: http://www.cypress.com/pld/datasheets.html.

Delta39K Part Numbers[17] (Ordering Information)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K30	233	CY39030V208-233NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39030Z208-233NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39030V256-233BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030Z256-233BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-233MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030Z256-233MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
	125	CY39030V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39030Z208-125NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39030V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030Z256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-125MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030Z256-125MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K30	125	CY39030V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39030Z208-125NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39030V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030Z256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-125MBI	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030Z256-125MBI	MB256	256-Lead Fine Pitch Ball Grid Array	√	
	83	CY39030V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39030Z208-83NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39030V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030Z256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-83MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030Z256-83MBC	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030V208-83NTI	NT208	208-Lead Plastic Quad Flat Pack		Industrial
		CY39030Z208-83NI	N208	208-Lead Enhanced Quad Flat Pack		
		CY39030V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030Z256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39030V256-83MBI	MB256	256-Lead Fine Pitch Ball Grid Array	√	
		CY39030Z256-83MBI	MB256	256-Lead Fine Pitch Ball Grid Array	√	
39K50	233	CY39050V208-233NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39050Z208-233NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39050V256-233BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050Z256-233BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-233MGC	MG388	388-Lead Ball Grid Array	√	
		CY39050Z388-233MGC	MG388	388-Lead Ball Grid Array	√	
		CY39050V484-233MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050Z484-233MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
	125	CY39050V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39050Z208-125NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39050V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050Z256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-125MGC	MG388	388-Lead Pitch Ball Grid Array	√	
		CY39050Z388-125MGC	MG388	388-Lead Pitch Ball Grid Array	√	
		CY39050V484-125MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050Z484-125MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K50	125	CY39050V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39050Z208-125NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39050V256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050Z256-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-125MBI	MG388	388-Lead Fine Pitch Ball Grid Array	√	
		CY39050Z388-125MBI	MG388	388-Lead Fine Pitch Ball Grid Array	√	
		CY39050V484-125MBI	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050Z484-125MBI	MB484	484-Lead Fine Pitch Ball Grid Array	√	
	83	CY39050V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39050Z208-83NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39050V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050Z256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39050Z388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39050V484-83MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050Z484-83MBC	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050V208-83NTI	NT208	208-Lead Plastic Quad Flat Pack		Industrial
		CY39050Z208-83NI	N208	208-Lead Enhanced Quad Flat Pack		
		CY39050V256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050Z256-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39050V388-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39050Z388-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39050V484-83MBI	MB484	484-Lead Fine Pitch Ball Grid Array	√	
		CY39050Z484-83MBI	MB484	484-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K100 [18]	200	CY39100V208-200NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39100V256-200BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484-200BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388-200MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676-200MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208A-200NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39100V256A-200BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484A-200BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388A-200MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676A-200MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-200NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39100Z208B-200NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39100V256B-200BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100Z256B-200BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-200BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100Z484B-200BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-200MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100Z388B-200MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-200MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100Z676B-200MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K100 [18]	125	CY39100V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39100V256-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208A-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39100V256A-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484A-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388A-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676A-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39100Z208B-125NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39100V256B-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100Z256B-125BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100Z484B-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100Z388B-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100Z676B-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39100Z208B-125NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39100V256B-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100Z256B-125BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100Z484B-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-125MGI	MG388	388-Lead Ball Grid Array	√	
		CY39100Z388B-125MGI	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-125MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100Z676B-125MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K100 [18]	83	CY39100V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39100V256-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208A-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39100V256A-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484A-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388A-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676A-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		
		CY39100Z208B-83NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39100V256B-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100Z256B-83BBC	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100Z484B-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100Z388B-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100Z676B-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100V208B-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39100Z208B-83NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39100V256B-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100Z256B-83BBI	BB256	256-Lead Fine Pitch Ball Grid Array		
		CY39100V484B-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100Z484B-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39100V388B-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39100Z388B-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39100V676B-83MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39100Z676B-83MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K165	181	CY39165V208-181NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39165Z208-181NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39165V484-181BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165Z484-181BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165V388-181MGC	MG388	388-Lead Ball Grid Array	√	
		CY39165Z388-181MGC	MG388	388-Lead Ball Grid Array	√	
		CY39165V676-181MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165Z676-181MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
	125	CY39165V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39165Z208-125NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39165V484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165Z484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165V388-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39165Z388-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39165V676-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165Z676-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39165Z208-125NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39165V484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165Z484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165V388-125MGI	MG388	388-Lead Ball Grid Array	√	
		CY39165Z388-125MGI	MG388	388-Lead Ball Grid Array	√	
		CY39165V676-125MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165Z676-125MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
	83	CY39165V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39165Z208-83NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39165V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165Z484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165V388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39165Z388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39165V676-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165Z676-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165V208-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39165Z208-83NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39165V484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165Z484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39165V388-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39165Z388-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39165V676-83MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39165Z676-83MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	

Delta39K Part Numbers[17] (Ordering Information) (continued)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Self-Boot Solution	Operating Range
39K200	181	CY39200V208-181NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39200Z208-181NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39200V484-181BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200Z484-181BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-181MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200Z388-181MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-181MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200Z676-181MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
	125	CY39200V208-125NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39200Z208-125NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39200V484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200Z484-125BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200Z388-125MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200Z676-125MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200V208-125NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39200Z208-125NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39200V484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200Z484-125BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-125MGI	MG388	388-Lead Ball Grid Array	√	
		CY39200Z388-125MGI	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-125MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200Z676-125MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
	83	CY39200V208-83NTC	NT208	208-Lead Enhanced Quad Flat Pack		Commercial
		CY39200Z208-83NC	N208	208-Lead Plastic Quad Flat Pack		
		CY39200V484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200Z484-83BBC	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200Z388-83MGC	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200Z676-83MBC	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200V208-83NTI	NT208	208-Lead Enhanced Quad Flat Pack		Industrial
		CY39200Z208-83NI	N208	208-Lead Plastic Quad Flat Pack		
		CY39200V484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200Z484-83BBI	BB484	484-Lead Fine Pitch Ball Grid Array		
		CY39200V388-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39200Z388-83MGI	MG388	388-Lead Ball Grid Array	√	
		CY39200V676-83MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	
		CY39200Z676-83MBI	MB676	676-Lead Fine Pitch Ball Grid Array	√	

17. For the availability of Delta39KZ devices (1.8V), please contact your local sales office
18. Refer to the section titled “Delta39K100 Revisions/Errata” on page 49

Delta39K100 Revisions/Errata

Three revisions of Delta39K100, in 3.3V version, are currently offered which are marked as CY39100Vxxx, CY39100VxxxA and CY39100VxxxB. CY39100VxxxB devices operate exactly as specified in this data sheet. The following paragraphs explain the operation of the CY39100Vxxx and CY39100VxxxA parts as different from this data sheet:

CY39100Vxxx

1. The internal regulator takes several seconds to power down. Hence, cycling the power supply (within 8 seconds) may cause a high standby current (200 mA to 1A) until the part is configured.
2. The part always configures on power-up and will reconfigure on HIGH to LOW edge of the *Reconfig* pin. Please refer to the application note titled “Configuring Delta39K/Quantum38K” at http://www.cypress.com for more details.
3. The *Self Config* instruction starts reconfiguring the CPLD upon execution of the *Update-IR* state of the JTAG TAP controller state machine. In CY39100VxxxB parts, *Self Config* instruction is executed upon execution of *Test-Logic-Reset* state of the TAP controller.
4. An ESD failure is very unlikely. CDM ESD passes 1000V. HBM ESD passes 3300V with all I/O bank’s V_{CCIO} shorted together. If V_{CCIO}s in a bank are tested separately a percentage of parts will fail HBM ESD over 500V.

CY39100VxxxA

1. The part always configures on power-up and will reconfigure on HIGH to LOW edge of the *Reconfig* pin. Please refer to the application note titled “Configuring Delta39K/Quantum38K” at http://www.cypress.com for more details.
2. The *Self Config* instruction starts reconfiguring the CPLD upon execution of the *Update-IR* state of the JTAG TAP controller state machine. In CY39100VxxxB parts, *Self Config* instruction is executed upon execution of *Test-Logic-Reset* state of the TAP controller.
3. An ESD failure is very unlikely. CDM ESD passes 1000V. HBM ESD passes 3300V with all I/O bank’s V_{CCIO} shorted together. If V_{CCIO}s in a bank are tested separately a percentage of parts will fail HBM ESD over 500V.

CPLD Boot EEPROM[19] Part Numbers (Ordering Information)

Device	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
2Mbit	15	CY3LV002-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV002-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
1Mbit	15	CY3LV010-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV010-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
512Kbit	15	CY3LV512-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	10	CY3LV512-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial

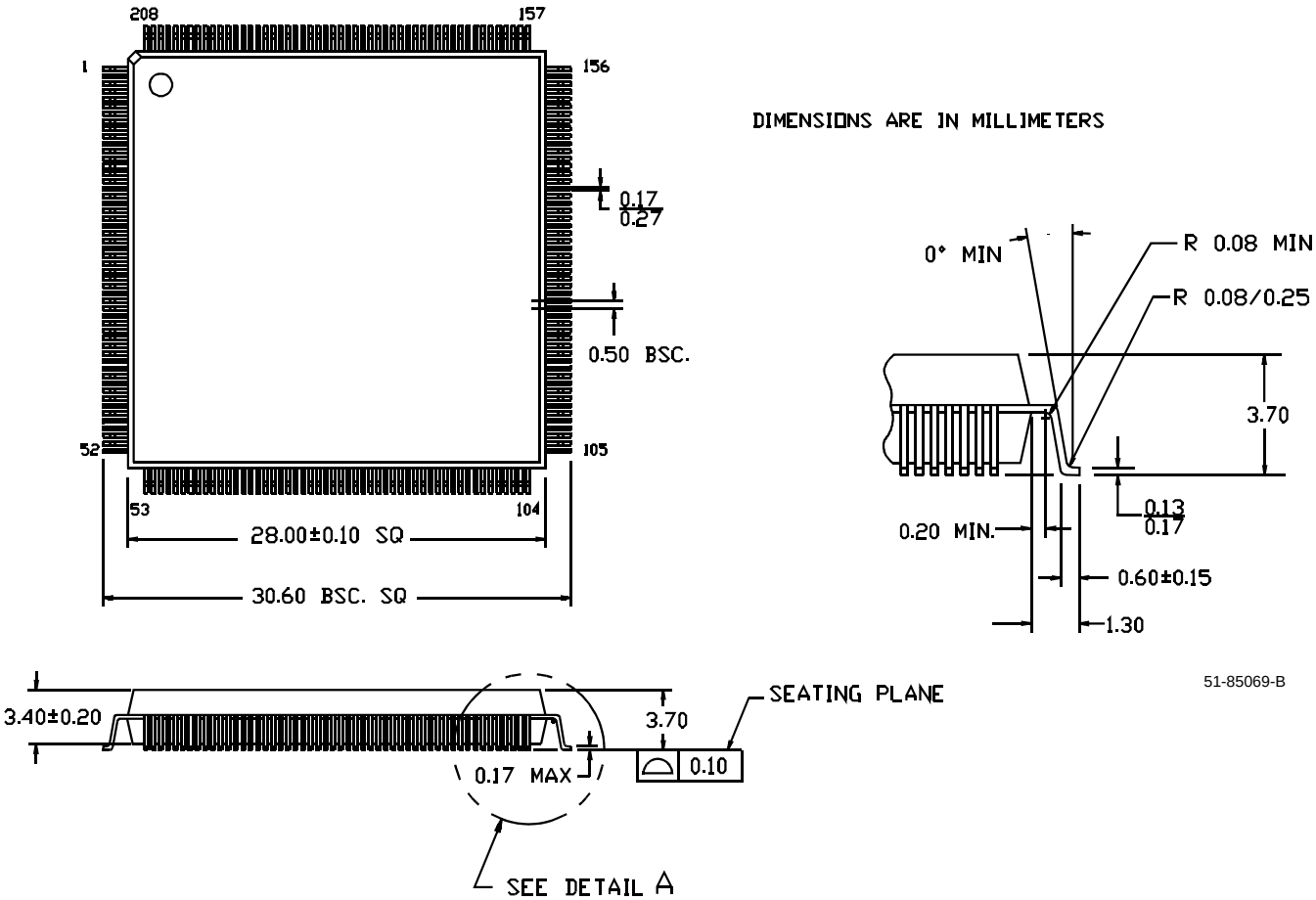
Recommended CPLD Boot EEPROM for corresponding Delta39K CPLDs

CPLD Device	Recommended boot EEPROM
39K30	CY3LV512
39K50	CY3LV512
39K100	CY3LV010
39K165	CY3LV002
39K200	CY3LV002

Note:
19. See the data sheet titled “CPLD Boot EEPROM” for detailed architectural and timing information.

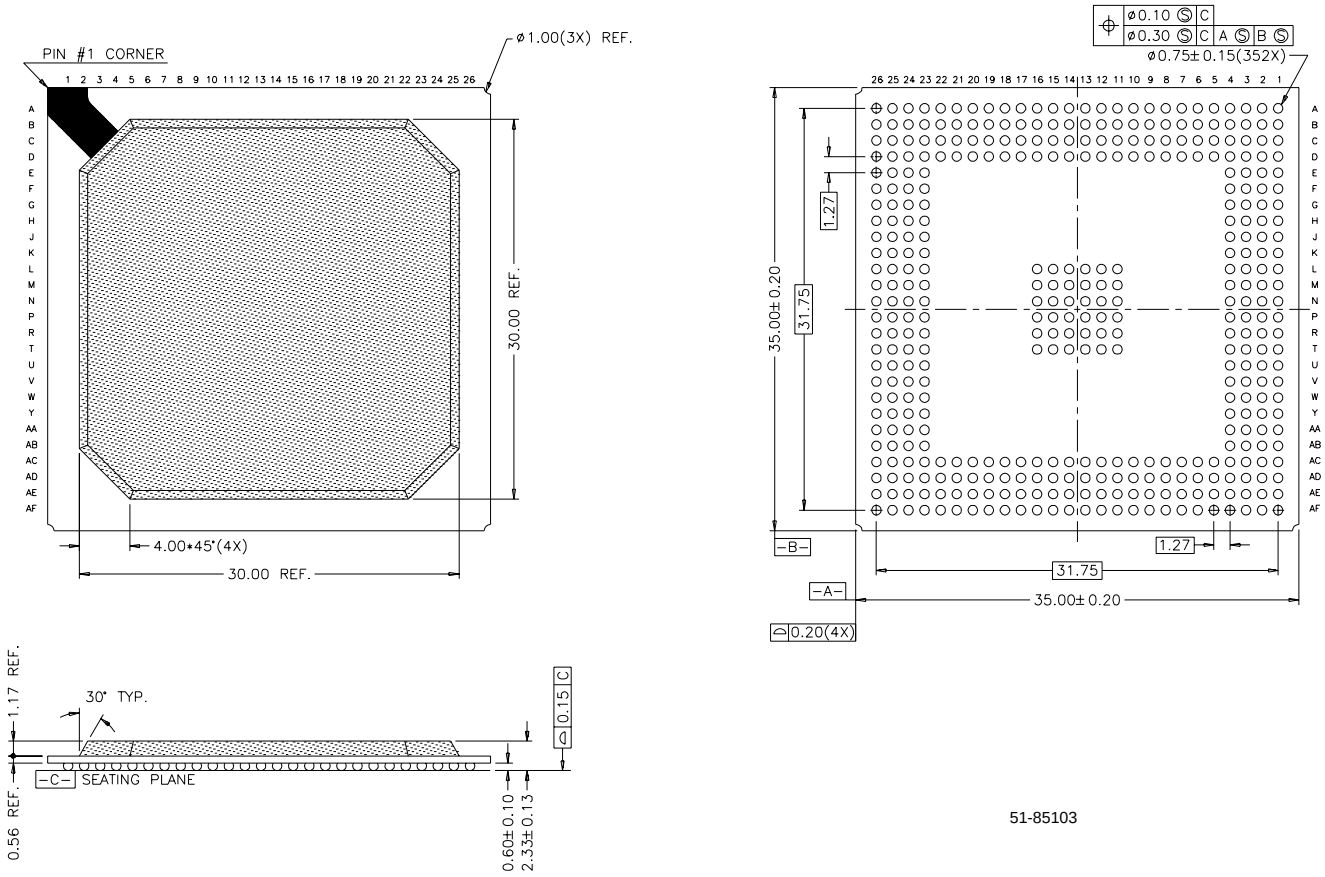
Package Diagrams

208-Lead Plastic Quad Flatpack (PQFP) N208
208-Lead Enhanced Quad Flat Pack (EQFP) NT208



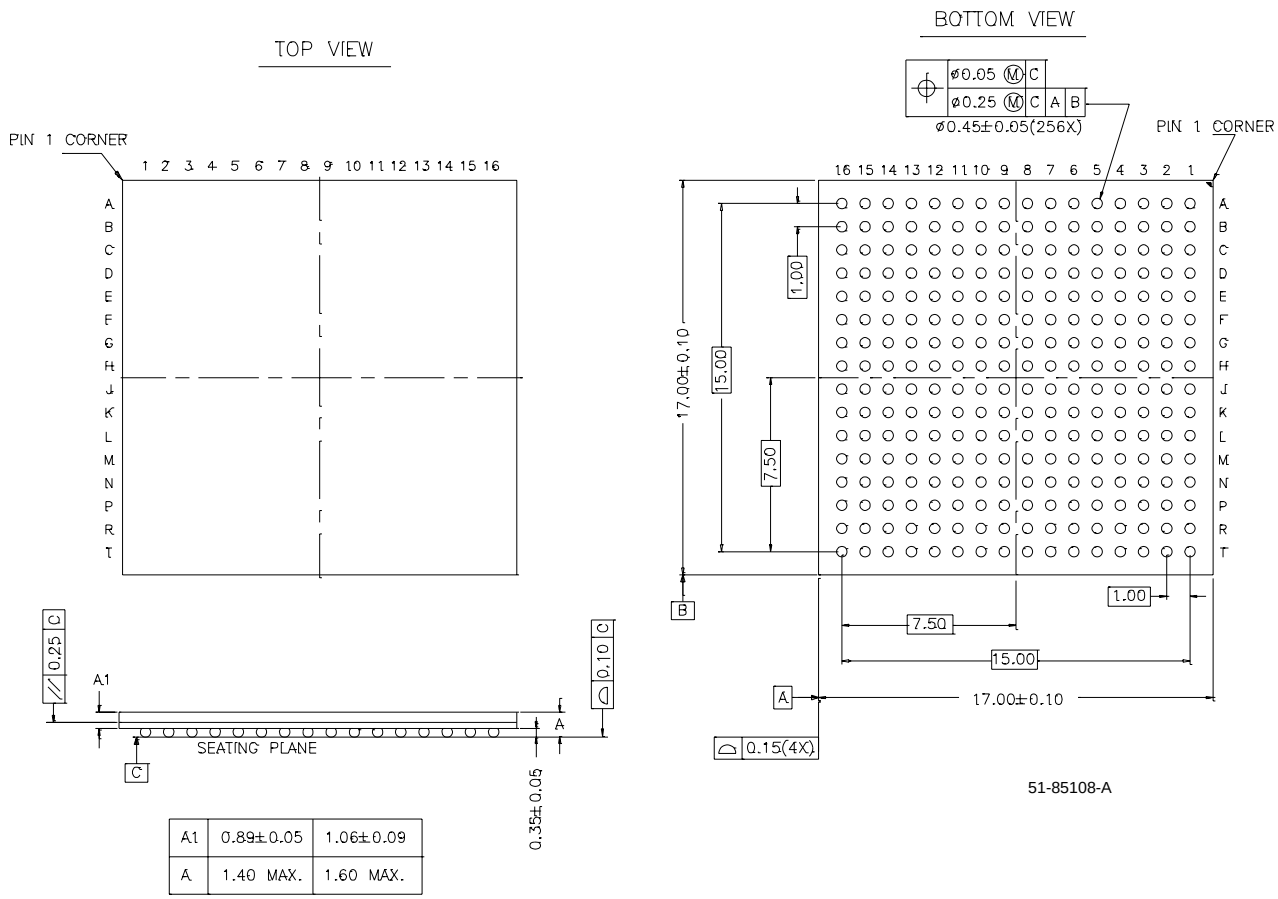
Package Diagrams (continued)

388-Lead Ball Grid Array MG388



Package Diagrams (continued)

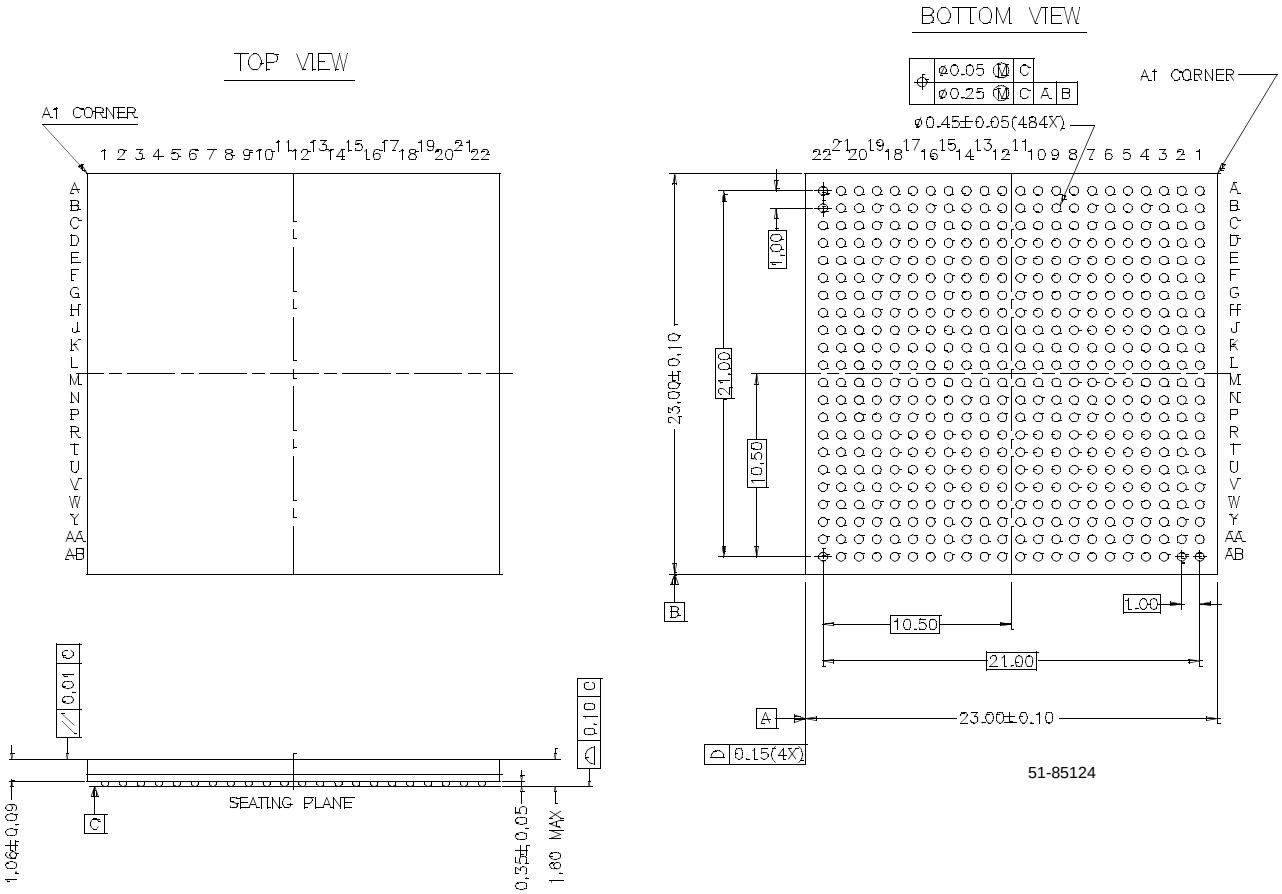
256-Ball Thin Ball Grid Array (17 x 17 x 1.6 mm) BB256/MB256



A1	0.89±0.05	1.06±0.09
A	1.40 MAX.	1.60 MAX.

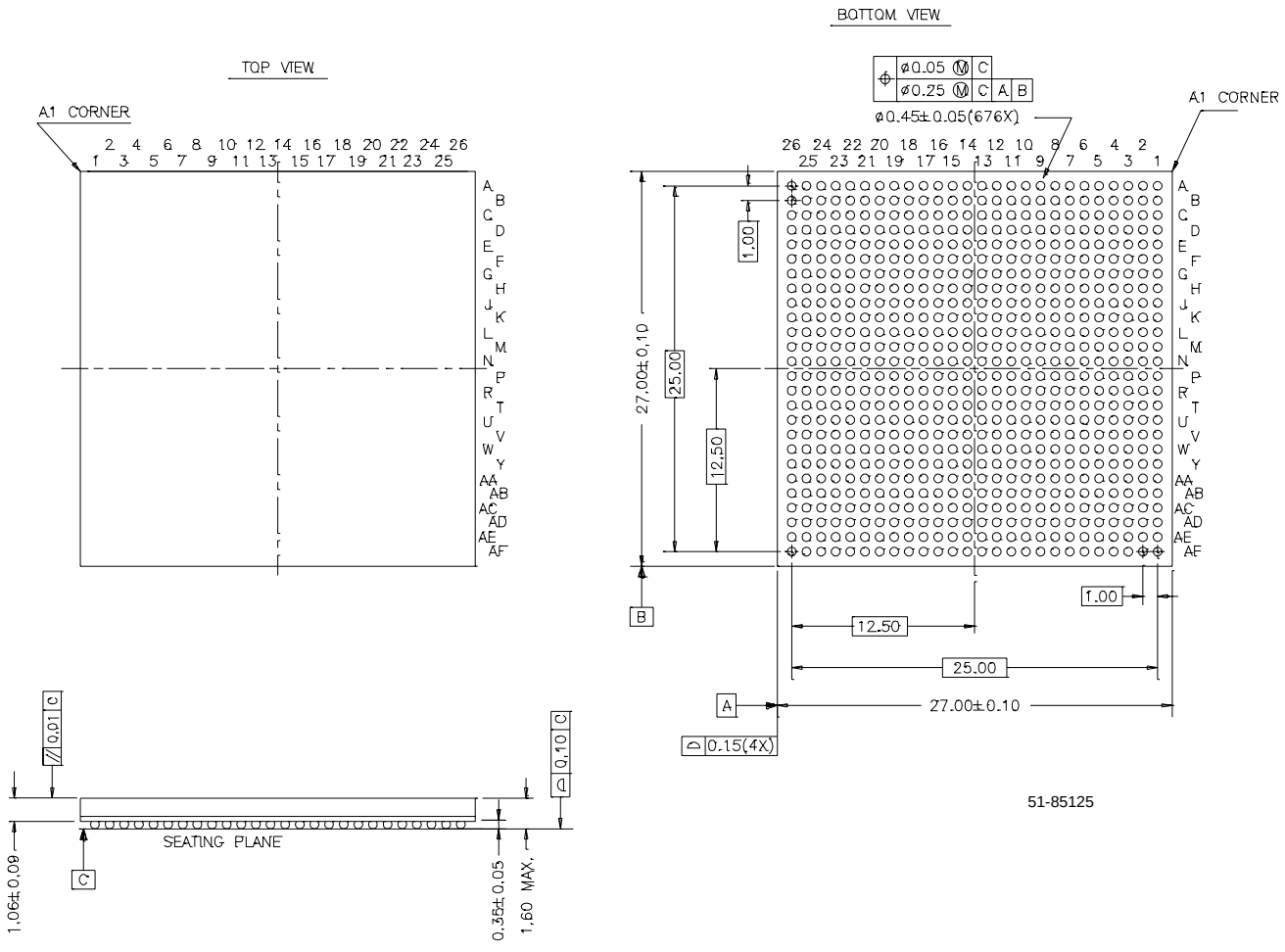
Package Diagrams (continued)

484-Ball Thin Ball Grid Array (23 x 23 x 1.6 mm) BB484/MB484



Package Diagrams (continued)

676-Ball FBGA (27 x 27 x 1.6 mm) BB676



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Document Title: DELTA39K™ ISR™ CPLD FAMILY Document Number: 38-03039				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106503	05/30/01	SZV	Change from Spec #: 38-00830 to 38-03039
*A	107625	07/11/01	RN	Deleted 39K15 device and the associate -250 MHz bin specs. Deleted 144FBGA package and associated part numbers. Changed ESD spec from “MIL-STD-883” to “JEDEC EIA./JESD22-A114-A “. Changed the Prime bin for 39K50 & 39K30 from “ MHz” to “233 MHz”. Changed the part ordering information accordingly. Updated the -233 MHz timing specs to match modified timing specs achieved by design (main affected params: t_{PD}, t_{MCCO}, t_{IOS}, t_{SCS}, t_{SCS2}, f_{MAX2}, t_{CLMAA}, $t_{CLMCYC2}$, $t_{CHMCYC2}$, t_{CHMCLK}). Updated I/O standard Timing Delay Specs and changed the default I/O standard from 3.3V PCI to LVCMOS. Added paragraph about Delta39K being CompactPCI hot swap Ready. Added X8 mode in the PLL description. Added Standby ICC spec. Updated the recommended boot PROM for 39K165/200 to be CY3LV002 instead of CY3LV020.