



INTEL CORP (MEMORY/PLD)/

56E D ■ 4826176 0077322 01T ■ ITL2

28F008SA-L

T-46-13-26

8 MBIT (1 MBIT x 8) FLASHFILE™ MEMORY

- **High-Density Symmetrically Blocked Architecture**
—Sixteen 64 KByte Blocks
- **Low-Voltage Operation**
—3.3V ± 0.3V or 5.0V ± 10% V_{CC}
- **Extended Cycling Capability**
—10,000 Block Erase Cycles
—160,000 Block Erase Cycles Per Chip
- **Automated Byte Write and Block Erase**
—Command User Interface
—Status Register
- **System Performance Enhancements**
—RY/BY Status Output
—Erase Suspend Capability
- **High-Performance Read**
—200 ns Maximum Access Time
- **Deep-Powerdown Mode**
—0.20 µA I_{CC} Typical
- **SRAM-Compatible Write Interface**
- **Hardware Data Protection Feature**
—Erase/Write Lockout During Power Transitions
- **Industry Standard Packaging**
—40-Lead TSOP, 44-Lead PSOP
- **ETOX™ III Nonvolatile Flash Technology**
—12V Byte Write/Block Erase

Intel's 28F008SA-L 8 Mbit FlashFile™ Memory is the highest density nonvolatile read/write solution for solid state storage. The 28F008SA-L's cycling, symmetrically blocked architecture, access time, write automation and very low power consumption provide a more reliable, lower power, lighter weight and higher performance alternative to traditional rotating disk technology. The 28F008SA-L brings new capabilities to 3.3V portable computing. Application and operating system software stored in resident flash memory arrays provide instant-on, rapid execute-in-place and protection from obsolescence through in-system software updates. Resident software also extends system battery life and increases reliability by reducing disk drive accesses.

For high density data acquisition applications, the 28F008SA-L offers a more cost-effective and reliable alternative to SRAM and battery. Traditional high density embedded applications, such as telecommunications, can take advantage of the 28F008SA-L's nonvolatility, blocking and minimal system code requirements for flexible firmware and modular software designs.

The 28F008SA-L is offered in 40-lead TSOP (standard and reverse) and 44-lead PSOP packages. Pin assignments simplify board layout when integrating multiple devices in a flash memory array or subsystem. This device uses an integrated Command User Interface and state machine for simplified block erasure and byte write. The 28F008SA-L memory map consists of 16 separately erasable 64 Kbyte blocks.

Intel's 28F008SA-L employs advanced CMOS circuitry for systems requiring low power consumption and noise immunity. Its 200ns access time provides superior performance when compared with magnetic storage media. A deep powerdown mode lowers power consumption to 0.66 µW typical thru V_{CC}, crucial in portable computing, handheld instrumentation and other low-power applications. The PWD power control input also provides absolute data protection during system powerup/down.

Manufactured on Intel's 0.8 micron ETOX process, the 28F008SA-L provides the highest levels of quality, reliability and cost-effectiveness.

* Microsoft is a trademark of Microsoft Corporation.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

© Intel Corporation, 1992

March 1992

Order Number: 290435-001



PRODUCT OVERVIEW

T-46-13-26

The 28F008SA-L is a high-performance **8 Mbit** (8,388,608 bit) memory organized as **1 Mbyte** (1,048,576 bytes) of 8 bits each. **Sixteen 64 KByte** (65,536 byte) **blocks** are included on the 28F008SA-L. A memory map is shown in figure 6 of this specification. A block erase operation erases one of the sixteen blocks of memory in typically **2.0 seconds**, independent of the remaining blocks. Each block can be independently erased and written **10,000 cycles**. **Erase Suspend** allows system software to suspend block erase to read data or execute code from any other block of the 28F008SA-L.

The 28F008SA-L is available in the **40-lead TSOP** (Thin Small Outline, 1.2 mm thick) and **44-lead PSOP** (Plastic Small Outline) packages. Pinouts are shown in figures 2 and 4 of this specification.

The **Command User Interface** serves as the interface between the microprocessor or microcontroller and the internal operation of the 28F008SA-L.

Byte Write and Block Erase Automation allow byte write and block erase operations to be executed using a two-write command sequence to the Command User Interface. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for byte write and block erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in byte increments typically within **11 μ s**. **I_{pp} byte write and block erase currents are 10mA typical, 30mA maximum. V_{pp} byte write and block erase voltage is 11.4V to 12.6V.**

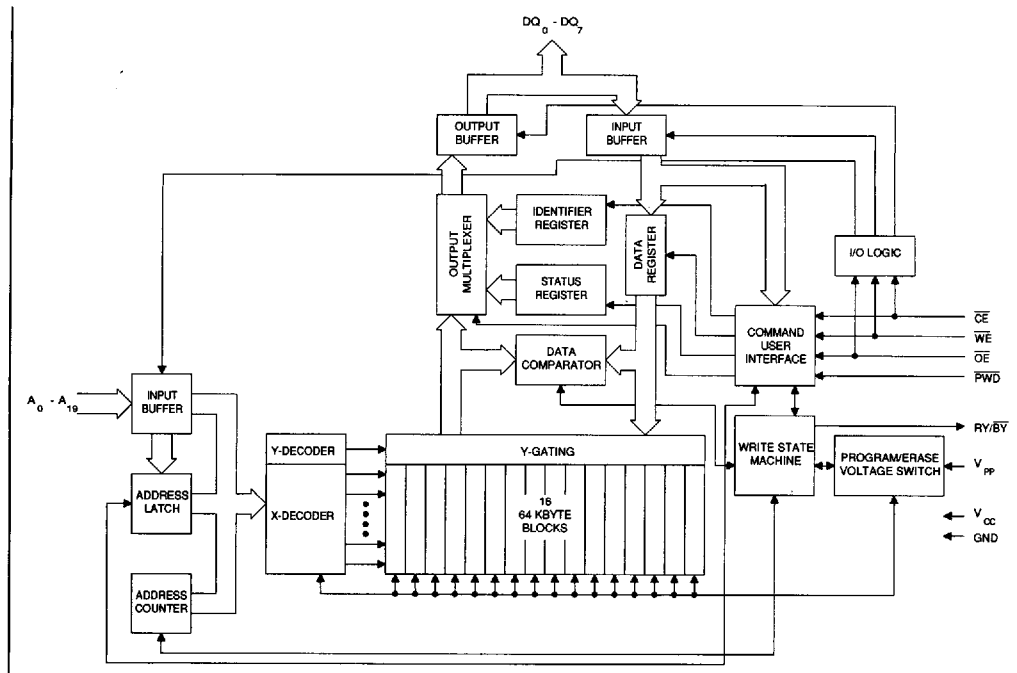
The **Status Register** indicates the status of the WSM and when the WSM successfully completes the desired byte write or block erase operation.

The **RY/ \overline{BY}** output gives an additional indicator of WSM activity, providing capability for both hardware signal of status (versus software polling) and status masking (interrupt masking for background erase, for example). Status polling using RY/ \overline{BY} minimizes both CPU overhead and system power consumption. When low, RY/ \overline{BY} indicates that the WSM is performing a block erase or byte write operation. RY/ \overline{BY} high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode.

Maximum access time is **200ns (t_{ACC})** over the commercial temperature range (0 °C to 70 °C) and over V_{CC} supply voltage range (3.0V to 3.6V, 4.5 to 5.5V). **I_{CC} active current (CMOS Read) is 5mA typical, 12mA maximum at 5 MHz, 3.3V \pm 0.3V.**

When the \overline{CE} and \overline{PWD} pins are at V_{CC} , the I_{CC} **CMOS Standby** mode is enabled.

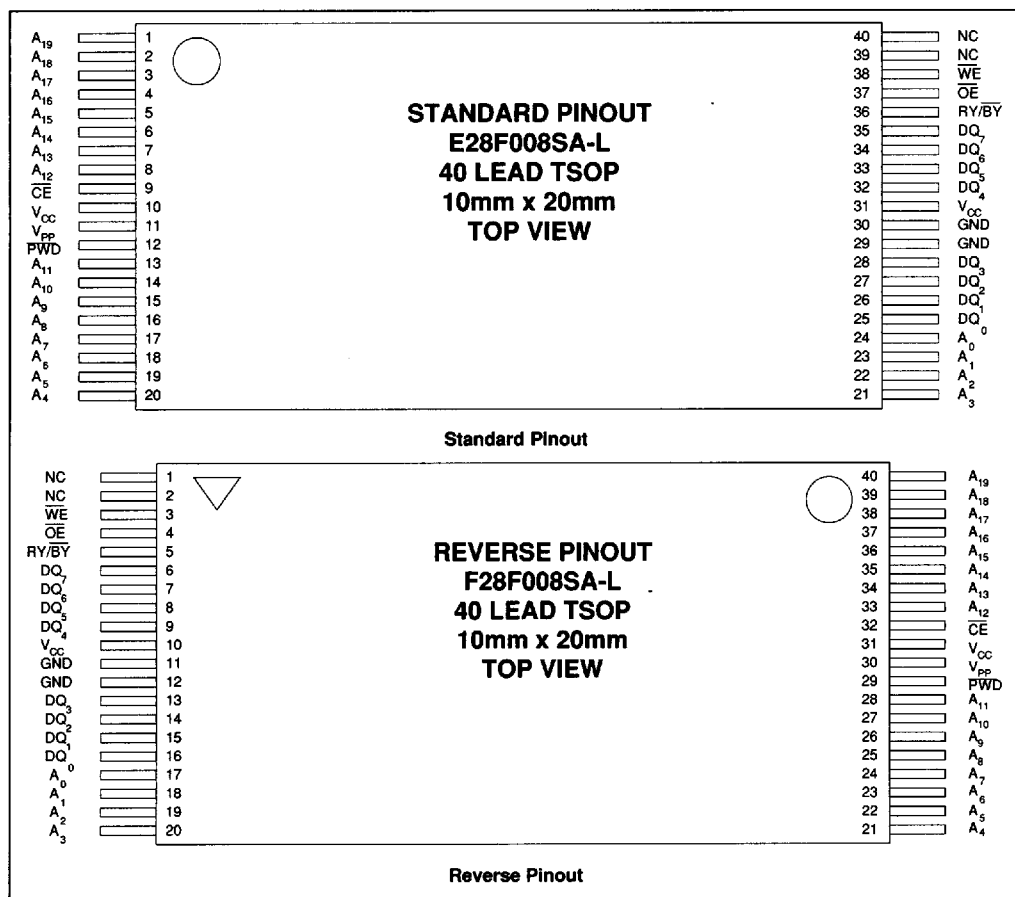
A **Deep Powerdown** mode is enabled when the \overline{PWD} pin is at GND, minimizing power consumption and providing write protection. **I_{CC} current in deep powerdown is 0.20 μ A typical.** Reset time of 500ns is required from \overline{PWD} switching high until outputs are valid to read attempts. Equivalently, the device has a wake time of 1 μ s from \overline{PWD} high until writes to the Command User Interface are recognized by the 28F008SA-L. With \overline{PWD} at GND, the WSM is reset and the Status Register is cleared.

INTEL CORP (MEMORY/PLD/
56E D
4826176 0077324 992 ITL2

Figure 1. Block Diagram
Table 1. Pin Description

Symbol	Type	Name and Function
$A_0 - A_{19}$	INPUT	ADDRESS INPUTS for memory addresses. Addresses are internally latched during a write cycle.
$DQ_0 - DQ_7$	INPUT/OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during Command User Interface write cycles; outputs data during memory array, Status Register and Identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
\overline{CE}	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. \overline{CE} is active low; \overline{CE} high deselects the memory device and reduces power consumption to standby levels.
\overline{PWD}	INPUT	POWERDOWN: Puts the device in deep powerdown mode. \overline{PWD} is active low; \overline{PWD} high deselects normal operation. \overline{PWD} also locks out block erase or byte write operations when active low, providing data protection during power transitions.
\overline{OE}	INPUT	OUTPUT ENABLE: Gates the device's outputs through the data buffers during a read cycle. \overline{OE} is active low.
\overline{WE}	INPUT	WRITE ENABLE: Controls writes to the Command User Interface and array blocks. \overline{WE} is active low. Addresses and data are latched on the rising edge of the \overline{WE} pulse.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
RY/BY	OUTPUT	READY/BUSY: Indicates the status of the internal Write State Machine. When low, it indicates that the WSM is performing a block erase or byte write operation. RY/BY high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode. RY/BY is always active and does NOT float to tri-state off when the chip is deselected or data outputs are disabled.
V _{PP}		BLOCK ERASE/BYTE WRITE POWER SUPPLY for erasing blocks of the array or writing bytes of each block. Note: With V _{PP} < V _{PPLMAX} , memory contents cannot be altered.
V _{CC}		DEVICE POWER SUPPLY (3.3V ± 0.3V, 5V ± 10%)
GND		GROUND


Figure 2. TSOP Lead Configurations

28F008SA-L

INTEL CORP (MEMORY/PLD)/

56E D ■ 4826176 0077326 765 ■ ITL2

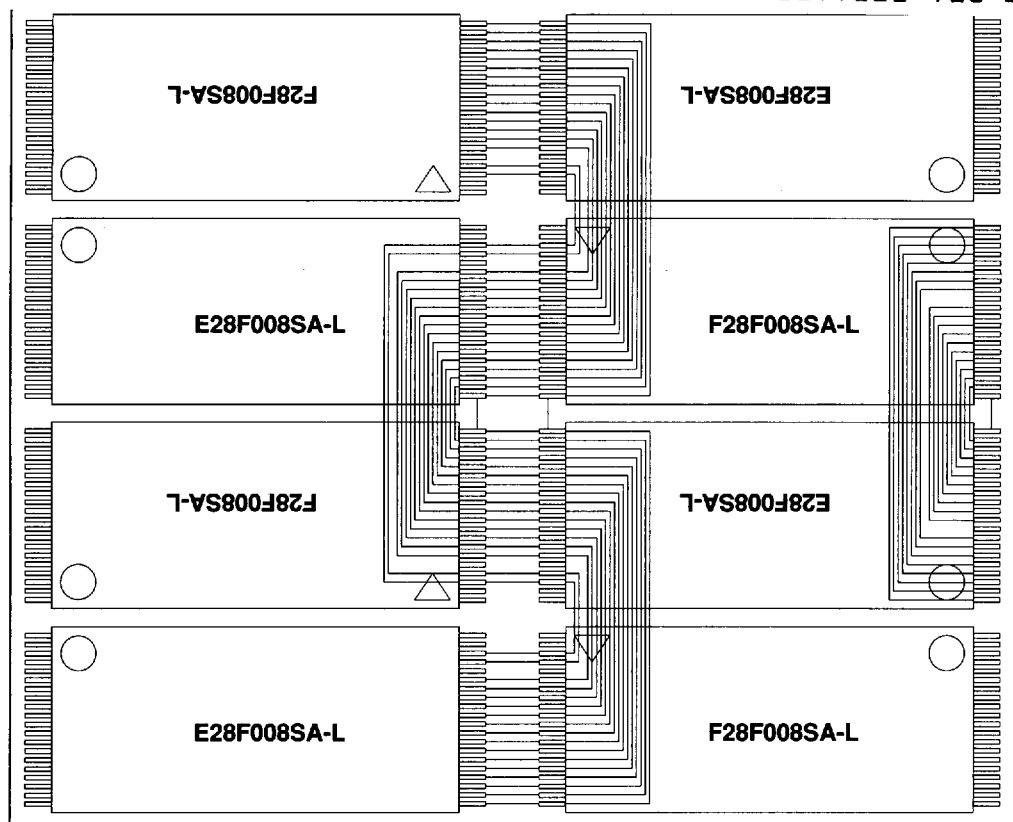


Figure 3. TSOP Serpentine Layout

NOTES:

1. Connect all V_{CC} and GND pins of each device to common power supply outputs. DO NOT leave V_{CC} or GND inputs disconnected.

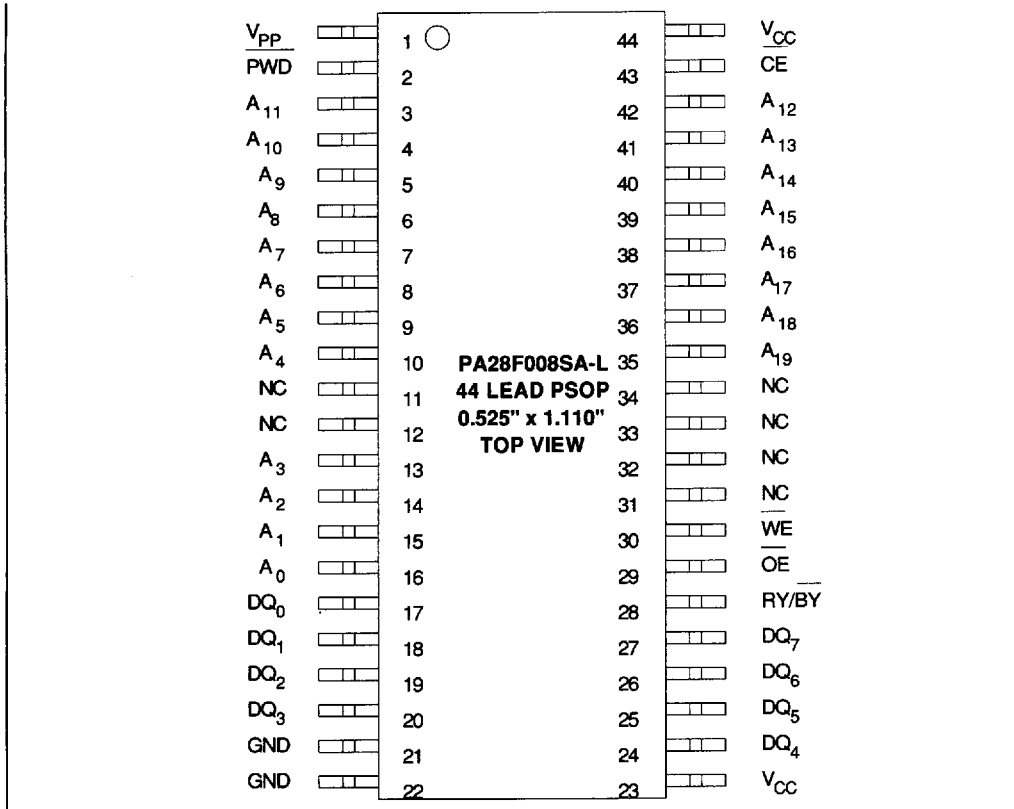


Figure 4. PSOP Lead Configuration

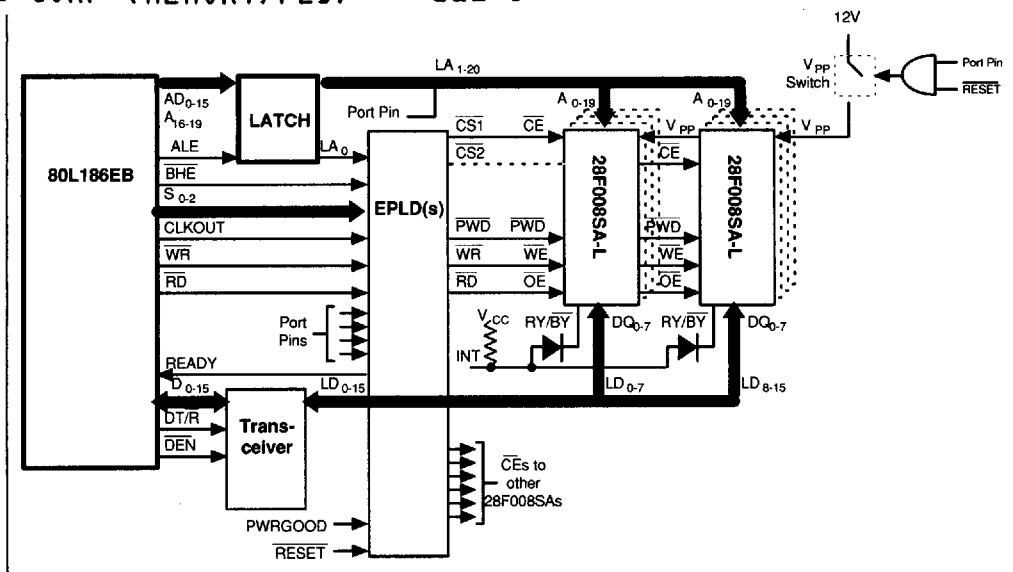


Figure 5. 28F008SA-L Array Interface to Intel 3.3V 80L186EB Embedded Microprocessor

PRINCIPLES OF OPERATION

The 28F008SA-L includes on-chip write automation to manage write and erase functions. The Write State Machine allows for: 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with RAM-like interface timings.

After initial device powerup, or after return from deep powerdown mode (see Bus Operations), the 28F008SA-L functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. Both Status Register and intelligent identifiers can also be accessed through the Command User Interface when $V_{pp}=V_{PPL}$.

This same subset of operations are also available when high voltage is applied to the V_{pp} pin. In addition, high voltage on V_{pp} enables successful block erasure and byte writing of the device. All functions associated with altering memory contents—byte write, block erase, status and intelligent identifier—are accessed via the Command User Interface and verified thru the Status Register.

Commands are written using standard microprocessor write timings. Command User Interface contents serve as input to the WSM, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations. With the appropriate command written to the Command User Interface, standard microprocessor read timings output array data, access the intelligent identifier codes, or output byte write and block erase status for verification.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the 28F008SA-L blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the 28F008SA-L are again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase to read data/execute code from other blocks.



FFFFF	64K Byte Block
F0000 EFFFF	64K Byte Block
E0000 DFFFF	64K Byte Block
D0000 CFFFF	64K Byte Block
C0000 BFFFF	64K Byte Block
B0000 AFFFF	64K Byte Block
A0000 9FFFF	64K Byte Block
90000 8FFFF	64K Byte Block
80000 7FFFF	64K Byte Block
70000 6FFFF	64K Byte Block
60000 5FFFF	64K Byte Block
50000 4FFFF	64K Byte Block
40000 3FFFF	64K Byte Block
30000 2FFFF	64K Byte Block
20000 1FFFF	64K Byte Block
10000 0FFFF	64K Byte Block
00000	64K Byte Block

Figure 6. Memory Map

Command User Interface and Write Automation

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the Status Register and RY/BY output. Byte write is similarly controlled, after destination address and expected data are supplied. The program and erase algorithms of past Intel Flash memories are now regulated by the state machine, including pulse repetition where required and internal verification and margining of data.

Data Protection

Depending on the application, the system designer may choose to make the V_{pp} power supply switchable (available only when memory byte writes/block erases are required) or hardwired to V_{PPH} . When $V_{pp}=V_{PPL}$, memory contents cannot be altered. The 28F008SA-L Command User Interface architecture provides protection from unwanted byte write or block erase operations even when high voltage is applied to V_{pp} . Additionally, all functions are disabled whenever V_{cc} is below the write lockout voltage V_{LKO} , or when PWD is at V_{IL} . The 28F008SA-L accommodates either design practice and encourages optimization of the processor-memory interface.

The two-step byte write/block erase Command User Interface write sequence provides additional software write protection.

BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Read

The 28F008SA-L has three read modes. The memory can be read from any of its blocks, and information can be read from the intelligent identifier or Status Register. V_{pp} can be at either V_{PPL} or V_{PPH} .

The first task is to write the appropriate read mode command to the Command User Interface (array, intelligent identifier, or Status Register). The 28F008SA-L automatically resets to Read Array mode upon initial device powerup or after exit from deep powerdown. The 28F008SA-L has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable (\overline{CE}) is the device selection control, and when active enables the selected memory device. Output Enable (\overline{OE}) is the data input/output (DQ_0 - DQ_7) direction control, and when active drives data from the selected memory onto the I/O bus. PWD and \overline{WE} must also be at V_{IH} . Figure 10 illustrates read bus cycle waveforms.

Output Disable

With \overline{OE} at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0 - DQ_7) are placed in a high-impedance state.

Table 2. Bus Operations

Mode	Notes	PWD	CE	OE	WE	A ₀	V _{PP}	DQ ₀₋₇	RY/BY
Read	1,2,3	V _{IH}	V _{IL}	V _{IL}	V _{IH}	X	X	D _{OUT}	X
Output Disable	3	V _{IH}	V _{IL}	V _{IH}	V _{IH}	X	X	High Z	X
Standby	3	V _{IH}	V _{IH}	X	X	X	X	High Z	X
Deep PowerDown		V _{IL}	X	X	X	X	X	High Z	V _{OH}
Intelligent Identifier (Mfr)		V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	X	89H	V _{OH}
Intelligent Identifier (Device)		V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IH}	X	A1H	V _{OH}
Write	3,4,5	V _{IH}	V _{IL}	V _{IH}	V _{IL}	X	X	D _{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{pp}=V_{PPL}$, memory contents can be read but not written or erased.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPL} or V_{PPH} for V_{PP}. See DC Characteristics for V_{PPL} and V_{PPH} voltages.
3. RY/BY is V_{OL} when the Write State Machine is executing internal block erase or byte write algorithms. It is V_{OH} when the WSM is not busy, in Erase Suspend mode or deep powerdown mode.
4. Command writes involving block erase or byte write are only successfully executed when $V_{pp}=V_{PPH}$.
5. Refer to Table 3 for valid D_{IN} during a write operation

Standby

\overline{CE} at a logic-high level (V_{IH}) places the 28F008SA-L in standby mode. Standby operation disables much of the 28F008SA-L's circuitry and substantially reduces device power consumption. The outputs (DQ₀-DQ₇) are placed in a high-impedance state independent of the status of \overline{OE} . If the 28F008SA-L is deselected during block erase or byte write, the device will continue functioning and consuming normal active power until the operation completes.

Deep Power-Down

The 28F008SA-L offers a deep powerdown feature, entered when \overline{PWD} is at V_{IL}. Current draw thru V_{CC} is 0.20 μ A typical in deep powerdown mode, with current draw through V_{PP} typically 0.1 μ A. During read modes, \overline{PWD} -low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The 28F008SA-L requires time t_{PHQV} (see AC Characteristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command User Interface is reset to Read Array, and the Status Register is cleared to value 80H, upon return to normal operation.

During block erase or byte write modes, \overline{PWD} low will abort either operation. Memory contents of the

block being altered are no longer valid as the data will be partially written or erased. Time t_{PHWL} after \overline{PWD} goes to logic-high (V_{IH}) is required before another command can be written.

Intelligent Identifier Operation

The intelligent identifier operation outputs the manufacturer code, 89H; and the device code, A1H for the 28F008SA-L. The system CPU can then automatically match the device with its proper block erase and byte write algorithms.

The manufacturer- and device-codes are read via the Command User Interface. Following a write of 90H to the Command User Interface, a read from address location 00000H outputs the manufacturer code (89H). A read from address 00001H outputs the device code (A1H). It is not necessary to have high voltage applied to V_{PP} to read the intelligent identifiers from the Command User Interface.

Write

Writes to the Command User Interface enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register. Additionally, when $V_{pp}=V_{PPH}$, the Command User Interface controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.



ADVANCE INFORMATION

28F008SA-L

INTEL CORP (MEMORY/PLD)/

56E D

4826176 0077331 022 ITL2

Table 3. Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Operation	Address	Data	Operation	Address	Data
Read Array/Reset	1	1	Write	X	FFH			
Intelligent Identifier	3	2,3,4	Write	X	90H	Read	IA	IID
Read Status Register	2	3	Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Erase Setup/Erase Confirm	2	2	Write	BA	20H	Write	BA	D0H
Erase Suspend/Erase Resume	2		Write	X	B0H	Write	X	D0H
Byte Write Setup/Write	2	2,3,5	Write	WA	40H	Write	WA	WD
Alternate Byte Write Setup/Write	2	2,3,5	Write	WA	10H	Write	WA	WD

NOTES:

1. Bus operations are defined in Table 2.
2. IA = Identifier Address: 00H for manufacturer code, 01H for device code.
BA = Address within the block being erased.
WA = Address of memory location to be written.
3. SRD = Data read from Status Register. See table 4 for a description of the Status Register bits.
WD = Data to be written at location WA. Data is latched on the rising edge of WE.
IID = Data read from intelligent identifiers.
4. Following the intelligent identifier command, two read operations access manufacturer and device codes.
5. Either 40H or 10H are recognized by the WSM as the Byte Write Setup command.
6. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

The Command User Interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The Command User Interface is written by bringing WE to a logic-low level (V_{LL}) with CE low. Addresses and data are latched on WE's rising edge. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operations, figure 11, for specific timing parameters.

COMMAND DEFINITIONS

When V_{PPL} is applied to the V_{PP} pin, read operations

from the Status Register, intelligent identifiers, or array blocks are enabled. Placing V_{PPH} on V_{PP} enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands to the Command User Interface. Table 3 defines the 28F008SA-L commands.

Read Array Command

Upon initial device powerup and after exit from deep powerdown mode, the 28F008SA-L defaults to Read Array mode. This operation is also initiated by writing FFH to the Command User Interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the Command User Interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when $V_{PP}=V_{PPL}$ or V_{PPH} .

Table 4. Status Register Definitions

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTES:

SR.7 = WRITE STATE MACHINE STATUS
 1 = Ready
 0 = Busy

SR.6 = ERASE SUSPEND STATUS
 1 = Erase Suspended
 0 = Erase In Progress/Completed

SR.5 = ERASE STATUS
 1 = Error in Block Erasure
 0 = Successful Block Erase

SR.4 = BYTE WRITE STATUS
 1 = Error in Byte Write
 0 = Successful Byte Write

SR.3 = V_{PP} STATUS
 1 = V_{PP} Low Detect; Operation Abort
 0 = V_{PP} OK

SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS
 These bits are reserved for future use and should be masked out when polling the Status Register.

RY/BY or the Write State Machine Status bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bits are checked for success.

If the Byte Write AND Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.

If V_{PP} low status is detected, the Status Register must be cleared before another byte write or block erase operation is attempted.

The V_{PP} Status bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been entered and informs the system if V_{PP} has not been switched 0. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH} .

Intelligent Identifier Command

The 28F008SA-L contains an intelligent identifier operation, initiated by writing 90H to the Command User Interface. Following the command write, a read cycle from address 00000H retrieves the manufacturer code of 89H. A read cycle from address 00001H returns the device code of A1H. To terminate the operation, it is necessary to write another valid command to the Command User Interface. Like the Read Array command, the intelligent identifier command is functional when $V_{PP}=V_{PPL}$ or V_{PPH} .

Read Status Register Command

The 28F008SA-L contains a Status Register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status Register command (70H) to the Command User Interface. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface. The contents of the Status Register are latched on

the falling edge of \overline{OE} or \overline{CE} , whichever occurs last in the read cycle. \overline{OE} or \overline{CE} must be toggled to V_{IH} before further reads to update the Status Register latch. The Read Status Register command functions when $V_{PP}=V_{PPL}$ or V_{PPH} .

Clear Status Register Command

The Erase Status and Byte Write Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register Command. These bits indicate various failure conditions (see Table 4). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (SR.3) MUST be reset by system software before further byte writes or block erases are attempted. To clear the Status Register, the Clear Status Register command (50H) is written to the Command User Interface. The Clear Status Register command is functional when $V_{PP}=V_{PPL}$ or V_{PPH} .



Erase Setup/Erase Confirm Commands

Erase is executed one block at a time, initiated by a two-cycle command sequence. An Erase Setup command (20H) is first written to the Command User Interface, followed by the Erase Confirm command (D0H). These commands require both appropriate sequencing and an address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two-command erase sequence is written to it, the 28F008SA-L automatically outputs Status Register data when read (see figure 8; Block Erase Flowchart). The CPU can detect the completion of the erase event by analyzing the output of the RY/ $\overline{\text{BY}}$ pin, or the WSM Status bit of the Status Register.

When erase is completed, the Erase Status bit should be checked. If erase error is detected, the Status Register should be cleared. The Command User Interface remains in Read Status Register mode until further commands are issued to it.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, reliable block erasure can only occur when $V_{PP} = V_{PPH}$. In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} Status bit will be set to "1". Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the Erase Suspend command (B0H) to the Command User Interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The 28F008SA-L continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended (both will be set to "1"). RY/ $\overline{\text{BY}}$ will also transition to V_{OH} .

At this point, a Read Array command can be written to the Command User Interface to read data from blocks **other than that which is suspended**. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H), at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and RY/ $\overline{\text{BY}}$ will return to V_{OL} . After the Erase Resume command is written to it, the 28F008SA-L automatically outputs Status Register data when read (see figure 9; Erase Suspend/Resume Flowchart). V_{PP} must remain at V_{PPH} while the 28F008SA-L is in Erase Suspend.

Byte Write Setup/Write Commands

Byte write is executed by a two-command sequence. The Byte Write Setup command (40H) is written to the Command User Interface, followed by a second write specifying the address and data (latched on the rising edge of WE) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two-command byte write sequence is written to it, the 28F008SA-L automatically outputs Status Register data when read (see figure 7; Byte Write Flowchart). The CPU can detect the completion of the byte write event by analyzing the output of the RY/ $\overline{\text{BY}}$ pin, or the WSM Status bit of the Status Register. Only the Read Status Register command is valid while byte write is active.

When byte write is complete, the Byte Write Status bit should be checked. If byte write error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The Command User Interface remains in Read Status Register mode until further commands are issued to it. If byte write is attempted while $V_{PP} = V_{PPL}$, the V_{PP} Status bit will be set to "1". Byte write attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and should not be attempted.

EXTENDED BLOCK ERASE/BYTE WRITE CYCLING

Intel has designed extended cycling capability into its ETOX flash memory technologies. The 28F008SA-L is designed for 10,000 byte write/block erase cycles on each of the sixteen 64K-byte blocks. Low electric fields, advanced oxides and minimal oxide area per cell subjected to the tunneling electric field combine to greatly reduce oxide stress and the probability of failure. A 20 Mbyte solid-state drive using an array of 28F008SA-Ls has a cycling MTBF (Mean Time Between Failure) of 3.33 million hours⁽¹⁾, over 33 times more reliable than equivalent rotating disk technology.

AUTOMATED BYTE WRITE

The 28F008SA-L integrates the Quick-Pulse programming algorithm of prior Intel Flash devices on-chip, using the Command User Interface, Status Register and Write State Machine (WSM). On-chip integration dramatically simplifies system software and provides processor interface timings to the Command User Interface and Status Register. WSM operation, internal verify and V_{pp} high voltage presence are monitored and reported via the RY/BY output and appropriate Status Register bits. Figure 7 shows a system software flowchart for device byte write. The entire sequence is performed with V_{pp} at V_{ppH} . Byte write abort occurs when PWD transitions to V_{IL} or V_{pp} drops to V_{pPL} . Although the WSM is halted, byte data is partially written at the location where byte write was aborted. Block erasure is required to initialize this data to a known value.

AUTOMATED BLOCK ERASE

As above, the Quick-Erase algorithm of prior Intel Flash devices is now implemented internally, including all preconditioning of block data. WSM operation, erase success and V_{pp} high voltage presence are monitored and reported through RY/BY and the Status Register. Additionally, if a command other than Erase Confirm is written to the device following Erase Setup, both the Erase Status and Byte Write Status bits will be set to "1"s. When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 8 shows a system software flowchart for block erase.

Erase typically takes 2.0 seconds per block. The Erase Suspend/Erase Resume command sequence allows suspension of this erase operation to read data from a block other than that in which erase is being performed. A system software flowchart is shown in Figure 9.

The entire sequence is performed with V_{pp} at V_{ppH} . Abort occurs when PWD transitions to V_{IL} or V_{pp} falls to V_{pPL} , while erase is in progress. Block data is partially erased by this operation, and a repeat of erase is required to obtain a fully erased block.

DESIGN CONSIDERATIONS

Three-Line Output Control

The 28F008SA-L will often be used in large memory arrays. Intel provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- a) lowest possible memory power dissipation
- b) complete assurance that data bus contention will not occur

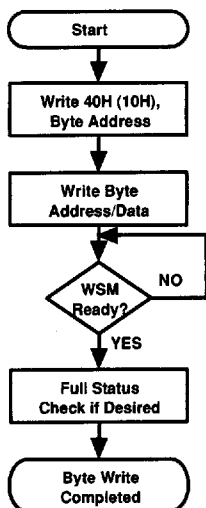
To efficiently use these control inputs, an address decoder should enable \overline{CE} , while \overline{OE} should be connected to all memory devices and the system's READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode. Finally, PWD should either be tied to the system \overline{RESET} , or connected to V_{cc} if unused.

RY/ \overline{BY} and Byte Write/Block Erase Polling

RY/ \overline{BY} is a full CMOS output that provides a hardware method of detecting byte write and block erase completion. It transitions low time t_{WHRL} after a write or erase command sequence is written to the 28F008SA-L, and returns to V_{OH} when the WSM has finished executing the internal algorithm.

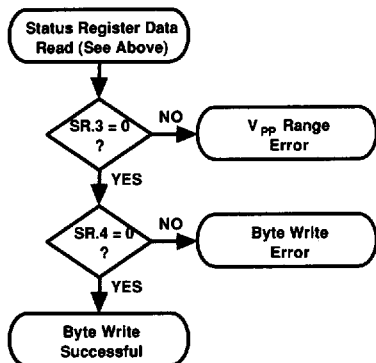
RY/ \overline{BY} can be connected to the interrupt input of the system CPU or controller. It is active at all times, not tristated if the 28F008SA-L \overline{CE} or \overline{OE} inputs are brought to V_{IH} . RY/ \overline{BY} is also V_{OH} when the device is in Erase Suspend or deep powerdown modes.

⁽¹⁾Assumptions: 10Kbyte file written every 10 minutes. (20Mbyte array)/(10Kbyte file) = 2,000 file writes before erase required. (2000 file writes/erase) x (10,000 cycles per 28F008SA block) = 20 million file writes. (20x10⁶ file writes) x (10 min/write) x (1hr/60 min) = 3.3x10⁶ MTBF



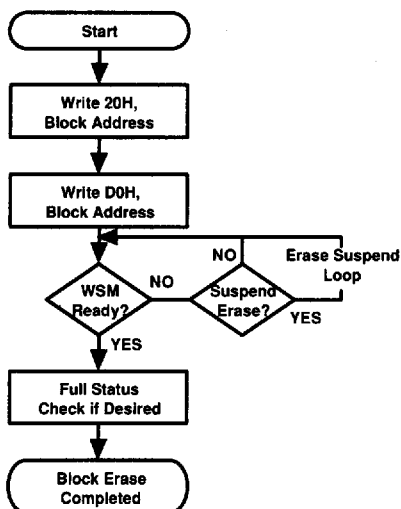
Bus Operation	Command	Comments
Write	Setup Byte Write	Data = 40H (10H) Address = Byte to be written
Write	Byte Write	Data to be written Address = Byte to be written
Standby/Read		Check RY/BY V _{OH} Ready, V _{OL} = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE or CE to update Status Register
Repeat for subsequent bytes		
Full status check can be done after each byte or after a sequence of bytes		
Write FFH after the last byte write operation to reset the device to Read Array Mode		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check SR.3 1 = V _{pp} Low Detect
Standby		Check SR.4 1 = Byte Write Error
SR.3 MUST be cleared, if set during a byte write attempt, before further attempts are allowed by the Write State Machine		
SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are written before full status is checked.		
If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 7. Automated Byte Write Flowchart



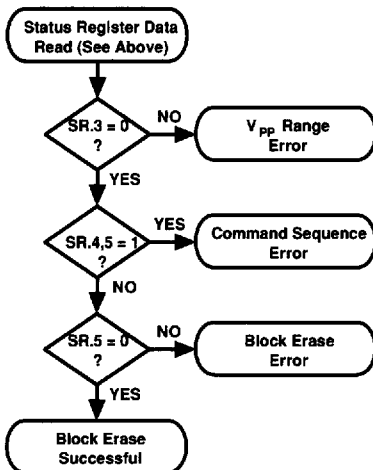
Bus Operation	Command	Comments
Write	Setup Erase	Data = 20H Address = Within block to be erased
Write	Erase	Data = D0H Address = Within block to be erased
Standby/Read		Check RY/BY $V_{\alpha T}$ Ready, $V_{\alpha L}$ Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE or CE to update Status Register

Repeat for subsequent blocks

Full status check can be done after each block or after a sequence of blocks

Write FFH after the last block erase operation to reset the device to Read Array Mode

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check SR.3 1 = V_{pp} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 8. Automated Block Erase Flowchart



ADVANCE INFORMATION

28F008SA-L

INTEL CORP (MEMORY/PLD/

56E D ■ 4826176 0077337 540 ■ ITL2

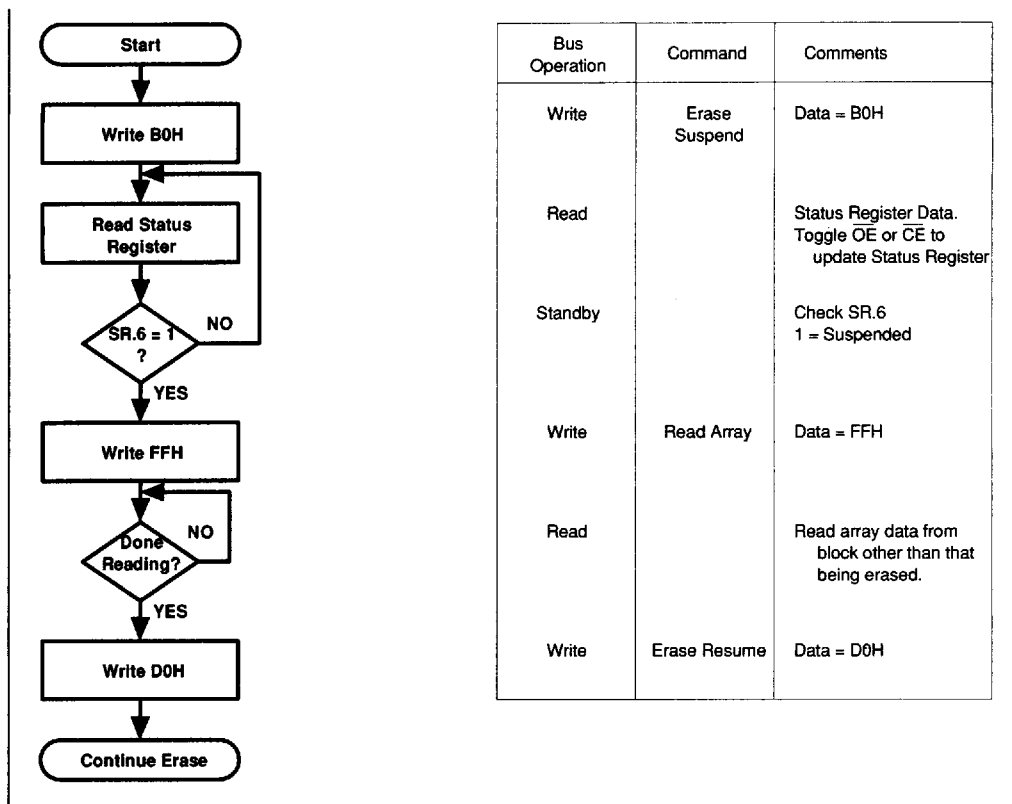


Figure 9. Erase Suspend/Resume Flowchart

INTEL CORP (MEMORY/PLD)/ Power Supply Decoupling

56E D ■ 4826176 0077338 487 ■ ITL2

 V_{CC} transitions below V_{LKO} is Read Array Mode.

Flash memory power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues; standby current levels (I_{SB}), active current levels (I_{CC}) and transient peaks produced by falling and rising edges of \overline{CE} . Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, low inherent-inductance capacitors should be placed as close as possible to package leads. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

V_{PP} Trace on Printed Circuit Boards

Writing flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for writing and erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{CC} , V_{PP} , PWD Transitions and the Command User Interface/Status Register

Byte write and block erase completion are not guaranteed if V_{PP} drops below V_{PPH} . If the V_{PP} Status bit of the Status Register (SR.3) is set to "1", a Clear Status Register command MUST be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (SR.4) or Erase (SR.5) Status bits of the Status Register will be set to "1" if error is detected. PWD transitions to V_{IL} during byte write and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device poweroff, or PWD transitions to V_{IL} , clear the Status Register to initial value 80H.

The Command User Interface latches commands as issued by system software and is not altered by V_{PP} or \overline{CE} transitions or WSM actions. Its state upon powerup, after exit from deep powerdown or after

After byte write or block erase is complete, even after V_{PP} transitions down to V_{PPL} , the Command User Interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

Power Up/Down Protection

The 28F008SA-L is designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the 28F008SA-L is indifferent as to which power supply, V_{PP} or V_{CC} , powers up first. Power supply sequencing is not required. Internal circuitry in the 28F008SA-L ensures that the Command User Interface resets to Read Array mode on powerup.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both \overline{WE} and \overline{CE} must be low for a command write, driving either to V_{IH} will inhibit writes. The Command User Interface architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

Finally, the device is disabled until PWD is brought to V_{IH} , regardless of the state of its control inputs. This provides an additional level of memory protection.

Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases usable battery life, because the 28F008SA-L does not consume any power to retain code or data when the system is off.

In addition, the 28F008SA-L's deep powerdown mode ensures extremely low power dissipation even when system power is applied. For example, portable PCs and other power sensitive applications, using an array of 28F008SA-Ls for solid-state storage, can lower PWD to V_{IL} in standby or sleep modes, producing negligible power consumption. If access to the 28F008SA-L is again needed, the part can again be read, following the t_{PHOV} and t_{PHWL} wakeup cycles required after PWD is first raised back to V_{IH} . See AC Characteristics-Read-Only/Write and Figures 10/11 for more information.



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature

During Read.....0°C to 70°C⁽¹⁾

During Block Erase/Byte Write.....0°C to 70°C

Temperature Under Bias.....-10°C to 80°C

Storage Temperature.....-65°C to 125°C

Voltage on Any Pin

(except V_{CC} and V_{PP})with Respect to GND.....-2.0V to 7.0V⁽²⁾ V_{PP} Program Voltage

with Respect to GND

During Block Erase/Byte Write....-2.0V to 14.0V^(2,3) V_{CC} Supply Voltagewith Respect to GND.....-2.0V to 7.0V⁽²⁾Output Short Circuit Current.....100 mA⁽⁴⁾

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20ns. Maximum DC voltage on input/output pins is $V_{CC} + 0.5V$ which, during transitions, may overshoot to $V_{CC} + 2.0V$ for periods < 20ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods < 20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.

OPERATING CONDITIONS

Symbol	Parameter	Notes	Min	Max	Unit
T_A	Operating Temperature		0	70	°C
V_{CC}	V_{CC} Supply Voltage	5	3.00	3.60	V
V_{CC}	V_{CC} Supply Voltage	5	4.50	5.50	V

DC CHARACTERISTICS $V_{CC} = 3.3V \pm 0.3V$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	1			± 0.5	μA	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$
I_{LO}	Output Leakage Current	1			± 0.5	μA	$V_{CC} = V_{CC} \text{ Max}$ $V_{OUT} = V_{CC} \text{ or GND}$
I_{CCS}	V_{CC} Standby Current	1,3		20	50	μA	$V_{CC} = V_{CC} \text{ Max}$ $\overline{CE} = \overline{PWD} = V_{CC} \pm 0.2V$
				30	100	μA	$V_{CC} = V_{CC} \text{ Max}$ $\overline{CE} = \overline{PWD} = V_{IH}$
I_{CCD}	V_{CC} Deep PowerDown Current	1		0.20	1.0	μA	$\overline{PWD} = \text{GND} \pm 0.2V$ $I_{OUT} (\text{RY}/\text{BY}) = 0 \text{ mA}$
I_{CCR}	V_{CC} Read Current	1		5	12	mA	$V_{CC} = V_{CC} \text{ Max}$, $\overline{CE} = \text{GND}$ $f = 5 \text{ MHz}$, $I_{OUT} = 0 \text{ mA}$ CMOS Inputs
				5	12	mA	$V_{CC} = V_{CC} \text{ Max}$, $\overline{CE} = V_{IL}$ $f = 5 \text{ MHz}$, $I_{OUT} = 0 \text{ mA}$ TTL Inputs

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Notice: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

DC CHARACTERISTICS $V_{CC} = 3.3V \pm 0.3V$ (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{CCW}	V_{CC} Byte Write Current	1		6	18	mA	Byte Write In Progress
I_{CCE}	V_{CC} Block Erase Current	1		6	18	mA	Block Erase In Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	6	mA	Block Erase Suspended, $CE = V_{IH}$
I_{PPS}	V_{PP} Standby Current	1		± 1	± 10	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep PowerDown Current	1		0.10	5.0	μA	$PWD = GND \pm 0.2V$
I_{PPR}	V_{PP} Read Current	1		90	200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Byte Write Current	1		10	30	mA	$V_{PP} = V_{PPH}$ Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current	1		10	30	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		90	200	μA	$V_{PP} = V_{PPH}$ Block Erase Suspended
V_{IL}	Input Low Voltage		-0.5		0.6	V	
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage	3			0.4	V	$V_{CC} = V_{CC} \text{ Min}$ $I_{OL} = 2 \text{ mA}$
V_{OH}	Output High Voltage	3	2.4			V	$V_{CC} = V_{CC} \text{ Min}$ $I_{OH} = -2 \text{ mA}$
V_{PPL}	V_{PP} during Normal Operations	4	0.0		6.5	V	
V_{PPH}	V_{PP} during Erase/Write Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.2			V	

CAPACITANCE⁽⁵⁾ $T_A = 25^\circ C$, $f = 1 \text{ MHz}$

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 3.3V$, $V_{PP} = 12.0V$, $T = 25^\circ C$. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the 28F008SA-L is read while in Erase Suspend Mode, current draw is the sum of I_{CCES} and I_{CCR} .
3. Includes RY/BY.
4. Block Erases/Byte Writes are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL} .
5. Sampled, not 100% tested.



INTEL CORP (MEMORY/PLD) 56E D 4826176 0077341 T71 ITL2
DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	1			± 1.0	μA	$V_{CC} = V_{CC} \text{ Max}$ $V_{IN} = V_{CC} \text{ or GND}$
I_{LO}	Output Leakage Current	1			± 10	μA	$V_{CC} = V_{CC} \text{ Max}$ $V_{OUT} = V_{CC} \text{ or GND}$
I_{CCS}	V_{CC} Standby Current	1,3		1.0	2.0	mA	$V_{CC} = V_{CC} \text{ Max}$ $CE = PWD = V_{IH}$
				30	100	μA	$V_{CC} = V_{CC} \text{ Max}$ $CE = PWD = V_{CC} \pm 0.2V$
I_{CCD}	V_{CC} Deep PowerDown Current	1		0.20	1.2	μA	$PWD = GND \pm 0.2V$ $I_{OUT} (RY/BY) = 0 \text{ mA}$
I_{CCR}	V_{CC} Read Current	1		20	35	mA	$V_{CC} = V_{CC} \text{ Max}, CE = GND$ $f = 5 \text{ MHz}, I_{OUT} = 0 \text{ mA}$ CMOS Inputs
				25	50	mA	$V_{CC} = V_{CC} \text{ Max}, CE = V_{IL}$ $f = 5 \text{ MHz}, I_{OUT} = 0 \text{ mA}$ TTL Inputs
I_{CCW}	V_{CC} Byte Write Current	1		10	30	mA	Byte Write In Progress
I_{CCE}	V_{CC} Block Erase Current	1		10	30	mA	Block Erase In Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		5	10	mA	Block Erase Suspended, $CE = V_{IH}$
I_{PPS}	V_{PP} Standby Current	1		± 1	± 10	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep PowerDown Current	1		0.10	5.0	μA	$PWD = GND \pm 0.2V$
I_{PPR}	V_{PP} Read Current	1		90	200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Byte Write Current	1		10	30	mA	$V_{PP} = V_{PPH}$ Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current	1		10	30	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		90	200	μA	$V_{PP} = V_{PPH}$ Block Erase Suspended
V_{IL}	Input Low Voltage		-0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage	3			0.45	V	$V_{CC} = V_{CC} \text{ Min}$ $I_{OL} = 5.8 \text{ mA}$
V_{OH}	Output High Voltage	3	2.4			V	$V_{CC} = V_{CC} \text{ Min}$ $I_{OH} = -2.5 \text{ mA}$

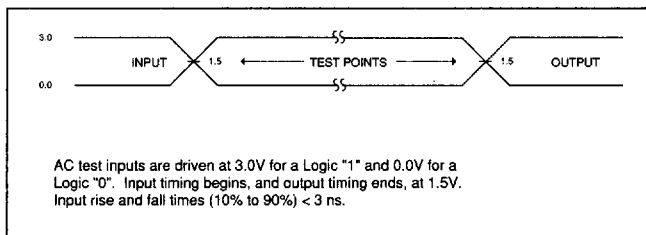
INTEL CORP (MEMORY/PLD)/ 56E D ■ 4826176 0077342 908 ■ ITL2
DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$ (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
V_{PPL}	V_{PP} during Normal Operations	4	0.0		6.5	V	
V_{PPH}	V_{PP} during Erase/Write Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.2			V	

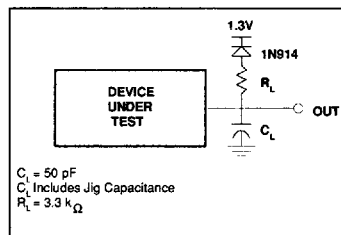
NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0V$, $V_{PP} = 12.0V$, $T = 25^\circ C$. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the 28F008SA-L is read while in Erase Suspend Mode, current draw is the sum of I_{CCES} and I_{CCR} .
3. Includes RY/BY.
4. Block Erases/Byte Writes are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL} .

AC INPUT/OUTPUT REFERENCE WAVEFORM



AC TESTING LOAD CIRCUIT



AC CHARACTERISTICS-Read-Only Operations⁽¹⁾ $V_{CC} = 3.3V \pm 0.3V$, $5.0V \pm 10\%$

Versions			28F008SA-L200		28F008SA-L250		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	
t_{AVAV} t_{RC}	Read Cycle Time		200		250		ns
t_{AVQV} t_{ACC}	Address to Output Delay			200		250	ns
t_{ELQV} t_{CE}	\overline{CE} to Output Delay	2		200		250	ns
t_{PHQV} t_{PWH}	\overline{PWD} High to Output Delay			500		500	ns
t_{GLQV} t_{OE}	\overline{OE} to Output Delay	2		85		85	ns
t_{ELQX} t_{LZ}	\overline{CE} to Output Low Z	3	0		0		ns
t_{EHQZ} t_{HZ}	\overline{CE} High to Output High Z	3		55		55	ns
t_{GLOX} t_{OLZ}	\overline{OE} to Output Low Z	3	0		0		ns
t_{GHQZ} t_{DF}	\overline{OE} High to Output High Z	3		30		30	ns
	t_{OH} Output Hold from Addresses, \overline{CE} or \overline{OE} Change, Whichever is First	3	0		0		ns

NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
3. Sampled, not 100% tested.



AC CHARACTERISTICS-Write Operations⁽¹⁾ $V_{CC} = 3.3V \pm 0.3V, 5.0V \pm 10\%$

Versions				28F008SA-L200		28F008SA-L250		Unit
Symbol		Parameter	Notes	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		200		250		ns
t_{PHWL}	t_{PS}	PWD High Recovery to \overline{WE} Going Low	2	1		1		μs
t_{ELWL}	t_{CS}	\overline{CE} Setup to \overline{WE} Going Low		20		20		ns
t_{WLWH}	t_{WP}	\overline{WE} Pulse Width		60		60		ns
t_{VPWH}	t_{VPS}	V_{PP} Setup to \overline{WE} Going High	2	100		100		ns
t_{AVWH}	t_{AS}	Address Setup to \overline{WE} Going High	3	60		60		ns
t_{DVWH}	t_{DS}	Data Setup to \overline{WE} Going High	4	60		60		ns
t_{WHDX}	t_{DH}	Data Hold from \overline{WE} High		5		5		ns
t_{WHAX}	t_{AH}	Address Hold from \overline{WE} High		5		5		ns
t_{WHEH}	t_{CH}	\overline{CE} Hold from \overline{WE} High		10		10		ns
t_{WHWL}	t_{WPH}	\overline{WE} Pulse Width High		30		30		ns
t_{WHRL}		\overline{WE} High to RY/\overline{BY} Going Low			100		100	ns
t_{WHQV1}		Duration of Byte Write Operation	5,6	6		6		μs
t_{WHQV2}		Duration of Block Erase Operation	5,6	0.3		0.3		sec
t_{WHGL}		Write Recovery before Read		0		0		μs
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD, RY/\overline{BY} High	2,6	0		0		ns

NOTES:

1. Read timing characteristics during erase and byte write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Sampled, not 100% tested.
3. Refer to table 3 for valid A_{IN} for byte write or block erasure.
4. Refer to table 3 for valid D_{IN} for byte write or block erasure.
5. The on-chip Write State Machine incorporates all byte write and block erase system functions and overhead of standard Intel flash memory, including byte program and verify (byte write) and block precondition, precondition verify, erase and erase verify (block erase).
6. Byte write and block erase durations are measured to completion ($SR.7=1, RY/\overline{BY}=V_{OH}$). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success ($SR.3/4/5=0$).



28F008SA-L

INTEL CORP (MEMORY/PLD) / 56E D ■ 4826176 0077345 617 ■ ITL2
BLOCK ERASE AND BYTE WRITE PERFORMANCE $V_{CC} = 3.3V \pm 0.3V, 5.0V \pm 10\%$

Parameter	Notes	28F008SA-L200			28F008SA-L250			Unit
		Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max	
Block Erase Time	2		2.0	12.5		2.0	12.5	Sec
Block Write Time	2		0.7	2.6		0.7	2.6	Sec

NOTES:

1. 25 °C, 12.0 V_{pp} .
2. Excludes System-Level Overhead.

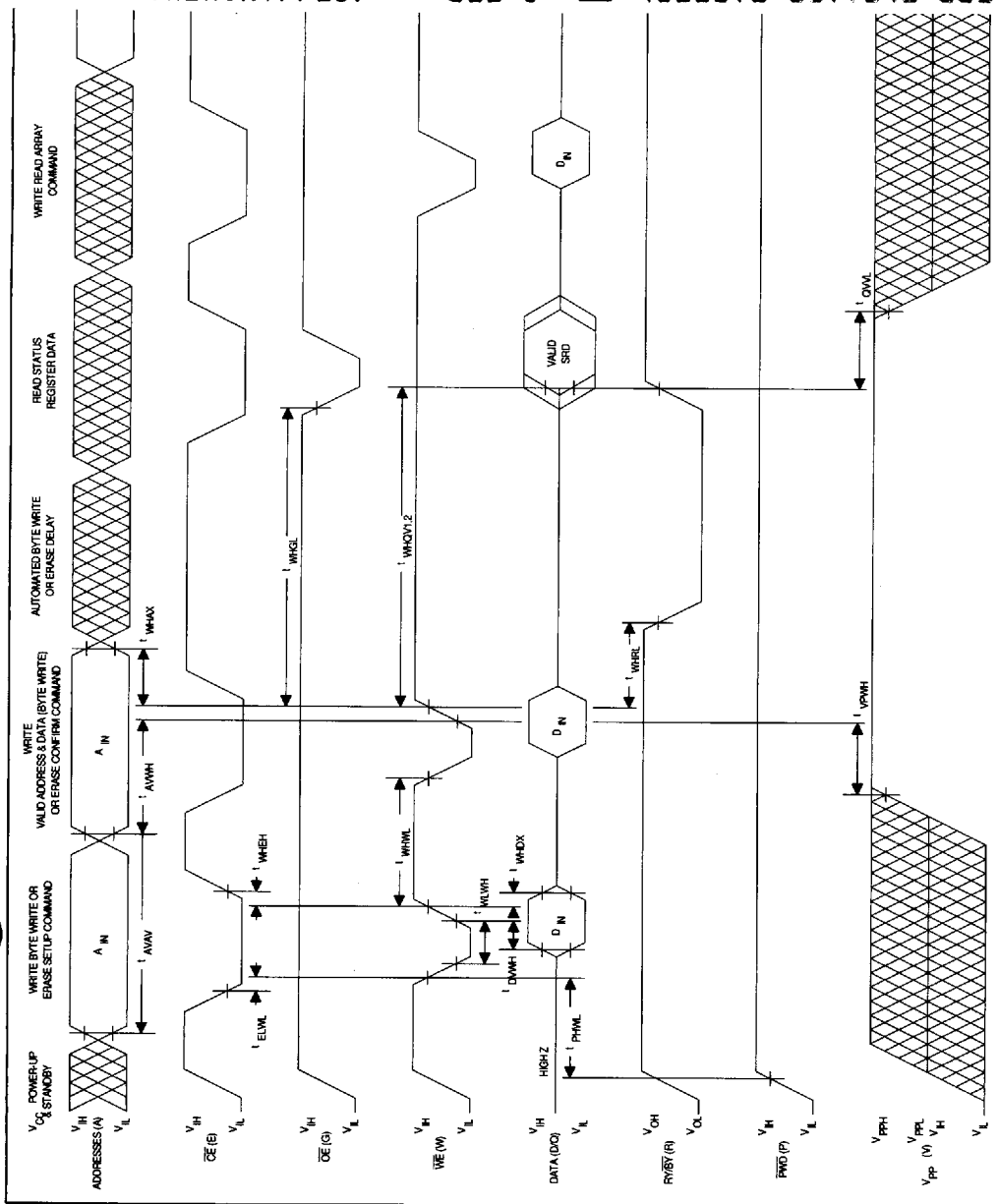


Figure 11. AC Waveform for Write Operations


ALTERNATIVE CE-CONTROLLED WRITES $V_{CC} = 3.3V \pm 0.3V, 5.0V \pm 10\%$

Versions				28F008SA-L200		28F008SA-L250		Unit
Symbol		Parameter	Notes	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		200		250		ns
t_{PHEL}	t_{PS}	PWD High Recovery to \overline{CE} Going Low	2	1		1		μs
t_{WLEL}	t_{WS}	\overline{WE} Setup to \overline{CE} Going Low		0		0		ns
t_{ELEH}	t_{CP}	\overline{CE} Pulse Width		70		70		ns
t_{VPEH}	t_{VPS}	V_{PP} Setup to \overline{CE} Going High	2	100		100		ns
t_{AVEH}	t_{AS}	Address Setup to \overline{CE} Going High	3	60		60		ns
t_{DVEH}	t_{DS}	Data Setup to \overline{CE} Going High	4	60		60		ns
t_{EHDH}	t_{DH}	Data Hold from \overline{CE} High		5		5		ns
t_{EHAX}	t_{AH}	Address Hold from \overline{CE} High		5		5		ns
t_{EHWL}	t_{WH}	\overline{WE} Hold from \overline{CE} High		0		0		ns
t_{EHEL}	t_{EPH}	\overline{CE} Pulse Width High		25		25		ns
t_{EHRL}		\overline{CE} High to RY/\overline{BY} Going Low			100		100	ns
t_{EHQV1}		Duration of Byte Write Operation	5	6		6		μs
t_{EHQV2}		Duration of Block Erase Operation	5	0.3		0.3		sec
t_{EHGL}		Write Recovery before Read		0		0		μs
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD, RY/\overline{BY} High	2,5	0		0		ns

NOTES:

1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of \overline{CE} and \overline{WE} . In systems where \overline{CE} defines the write pulsewidth (within a longer \overline{WE} timing waveform), all setup, hold and inactive \overline{WE} times should be measured relative to the \overline{CE} waveform.
2. Sampled, not 100% tested.
3. Refer to table 3 for valid A_{IN} for byte write or block erasure.
4. Refer to table 3 for valid D_{IN} for byte write or block erasure.
5. Byte write and block erase durations are measured to completion (SR.7=1, $RY/\overline{BY}=V_{OH}$). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5=0).

INTEL CORP (MEMORY/PLD)/

56E D ■ 4826176 0077348 326 ■ ITL2

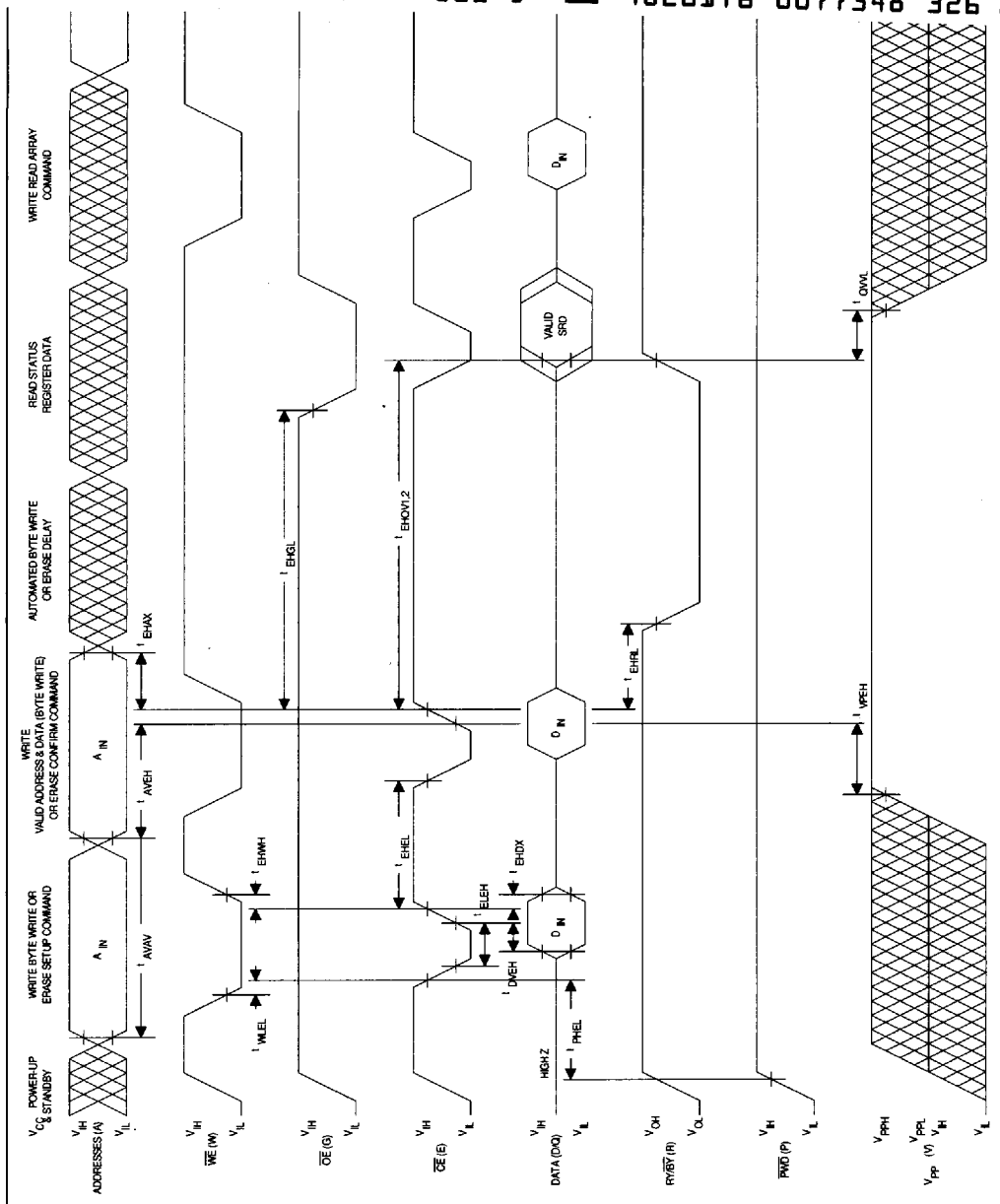


Figure 12. Alternate AC Waveform for Write Operations



ADVANCE INFORMATION

INTEL CORP (MEMORY/PLD)/
ORDERING INFORMATION

28F008SA-L

T-46-13-26

56E D 4826176 0077349 262 ITL2

E	2	8	F	0	0	8	S	A	-	L	2	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---

PACKAGE

E = STANDARD 40 LEAD TSOP

F = REVERSE 40 LEAD TSOP

PA = 44 LEAD PSOP

3.3V

ACCESS SPEED (ns)

200 ns

250 ns

VALID COMBINATIONS:

E28F008SA-L200

F28F008SA-L200

PA28F008SA-L200

E28F008SA-L250

F28F008SA-L250

PA28F008SA-L250

ADDITIONAL INFORMATION

28F008SA Datasheet
AP-359 "28F008SA Hardware Interfacing"
AP-360 "28F008SA Software Drivers"
ER-27 "The Intel 28F008SA Flash Memory"
ER-28 "ETOX™-III Flash Memory Technology"

Order Number

290429
292094
292095
294011
294012

REVISION HISTORY

Number	Description
-001	Original Version



UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119 • Tel: (408) 765-8080

Printed in USA/E582/492/20K/CC/MS
Memory Products