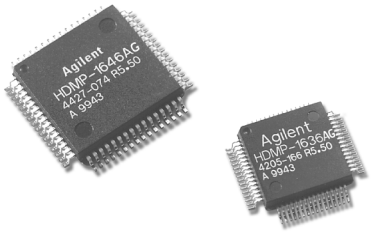
HDMP-1636AG

Gigabit Ethernet and Fibre Channel SerDes ICs

Data Sheet



HDMP-1636AG Transceiver
HDMP-1646AG Transceiver
HDMP-T1636AG Transceiver

Description

The HDMP-1636AG/46AG/T1636AG transceiver is a single integrated circuit packaged in a plastic QFP package. It provides a low-cost, low-power physical layer solution for 1250 MBd Gigabit Ethernet, 1062.5 MBd Fibre Channel, and proprietary link interfaces. It provides complete Serialize/Deserialize (SerDes) for copper transmission, incorporating the Gigabit Ethernet/Fibre Channel transmit and receive functions into a single device.

This chip is used to build a high speed interface (as shown in Figure 1) while minimizing board space, power and cost. It is compatible with the IEEE 802.3z specification.

The transmitter section accepts 10-bit wide parallel TTL data and serializes this data into a high speed serial data stream. The parallel data is expected to be “8B/10B” encoded data, or equivalent. This parallel data is latched into the input register of the transmitter section on the rising edge of the reference clock (used as the transmit byte clock). A 1062.5 MHz reference clock is used in Fibre Channel operation, whereas a 125 MHz reference clock is used in Gigabit Ethernet operation.

The transmitter section’s PLL locks to the user supplied reference byte clock. This clock is then multiplied by 10 to generate the high speed serial clock used to generate the high speed output. The high speed outputs are capable of inter-facing directly to copper cables for electrical transmission or to a separate fiber optic module for optical transmission.

Features

- **IEEE 802.3z gigabit ethernet compatible**
- **ANSI x3.230-1994 fibre channel compatible (FC-0)**
- **Supports serial data rates of 1062.5 MBd (Fibre Channel) and 1250 MBd (Gigabit Ethernet)**
- **Low power consumption, 630 mW typical**
- **Transmitter and receiver functions incorporated onto a single IC**
- **Three package sizes available:**
  – 10 mm TQFP (HDMP-T1636AG)
  – 10 mm PQFP (HDMP-1636AG)
  – 10 mm PQFP (HDMP-1646AG)
- **10-bit wide parallel TTL compatible I/Os**
- **Single +3.3 V power supply**
- **5-volt tolerant I/Os**
- **2 kV ESD protection o n all pins**

Applications

- **1250 MBd Gigabit Ethernet interface**
- **1062.5 MBd Fibre Channel interface**
- **Mass storage system I/O channel**
- **Work station/server I/O channel**
- **Backplane serialization**
- **FC interface for disk drives and arrays**

CAUTION: *As with all semiconductor ICs, it is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).*

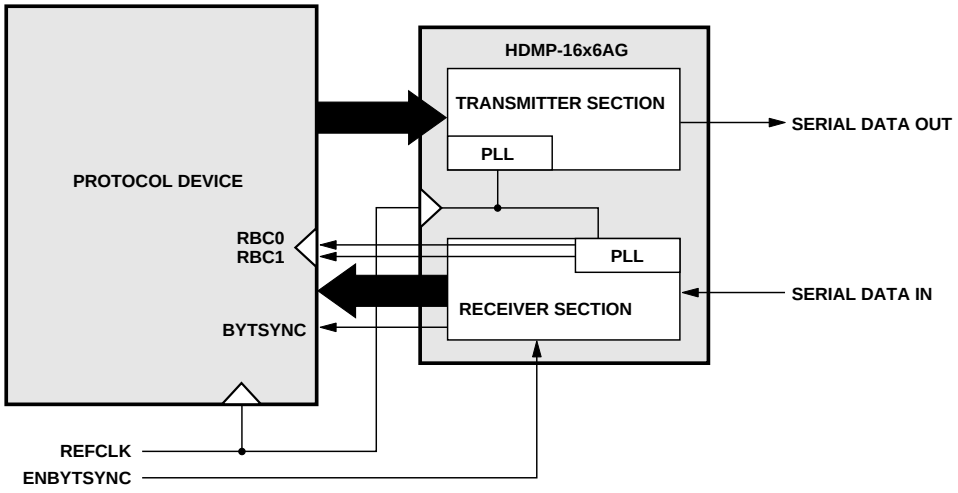


Figure 1. Typical application using the HDMP-1636AG/1646AG/T1636AG.

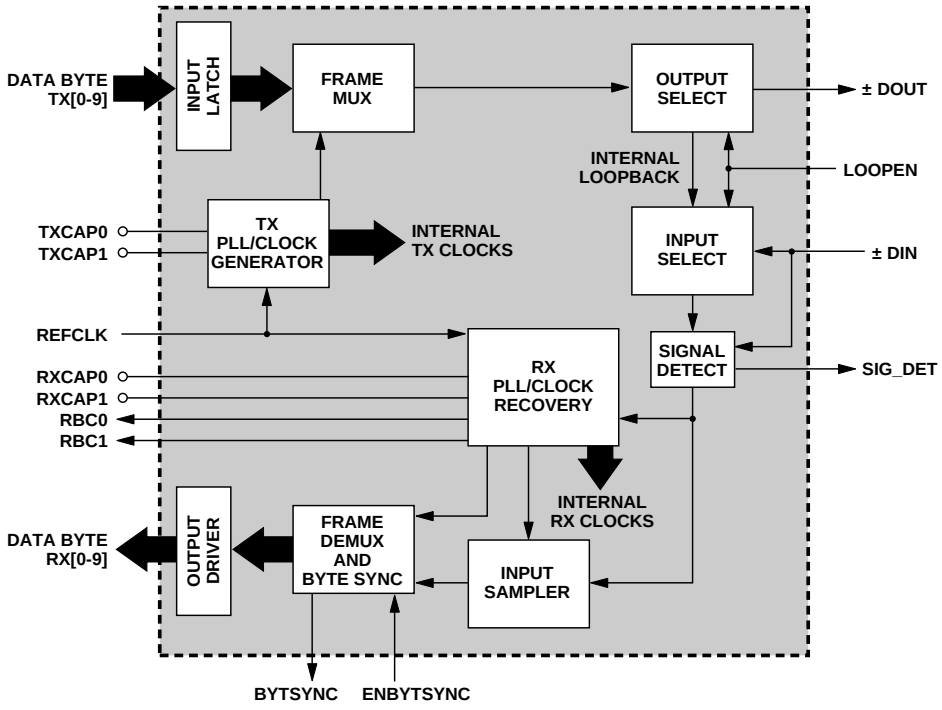


Figure 2. HDMP-1636AG/1646AG/T1636AG transceiver block diagram.

The receiver section accepts a serial electrical data stream at 1062.5 MBd or 1250 MBd and recovers the original 10-bit wide parallel data. The receiver PLL locks onto the incoming serial signal and recovers the high speed serial clock and data. The serial data is converted back into 10-bit parallel data, recognizing the 8B/10B comma character to establish byte alignment.

The recovered parallel data is presented to the user at TTL compatible outputs. The receiver section also recovers two receiver byte clocks which are 180 degrees out of phase with each other. For Gigabit Ethernet, these clocks are 62.5 MHz, whereas for Fibre Channel, they are 53.125 MHz. The parallel data is properly aligned with the rising edge of alternating clocks.

For test purposes, the transceiver provides for on-chip local loop-back functionality, controlled through an external input pin. Additionally, the byte synchronization feature may be disabled. This may be useful in proprietary applications which use alternative methods to align the parallel data.

HDMP-1636AG/1646AG/T1636AG Block Diagram

The HDMP-1636AG/1646AG/T1636AG was designed to transmit and receive 10-bit wide parallel data over a single high-speed line. The parallel data applied to the transmitter is expected to be 8B/10B encoded. In order to accomplish this task, the HDMP-1636AG/1646AG/T1636AG incorporates the following:

- TTL Parallel I/Os
- High Speed Phase Locked Loops
- Parallel to Serial Converter
- High Speed Serial Clock and Data Recovery Circuitry
- Comma Character Recognition Circuitry as per 8B/10B Specifications
- Byte Alignment Circuitry
- Serial to Parallel Converter

INPUT LATCH

The transmitter accepts 10-bit wide TTL parallel data at inputs TX[0..9]. The user-provided reference clock signal, REFCLK, is also used as the transmit byte clock. The TX[0..9] and REFCLK signals must be properly aligned, as shown in Figure 3.

TX PLL/CLOCK GENERATOR

The transmitter Phase Locked Loop and Clock Generator (TX PLL/CLOCK GENERATOR) block is responsible for generating all internal clocks needed by the transmitter section to perform its functions. These clocks are based on the supplied reference byte clock (REFCLK). REFCLK is used as both the frequency reference clock for the PLL and the transmit byte clock for the incoming data latches. It is expected to be properly aligned to the incoming parallel data (see Figure 3). This clock is then multiplied by 10 to generate the high speed clock necessary for clocking the high speed serial outputs.

FRAME MUX

The FRAME MUX accepts the 10-bit wide parallel data from the INPUT LATCH. Using internally generated high speed clocks, this parallel data is multiplexed into the high speed serial data stream. The data bits are transmitted sequentially, from the least significant bit (TX[0]) to the most significant bit (TX[9]).

OUTPUT SELECT

The OUTPUT SELECT block provides for an optional internal loopback of the high speed serial signal for testing purposes.

In normal operation, LOOPEN is set low and the serial data stream is placed at ±DOUT. When wrap-mode is activated by setting LOOPEN high, the ±DOUT pins are held static at logic 1 and the serial output signal is internally wrapped to the INPUT SELECT box of the receiver section.

INPUT SELECT

The INPUT SELECT block determines whether the signal at ±DIN or the internal loop-back serial signal is used. In normal operation, LOOPEN is set low and the serial data is accepted at ±DIN. When LOOPEN is set high, the high speed serial signal is internally looped-back from the transmitter section to the receiver section. This feature allows for loop back testing exclusive of the transmission medium.

RX PLL/CLOCK RECOVERY

The RX PLL/CLOCK RECOVERY block is responsible for frequency and phase locking onto the incoming serial data stream and recovering the bit and byte clocks. An automatic locking feature allows the Rx PLL to lock onto the input data stream without external PLL training controls. It does this by continually frequency locking onto the reference clock, and then phase locking onto the input data stream. An internal signal detection circuit monitors the presence of the input, and invokes the phase detection as the data stream appears. Once bit locked, the receiver generates the high speed sampling clock

for the input sampler, and recovers the two receiver byte clocks (RBC1/RBC0). These clocks are 180 degrees out of phase with each other, and are alternately used to clock out the 10-bit parallel output data.

INPUT SAMPLER

The INPUT SAMPLER is responsible for converting the serial input signal into a retimed serial bit stream. In order to accomplish this, it uses the high speed serial clock recovered from the RX PLL/CLOCK RECOVERY block. This serial bit stream is sent to the FRAME DEMUX and BYTE SYNC block.

FRAME DEMUX AND BYTE SYNC

The FRAME DEMUX AND BYTE SYNC block is responsible for restoring the 10-bit parallel data from the high speed serial bit stream. This block is also responsible for recognizing the comma character (or a K28.5 character) of positive disparity (0011111xxx). When recognized, the FRAME DEMUX AND BYTE SYNC block works with the RX PLL/CLOCK RECOVERY block to properly align the receive byte clocks to the parallel data. When a comma character is detected and realignment of the receiver byte clocks (RBC1/RBC0) is necessary, these clocks are stretched, not slivered, to the next possible correct alignment position. These clocks will be fully aligned by the start of the second 2-byte ordered set. The second comma character received shall be aligned with the rising edge of RBC1. As per the 8B/10B encoding scheme, comma characters must not be transmitted in consecutive bytes to allow the receiver byte clocks to maintain their proper recovered frequencies.

OUTPUT DRIVERS

The OUTPUT DRIVERS present the 10-bit parallel recovered data byte properly aligned to the receive byte clocks (RBC1/RBC0), as shown in Figure 5. These output data buffers provide TTL compatible signals.

SIGNAL DETECT

The SIGNAL DETECT block examines the differential amplitude of the inputs ±DIN. When this input signal is too small, it outputs a logic 0 at SIG_DET (refer to SIG_DET pin definition for detection thresholds), and at the same time, forces the parallel output RX[0]..RX[9] to all logic one (1111111111). The main purpose of this circuit is to prevent the generation of random data when the serial input lines are disconnected. When the signal at ±DIN is of a valid amplitude, SIG_DET is set to logic 1, and the output of the INPUT SELECT block is passed through.

HDMP-1636AG/1646AG/T1636AG (Transmitter Section) – Gigabit Ethernet Timing Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{setup}	Setup Time	nsec	1.5		
t_{hold}	Hold Time	nsec	1.0		
t_txlat[1]	Transmitter Latency	nsec		3.5	
		bits		4.4	

Note:

1. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock, REFCLK) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).

HDMP-1636AG/1646AG/T1636AG (Transmitter Section) – Fibre Channel Timing Characteristics

T_A[1] = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{setup}	Setup Time	nsec	2		
t_{hold}	Hold Time	nsec	1.5		
t_txlat[2]	Transmitter Latency	nsec		4.2	
		bits		4.4	

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.
2. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock, REFCLK) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).

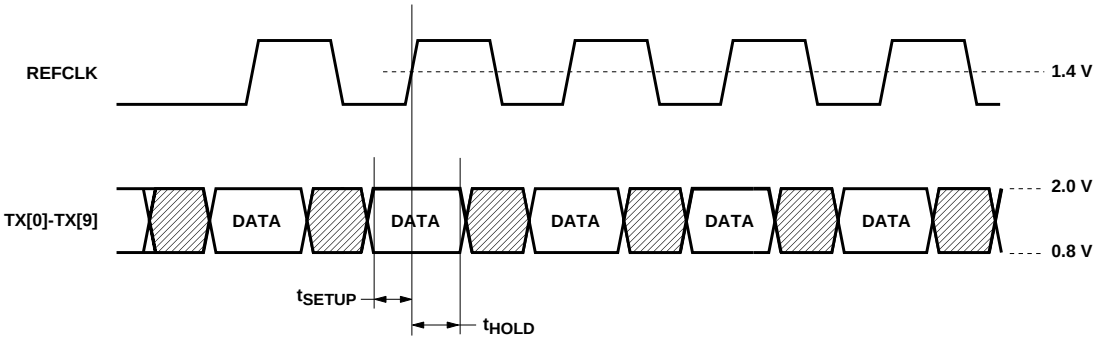


Figure 3. Transmitter section timing.

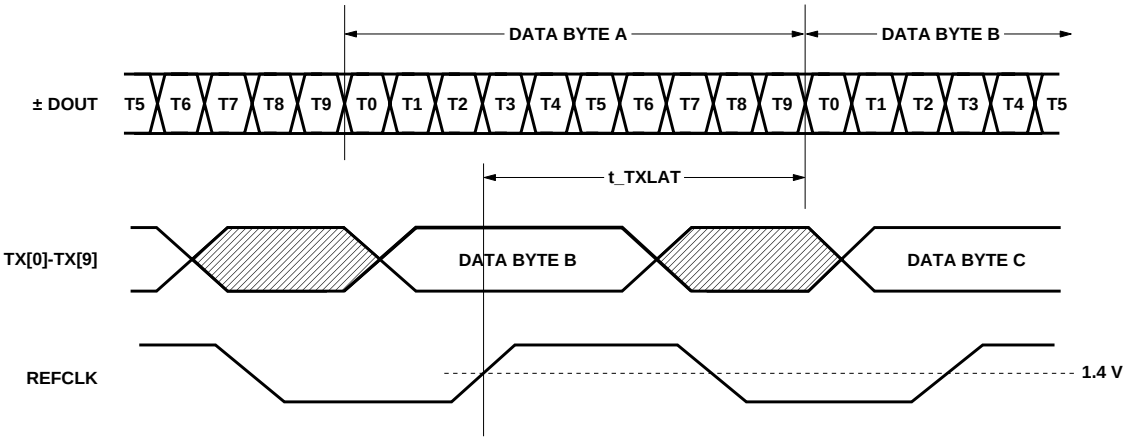


Figure 4. Transmitter latency.

HDMP-1636AG/1646AG/T1636AG (Receiver Section) – Gigabit Ethernet Timing Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
b_sync[1,2]	Bit Sync Time	bits			2500
f_lock	Frequency Lock at Powerup	µs			500
t_{valid_before}	Time Data Valid Before Rising Edge of RBC	nsec	2.5		
t_{valid_after}	Time Data Valid After Rising Edge of RBC	nsec	1.5		
t_{duty}	RBC Duty Cycle	%	40		60
t_{A-B}[3]	Rising Edge Time Difference between RBC0 and RBC1	nsec	7.5		8.5
t_rxlat[4]	Receiver Latency	nsec		22.4	
		bits		28.0	

Notes:

1. This is the recovery time for input phase jumps, per the Fibre Channel Specification X3.230-1994 FC-PH Standard, Sec 5.3.
2. Tested using C_{PLL} = 0.1 µF.
3. Guaranteed at room temperature.
4. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the first edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, either RBC1 or RBC0).

HDMP-1636AG/1646AG/T1636AG (Receiver Section) – Fibre Channel Timing Characteristics

T_A[1] = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
b_sync[2,3]	Bit Sync Time	bits			2500
t_{valid_before}	Time Data Valid Before Rising Edge of RBC	nsec	3		
t_{valid_after}	Time Data Valid After Rising Edge of RBC	nsec	1.5		
t_{duty}	RBC Duty Cycle	%	40		60
t_{A-B}[4]	Rising Edge Time Difference between RBC0 and RBC1	nsec	8.9	9.4	9.9
t_rxlat[5]	Receiver Latency	nsec		24.5	
		bits		26	

Notes:

1. Device tested and characterized under T_A conditions specified, with T_C monitored at approximately 20° higher than T_A.
2. This is the recovery time for input phase jumps, per the FC-PH specification Ref 4.1, Sec 5.3.
3. Tested using C_{PLL} = 0.1 µF.
4. The RBC clock skew is calculated as $t_{A-B(max)}$ - $t_{A-B(min)}$.
5. The receiver latency, as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the first edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, either RBC1 or RBC0).

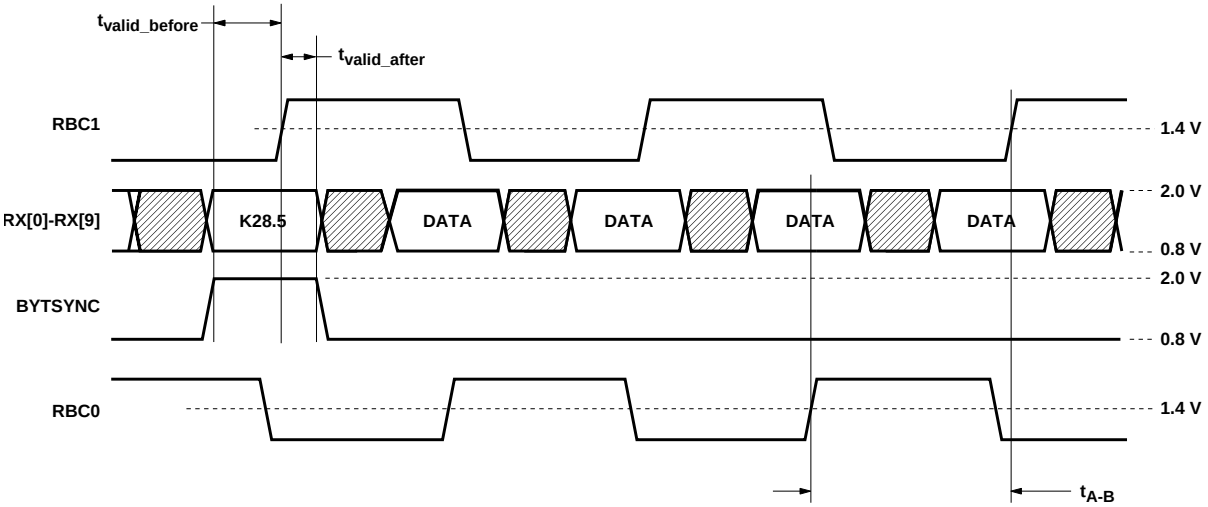


Figure 5. Receiver section timing.

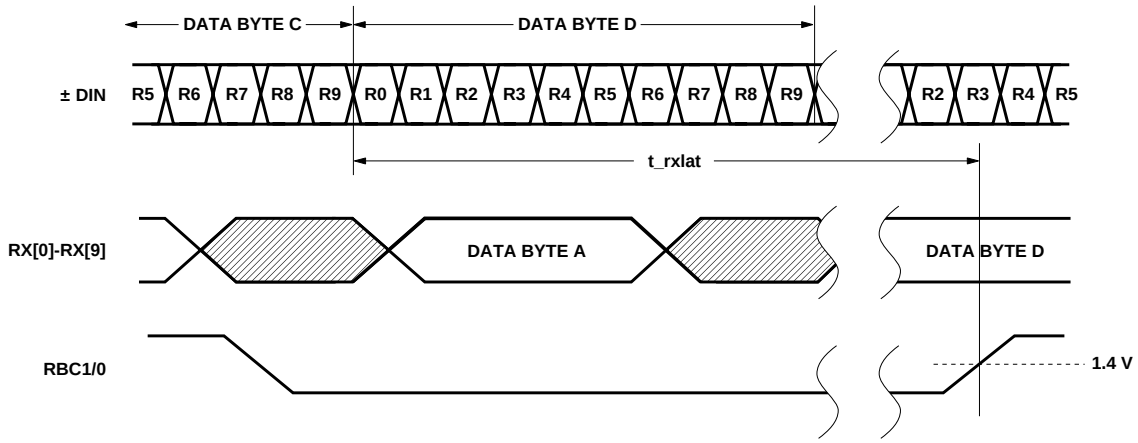


Figure 6. Receiver latency.

HDMP-1636AG/1646AG/T1636AG (TRx)

Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	-0.5	5.0
$V_{IN,TTL}$	TTL Input Voltage	V	-0.7	V_{CC} + 2.8
V_{IN,HS_IN}	HS_IN Input Voltage	V	2.0	V_{CC}
$I_{O,TTL}$	TTL Output Source Current	mA		13
T_{stg}	Storage Temperature	°C	-65	+150
T_j	Junction Operating Temperature	°C	0	+150

HDMP-1636AG/1646AG/T1636AG (TRx)

Guaranteed Operating Rates – Gigabit Ethernet

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Parallel Clock Rate (MHz)		Serial Baud Rate (MBaud)	
Min.	Max.	Min.	Max.
124.0	126.0	1240	1260

Guaranteed Operating Rates – Fibre Channel

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Parallel Clock Rate (MHz)		Serial Baud Rate (MBaud)	
Min.	Max.	Min.	Max.
106.20	106.30	1062.0	1063.0

HDMP-1636AG/1646AG/T1636AG (TRx)

Transceiver Reference Clock Requirements

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
f	Nominal Frequency (for Gigabit Ethernet Compliance)	MHz		125	
f	Nominal Frequency (for Fibre Channel Compliance)	MHz		106.25	
F_{tol}	Frequency Tolerance	ppm	-100		+100
Symm	Symmetry (Duty Cycle)	%	40		60

HDMP-1636AG/1646AG/T1636AG (TRx)

DC Electrical Specifications

T_A= 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed High Signal for All Inputs	V	2		V_{CC}
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs	V	0		0.8
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = -400 µA	V	2.2		V_{CC}
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.6
$I_{IH,TTL}$	Input High Current, V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA			40
$I_{IL,TTL}$	Input Low Current, V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA			-600
$I_{CC,TRx}$[1,2]	Transceiver V_{CC} Supply Current, T_A = 25°C	mA		220	

Notes:

1. Measurement conditions: Tested sending 1250 MBd PRBS 2^7-1 sequence from a serial BERT with ±DOUT outputs biased with 150 Ω resistors.
2. Typical specified with V_{CC} = 3.3 volts.

HDMP-1636AG/1646AG/T1636AG (TRx)

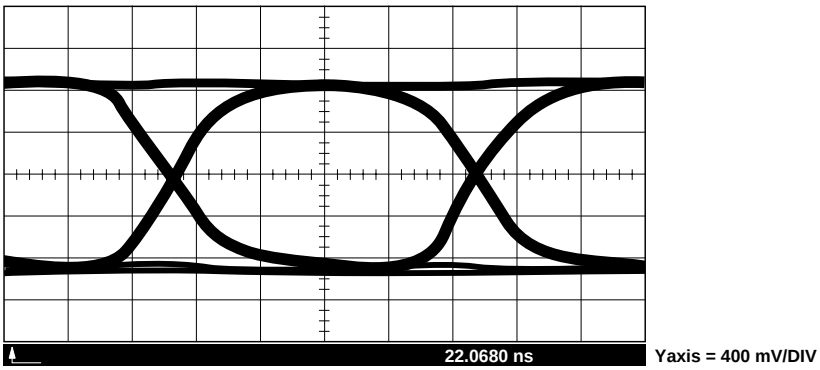
AC Electrical Specifications

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

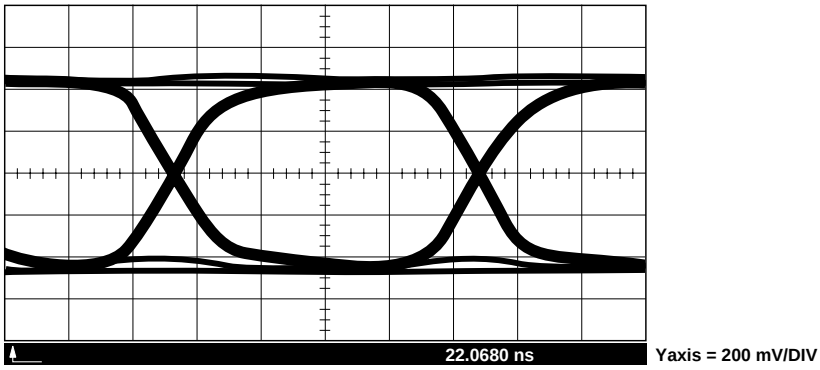
Symbol	Parameter	Units	Min.	Typ.	Max.
$t_{r,REFCLK}$	REFCLK Rise Time, 0.8 to 2.0 Volts	nsec			2.4
$t_{f,REFCLK}$	REFCLK Fall Time, 2.0 to 0.8 Volts	nsec			2.4
$t_{,TTLin}$	Input TTL Rise Time, 0.8 to 2.0 Volts	nsec		2	
$t_{f,TTLin}$	Input TTL Fall Time, 2.0 to 0.8 Volts	nsec		2	
$t_{r,TTLout}$	Output TTL Rise Time, 0.8 to 2.0 Volts, 10 pF Load	nsec		1.5	2.4
$t_{f,TTLout}$	Output TTL Fall Time, 2.0 to 0.8 Volts, 10 pF Load	nsec		1.1	2.4
t_{rs,HS_OUT}	HS_OUT Single-Ended (+DOUT) Rise Time	psec	85	225	327
t_{fs,HS_OUT}	HS_OUT Single-Ended (+DOUT) Fall Time	psec	85	200	327
t_{rd,HS_OUT}	HS_OUT Differential Rise Time	psec	85		327
t_{fd,HS_OUT}	HS_OUT Differential Fall Time	psec	85		327
V_{IP,HS_IN}	HS_IN Input Peak-to-Peak Differential Voltage	mV	200	1200	2000
V_{OP,HS_OUT}[1]	HS_OUT Output Peak-to-Peak Differential Voltage	mV	1200	1600	2200

Note:

1. Output Peak-to-Peak Differential Voltage specified as DOUT+ minus DOUT-.



a. Differential HS_OUT output (Dout+ minus Dout-).



b. Single-ended HS_OUT output (Dout+).

Eye diagrams of the high-speed serial outputs from the HDMP-1636AG/1646AG/T1636AG as captured on the 83480A digital communications analyzer. Tested with PRBS = 2^7-1.

Figure 7. Transmitter DOUT eye diagrams.

HDMP-1636AG/1646AG/T1636AG (Transmitter Section)

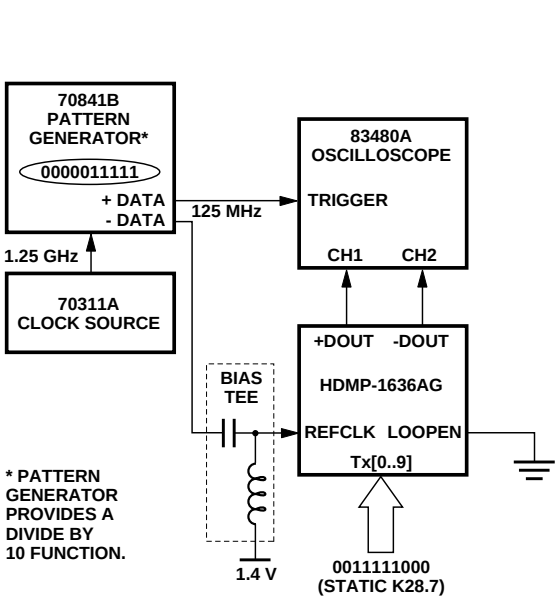
Output Jitter Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

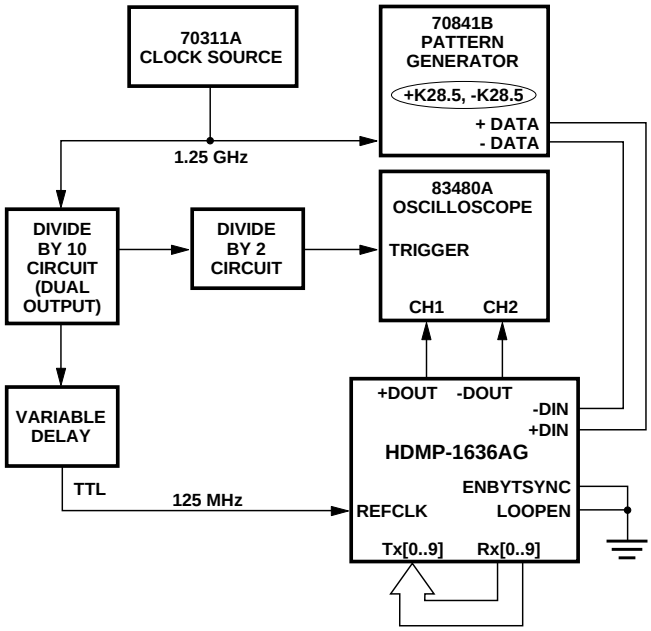
Symbol	Parameter	Units	Typ.
RJ[1]	Random Jitter at DOUT, the High Speed Electrical Data Port, specified as one sigma deviation of the 50% crossing point (RMS)	ps	8
DJ[1]	Deterministic Jitter at DOUT, the High Speed Electrical Data Port (pk-pk)	ps	15

Note:

1. Defined by Fibre Channel Specification X3.230-1994 FC-PH Standard, Annex A, Section A.4 and tested using measurement method shown in Figure 8.



a. Block diagram of RJ measurement method.



b. Block diagram of DJ measurement method.

Figure 8. Transmitter jitter measurement method.

HDMP-1636AG/1646AG/T1636AG

Package Thermal Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typ.	Max.
P_{Dmax}	Power Dissipation	mW	675	900
θ_{JA}[1]	Thermal Resistance: Junction to Ambient in Still Air	°C/W		
	HDMP-1646AG			36.3
	HDMP-1636AG			45.0
	HDMP-T1636AG			40.0
ψ_{JT}[2]	Thermal Characterization Parameter: Junction to Package Top	°C/W		
	HDMP-1646AG			9.6
	HDMP-1636AG			7.8
	HDMP-T1636AG			6.2

Notes:

Based on independent testing done by Avago.

1. θ_{JA} is based on thermal measurement in a still air environment at 23°C on a standard 3 x 3" FR4 PCB as specified in EIA/JESD 51-7.
2. ψ_{JT} is used to determine the actual junction temperature in a given application, using the following equation:
   $T_J = \psi_{JT} \times P_D + T_T$ where T_T is the measured temperature on top center of the package and P_D is the power being dissipated.

I/O Type Definitions

I/O Type	Definition
I-TTL	Input TTL, Floats High When Left Open
O-TTL	Output TTL
HS_OUT	High Speed Output, ECL Compatible
HS_IN	High Speed Input
C	External Circuit Node
S	Power Supply or Ground

HDMP-1636AG/46AG/T1636AG (TRx)
Pin Input Capacitance

Symbol	Parameter	Units	Typ.	Max.
C_{INPUT}	Input Capacitance on TTL Input Pins	pF	1.6	

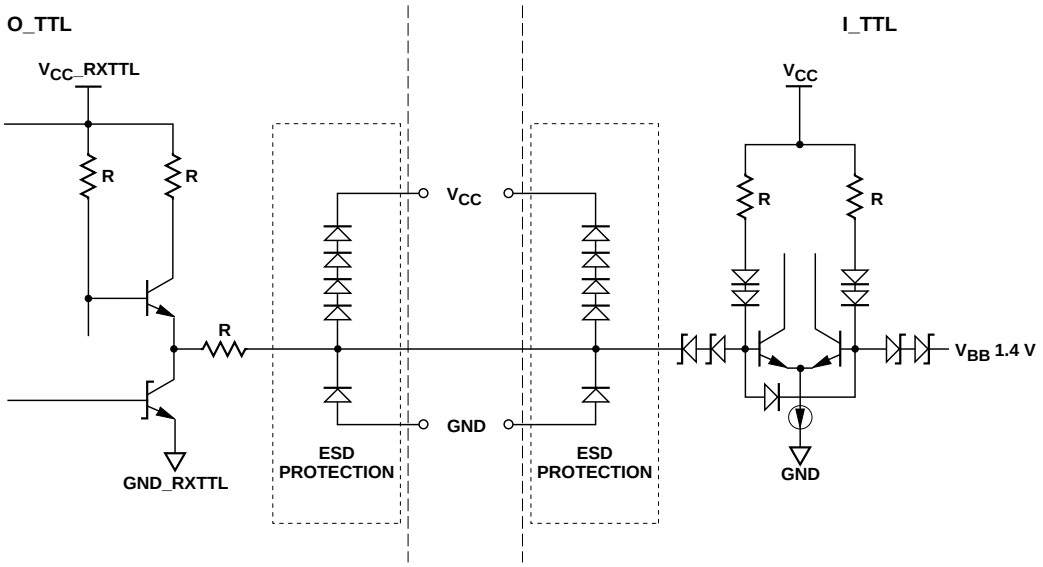


Figure 9. O-TTL and I-TTL simplified circuit schematic.

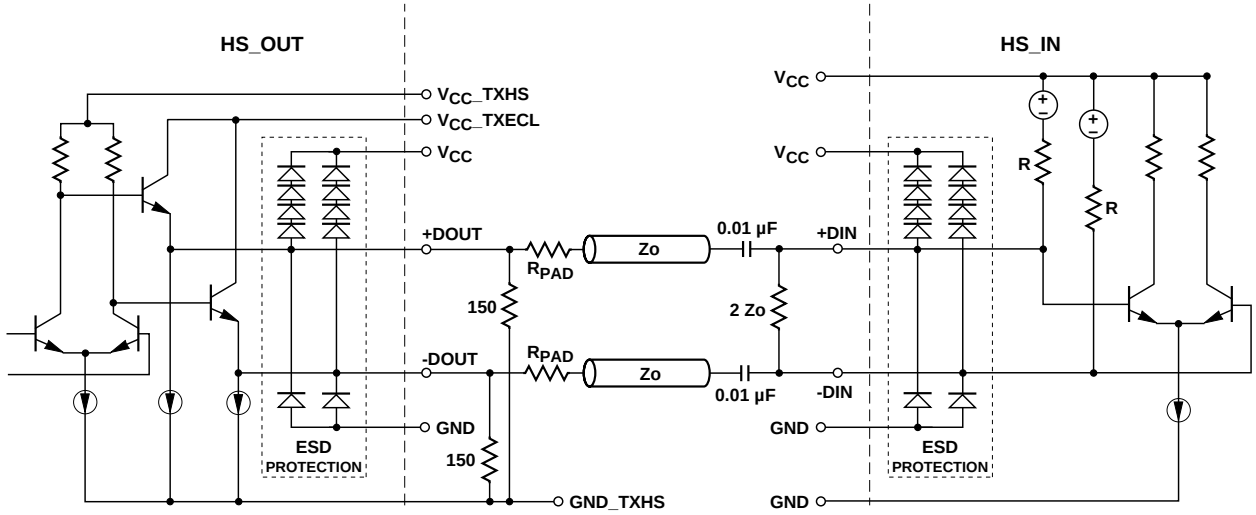
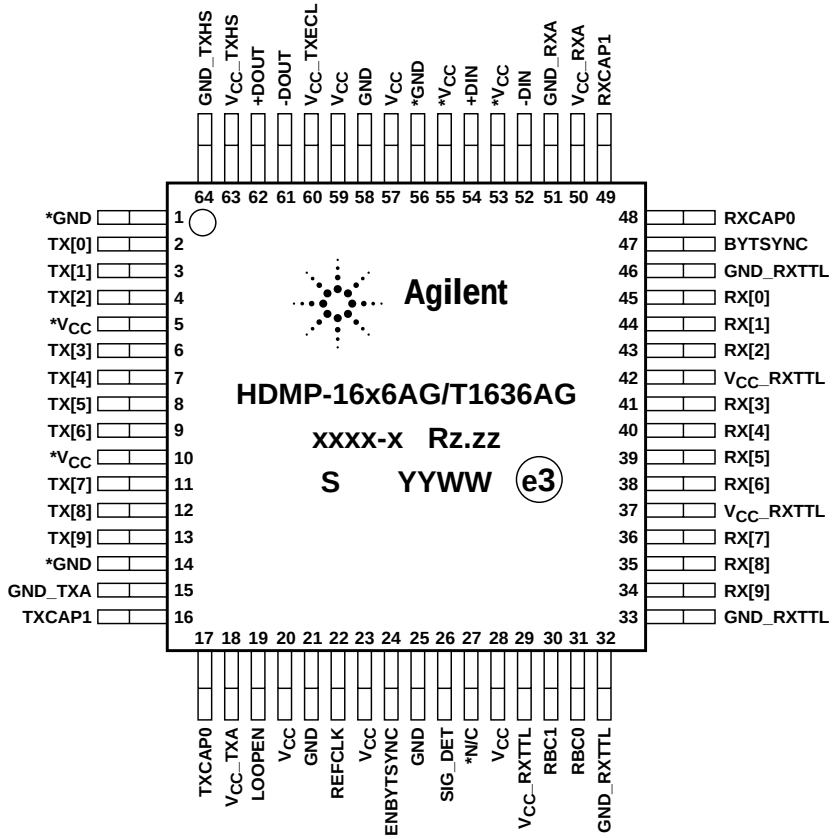


Figure 10. HS_OUT and HS_IN simplified circuit schematic.

Notes:
1. HS_IN inputs should never be connected to ground as permanent damage to the device may result.
2. The optional series padding resistors (R_{PAD}) help dampen load reflections. Typical R_{PAD} values for mismatched loads range between 25-Zo Ω.



xxxx-x = WAFER CODE
Rzz.zz = DIE REVISION
S = SUPPLIER CODE
YYWW = DATE CODE (YY = YEAR, WW = WORK WEEK)
COUNTRY = COUNTRY OF MANUFACTURE
(MARKED ON BACK OF DEVICE)

*N/C: THIS PIN IS CONNECTED TO AN ISOLATED PAD AND HAS NO FUNCTIONALITY. IT CAN BE LEFT OPEN, HOWEVER, TTL LEVELS CAN ALSO BE APPLIED TO THIS PIN.
*V_{CC}: THIS PIN IS BONDED TO AN ISOLATED PAD AND HAS NO FUNCTIONALITY. HOWEVER, IT IS RECOMMENDED THAT THIS PIN BE CONNECTED TO V_{CC} IN ORDER TO CONFORM WITH THE X3T11 "10-BIT SPECIFICATION," AND TO HELP DISSIPATE HEAT.
*GND: THIS PIN IS BONDED TO AN ISOLATED PAD AND HAS NO FUNCTIONALITY. HOWEVER, IT IS RECOMMENDED THAT THIS PIN BE CONNECTED TO GND IN ORDER TO CONFORM WITH THE X3T11 "10-BIT SPECIFICATION," AND TO HELP DISSIPATE HEAT.
(e3) = JESD97 Pb-FREE CATEGORY.

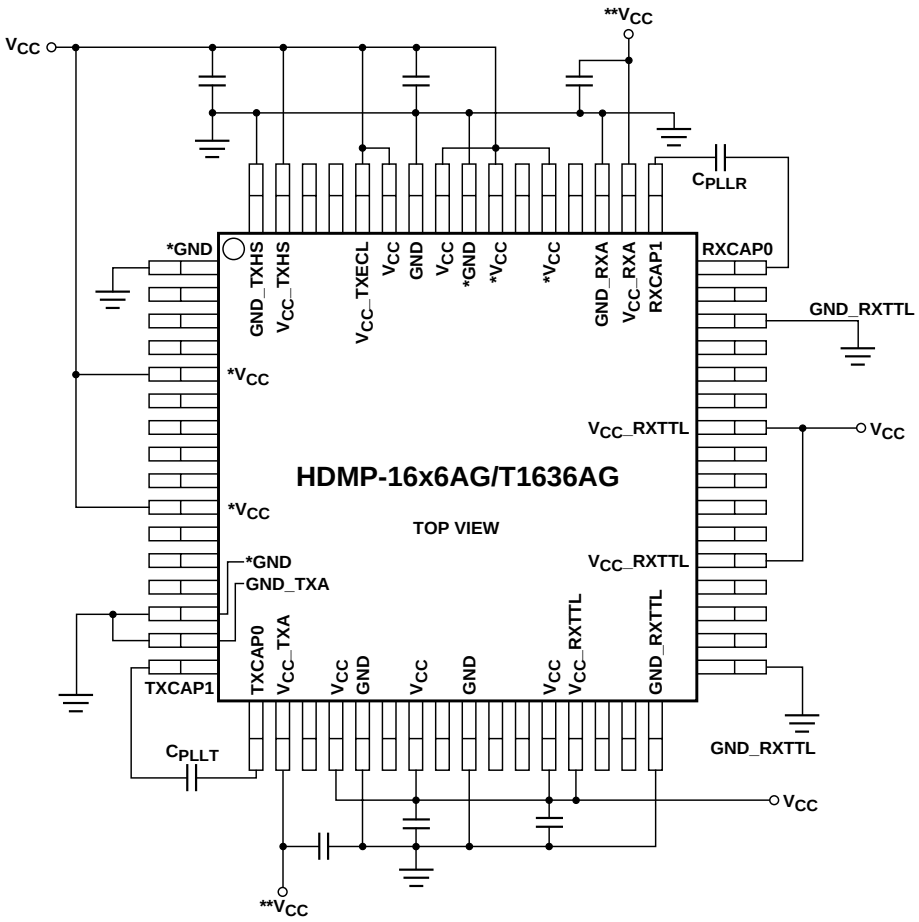
Figure 11. HDMP-1636AG/1646AG/T1636AG (TRx) package layout and marking, top view.

TRx I/O Definition

Name	Pin	Type	Signal
BYTSYNC	47	O-TTL	**Byte Sync Output:** An active high output. Used to indicate detection of a comma character (0011111XXX). It is only active when ENBYTSYNC is enabled.
-DIN +DIN	52 54	HS_IN	**Serial Data Inputs:** High-speed inputs. Serial data is accepted from the ±DIN inputs when LOOPEN is low.
-DOUT +DOUT	61 62	HS_OUT	**Serial Data Outputs:** High-speed outputs. These lines are active when LOOPEN is set low. When LOOPEN is set high, these outputs are held static at logic 1.
ENBYTSYNC	24	I-TTL	**Enable Byte Sync Input:** When high, turns on the internal byte sync function to allow clock synchronization to a comma character, (0011111XXX). When the line is low, the function is disabled and will not reset registers and clocks, or strobe the BYTSYNC line.
GND	21 25 58	S	**Logic Ground:** Normally 0 volts. This ground is used for internal PECL logic. It should be isolated from the noisy TTL ground as well as possible.
*GND	1 14 56		This pin is bonded to an isolated pad and has no functionality. However, it is recommended that this pin be connected to GND in order to conform with the X3T11 “10-bit specification,” and to help dissipate heat.
GND_RXA	51	S	**Analog Ground:** Normally 0 volts. Used to provide a clean ground plane for the receiver PLL and high-speed analog cells.
GND_RXTTL	32 33 46	S	**TTL Receiver Ground:** Normally 0 volts. Used for the TTL output cells of the receiver section.
GND_TXA	15	S	**Analog Ground:** Normally 0 volts. Used to provide a clean ground plane for the PLL and high-speed analog cells.
GND_TXHS	64	S	**Ground:** Normally 0 volts.
LOOPEN	19	I-TTL	**Loopback Enable Input:** When set high, the high-speed serial signal is internally wrapped from the transmitter’s serial loopback outputs back to the receiver’s loopback inputs. Also, when in loopback mode, the ±DOUT outputs are held static at logic 1. When set low, ±DOUT outputs and ±DIN inputs are active.
N/C	27		This pin is connected to an isolated pad and has no functionality. It can be left open, however, TTL levels can also be applied to this pin.
RBC1 RBC0	30 31	O-TTL	**Receiver Byte Clocks:** The receiver section recovers two 53.125 MHz (Fibre Channel)/62.5 MHz (Gigabit Ethernet) receive byte clocks. These two clocks are 180 degrees out of phase. The receiver parallel data outputs are alternately clocked on the rising edge of these clocks. The rising edge of RBC1 aligns with the output of the comma character (for byte alignment) when detected.
REFCLK	22	I-TTL	**Reference Clock and Transmit Byte Clock:** A 106.25 MHz (Fibre Channel)/125 MHz (Gigabit Ethernet) clock supplied by the host system. The transmitter section accepts this signal as the frequency reference clock. It is multiplied by 10 to generate the serial bit clock and other internal clocks. The transmit side also uses this clock as the transmit byte clock for the incoming parallel data TX[0]..TX[9]. It also serves as the reference clock for the receive portion of the transceiver.

TRx I/O Definition (cont'd.)

Name	Pin	Type	Signal
RX[0] RX[1] RX[2] RX[3] RX[4] RX[5] RX[6] RX[7] RX[8] RX[9]	45 44 43 41 40 39 38 36 35 34	O-TTL	**Data Outputs:** One 10 bit data byte. RX[0] is the first bit received. RX[0] is the least significant bit. When there is a loss of input signal at ±DIN, these outputs are held static at logic 1. Refer to SIG_DET (pin 26) pin definition for more details.
RXCAP0 RXCAP1	48 49	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal PLL must be connected across the RXCAP0 and RXCAP1 pins. (Typical value = 0.1 µF).
SIG_DET	26	O-TTL	**Signal Detect:** Indicates a loss of signal on the high-speed differential inputs, ±DIN, as in the case where the transmission cable becomes disconnected. If ±DIN >= 200 mV peak-to-peak, SIG_DET = logic 1. If ±DIN < 200 mV and ±DIN > 50 mV, SIG_DET = undefined. If ±DIN <= 50 mV, SIG_DET = logic 0. RX[0:9] = 1111111111.
TX[0] TX[1] TX[2] TX[3] TX[4] TX[5] TX[6] TX[7] TX[8] TX[9]	2 3 4 6 7 8 9 11 12 13	I-TTL	**Data Inputs:** One 10 bit, 8B/10B-encoded data byte. TX[0] is the first bit transmitted. TX[0] is the least significant bit.
TXCAP1 TXCAP0	16 17	C	**Loop Filter Capacitor:** A loop filter capacitor must be connected across the TXCAP1 and TXCAP0 pins (typical value = 0.1 µF).
V_{CC}	20, 23,28 57,59	S	**Logic Power Supply:** Normally 3.3 volts. Used for internal TX and RX PECL logic. It should be isolated from the noisy TTL supply as well as possible.
*V_{CC}	5, 10,53 55		This pin is bonded to an isolated pad and has no functionality. However, it is recommended that this pin be connected to V_{CC} in order to conform with the X3T11 "10-bit specification," and to help dissipate heat.
V_{CC}_RXA	50	S	**Analog Power Supply:** Normally 3.3 volts. Used to provide a clean supply line for the PLL and high-speed analog cells.
V_{CC}_RXTTL	29 37 42	S	**TTL Power Supply:** Normally 3.3 volts. Used for all TTL receiver output buffer cells.
V_{CC}_TXA	18	S	**Analog Power Supply:** Normally 3.3 volts. Used to provide a clean supply line for the PLL and high-speed analog cells.
V_{CC}_TXECL	60	S	**High-Speed ECL Supply:** Normally 3.3 volts. Used only for the last stage of the high-speed transmitter output cell (HS_OUT) as shown in Figure 10. Due to high current transitions, this V_{CC} should be well bypassed to a ground plane.
V_{CC}_TXHS	63	S	**High-Speed Supply:** Normally 3.3 volts. Used by the transmitter side for the high-speed circuitry. Noise on this line should be minimized for best operation.



*IT IS RECOMMENDED THAT THESE PINS BE CONNECTED TO THE APPROPRIATE SUPPLY LINE, EITHER V_{CC} OR GND, EVEN THOUGH THE PIN IS BONDED TO AN ISOLATED PAD. REFER TO THE I/O DEFINITIONS SECTION FOR THESE PINS FOR MORE DETAILS.
** SUPPLY VOLTAGE INTO V_{CC}_RXA AND V_{CC}_TXA SHOULD BE FROM A LOW NOISE SOURCE. ALL BYPASS CAPACITORS AND PLL FILTER CAPACITORS ARE 0.1 µF.

Figure 12. Power supply bypass.

Transceiver Power Supply Bypass and Loop Filter Capacitors

Bypass capacitors should be liberally used and placed as close as possible to the appropriate power supply pins of the HDMP-1636AG/1646AG/T1636AG as shown on the schematic of Figure 12. All bypass chip capacitors are 0.1 µF. The V_{CC}_RXA and V_{CC}_TXA pins are the analog power supply pins for the PLL sections. The voltage into these pins should be clean with minimum noise. The PLL loop filter capacitors and their pin locations are also shown on Figure 12. Notice that only two capacitors are required: C_{PLLT} for the transmitter and C_{PLLR} for the receiver. Nominal capacitance is 0.1 µF. The maximum voltage across the capacitors is on the order of 1 volt, so the capacitor can be a low voltage type and physically small. The PLL capacitors are placed physically close to the appropriate pins on the HDMP-1636AG/1646AG/T1636AG. Keeping the lines short will prevent them from picking up stray noise from surrounding lines or components.

Start-up Procedure:

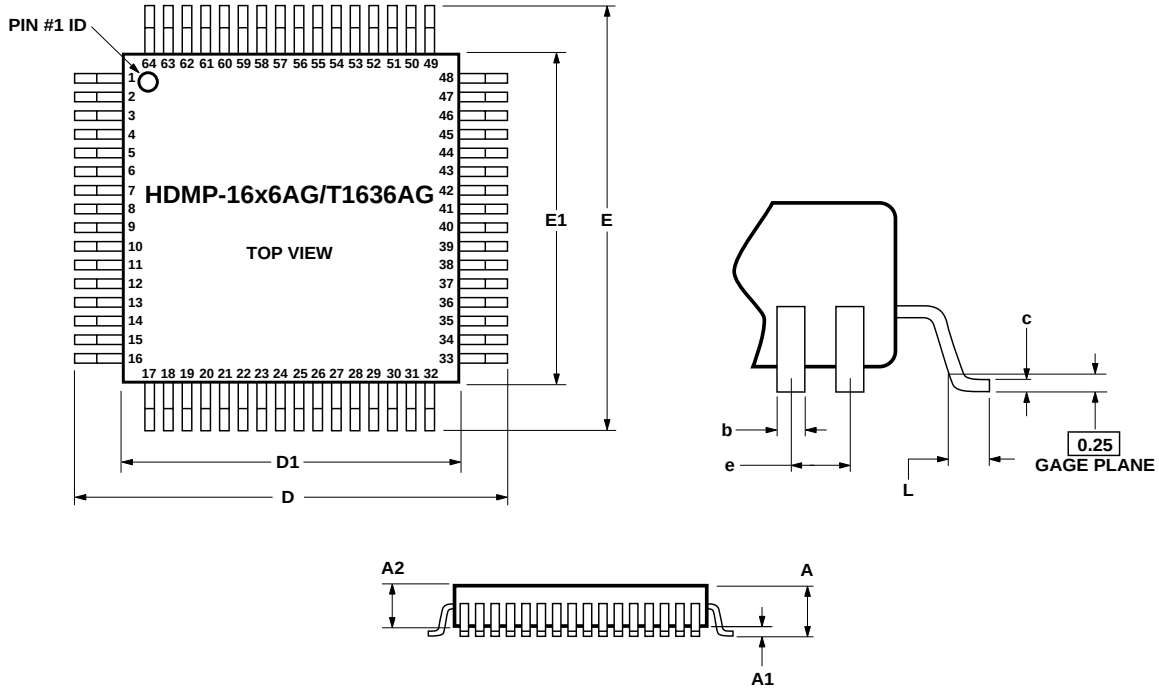
The transceiver start-up procedure(s) use the following conditions: V_{CC} = +3.3 V ±5% and REFCLK = 106.25 MHz (Fibre Channel)/125 MHz (Gigabit Ethernet) ±100 ppm.

After the above conditions have been met, apply valid data using a balanced code such as 8B/10B. Frequency lock occurs within 500 µs. After frequency lock, phase lock occurs within 2500 bit times.

Package Information

Item	Details
Package Material	Plastic
Lead Finish Material	100% Tin (Matte)
Lead Finish Thickness	10 µm minimum
Lead Coplanarity	HDMP-1636AG 0.08 mm max HDMP-T1636AG 0.08 mm max HDMP-1646AG 0.10 mm max

Mechanical Dimensions



ALL DIMENSIONS ARE IN MILLIMETERS.

PART NUMBER	D1/E1	D/E	b	e	L	c		A2	A1	A
HDMP-1636AG	10.00	13.20	0.22	0.50	0.88	0.17		2.00	0.25 MIN.	2.45
HDMP-1646AG	14.00	17.20	0.35	0.80	0.88	0.17		2.00	0.25 MAX.	2.35
TOLERANCE	± 0.10	± 0.25	± 0.05	BASIC	+ 0.15/ – 0.10	MAX.		+ 0.10/ – 0.05		MAX.

ALL DIMENSIONS ARE IN MILLIMETERS.

PART NUMBER	D1/E1	D/E	b	e	L	c		A2	A1	A
HDMP-T1636AG	10	12	0.22	0.50	0.60	0.20		1.00	0.15 MAX.	1.20
TOLERANCE	± 0.20	± 0.20	± 0.05	BASIC	± 0.15	MAX.		± 0.05	0.05 MIN.	MAX.

Meets JEDEC Pub 95 Outline: MS-026, Van. ACD

Figure 13. Mechanical dimensions of HDMP-1636AG/1646AG/T1636AG.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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