HARRIS SEMICONDUCTOR

HFA1102

Ultra High-Speed Current Feedback Amplifier with Compensation Pin

July 1995

Features

- Compensation Pin for Bandwidth Limiting
- Low Distortion (30MHz) . . . . . -56dBc
- -3dB Bandwidth 600MHz
- Very Fast Slew Rate 2000V/μs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) . . . . . ±0.05dB
  - (50MHz) . . . . . ±0.02dB
  - (30MHz) . . . . . ±0.01dB
- High Output Current 60mA
- Overdrive Recovery . . . . . <10ns

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1102 is a high speed wideband current feedback amplifier featuring a compensation pin for bandwidth limiting. Built with Harris' proprietary complementary bipolar UHF-1 process, it has excellent AC performance and low distortion.

Because the HFA1102 is already unity gain stable, the primary purpose for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. The bandwidth of the HFA1102 may be limited by connecting a capacitor and series damping resistor from pin 8 to ground. Typical bandwidths for various values of compensation capacitors are shown in the Electrical Specifications section of this datasheet.

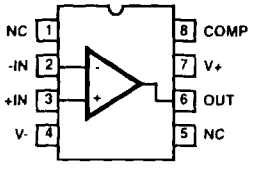
A variety of packages and temperature grades are available. See the ordering information below for details.

Ordering Information

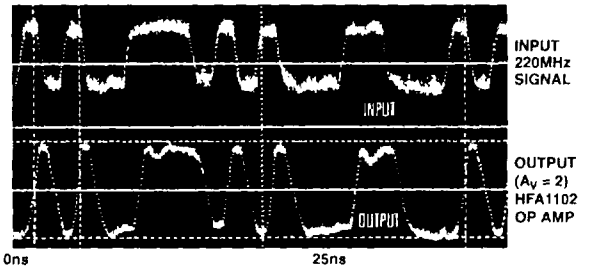
PART NUMBER	OPERATING TEMP RANGE	PRODUCT DESCRIPTION
HFA1102IJ	-40°C to +85°C	8 Lead CerDIP
HFA1102IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1102IB	-40°C to +85°C	8 Lead Plastic SOIC (N)
HFA1102Y	-40°C to +85°C	Die

Pinout

HFA1102
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps with Fastest Edges



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Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA
Junction Temperature (Ceramic and Die) ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10s) ..... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HFA1102I ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
CerDIP Package	116	36
Plastic DIP Package	130	N/A
SOIC Package	170	N/A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, C_{COMP} = 0pF. Unless Otherwise Specified

PARAMETER	TEMP	HFA1102I MIN	HFA1102I TYP	HFA1102I MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage	+25°C	-	2	6	mV
	Full	-	-	10	mV
Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} CMRR (ΔV_{CM} = ±2V)	+25°C	40	46	-	dB
	Full	38	-	-	dB
V_{IO} PSRR (ΔV_S = ±1.25V)	+25°C	45	50	-	dB
	Full	42	-	-	dB
Non-Inv. Input Bias Current (+IN = 0V)	+25°C	-	25	40	µA
	Full	-	-	65	µA
$+I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$+I_{BIAS}$ CMS (ΔV_{CM} = ±2V)	+25°C	-	20	40	µA/V
	Full	-	-	50	µA/V
Inv. Input Bias Current (-IN = 0V)	+25°C	-	12	50	µA
	Full	-	-	60	µA
$-I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$-I_{BIAS}$ CMS (ΔV_{CM} = ±2V)	+25°C	-	1	7	µA/V
	Full	-	-	10	µA/V
$-I_{BIAS}$ PSS (ΔV_S = ±1.25V)	+25°C	-	6	15	µA/V
	Full	-	-	27	µA/V
Non-Inv. Input Resistance	+25°C	25	50	-	kΩ
Inv. Input Resistance	+25°C	-	16	30	Ω
Input Capacitance (either input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±3.0	-	V
Input Noise Voltage (100kHz)	+25°C	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current (100kHz)	+25°C	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current (100kHz)	+25°C	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS A_V = +1, R_F = 150Ω, R_{DAMP} = 120Ω, Unless Otherwise Specified					
Open Loop Transimpedance	+25°C	-	500	-	kΩ

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, C_{COMP} = 0pF, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP	HFA1102I MIN	HFA1102I TYP	HFA1102I MAX	UNITS
Linear Phase Deviation (DC to 100MHz)		+25°C	-	0.6	-	Degrees
Differential Gain (NTSC, R_L = 75Ω)		+25°C	-	0.03	-	%
Differential Phase (NTSC, R_L = 75Ω)		+25°C	-	0.03	-	Degrees
Minimum Stable Gain		Full	1	-	-	V/V
Bandwidth Limiting Characteristics -3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, A_V = +1)	C_{COMP} = 0pF	+25°C	-	600	-	MHz
	C_{COMP} = 1pF	+25°C	-	350	-	MHz
	C_{COMP} = 3pF	+25°C	-	190	-	MHz
	C_{COMP} = 7pF	+25°C	-	55	-	MHz
Gain Flatness (to 30MHz)	C_{COMP} = 0pF	+25°C	-	±0.01	-	dB
	C_{COMP} = 1pF	+25°C	-	±0.05	-	dB
	C_{COMP} = 3pF	+25°C	-	±0.10	-	dB
Gain Flatness (to 100MHz)		+25°C	-	±0.05	-	dB
Gain Flatness (to 50MHz)		+25°C	-	±0.02	-	dB
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified						
Output Voltage (A_V = -1)		+25°C	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current (R_L = 50Ω, A_V = -1)		+25°C	50	65	-	mA
		Full	40	60	-	mA
DC Closed Loop Output Impedance		+25°C	-	0.1	-	Ω
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-56	-	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz)		+25°C	-	30	-	dBm
1dB Compression (100MHz)		+25°C	-	20	-	dBm
TRANSIENT RESPONSE A_V = +1, R_F = 150Ω, R_{DAMP} = 120Ω, Unless Otherwise Specified						
Rise Time (V_{OUT} = 2.0V Step)		+25°C	-	600	-	ps
Overshoot (V_{OUT} = 2.0V Step)		+25°C	-	10	-	%
Slew Rate (A_V = +1, V_{OUT} = 5V_{P-P})		+25°C	-	1200	-	V/µs
Slew Rate (A_V = +2, V_{OUT} = 5V_{P-P})		+25°C	-	2000	-	V/µs
0.1% Settling (V_{OUT} = 2V to 0V)		+25°C	-	11	-	ns
0.2% Settling (V_{OUT} = 2V to 0V)		+25°C	-	7	-	ns
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current		+25°C	-	21	26	mA
		Full	-	-	33	mA

Applications Information

Optimum Feedback Resistor (R_F)

All current feedback amplifiers require a feedback resistor, even for unity gain applications. The R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1102 design is optimized for a 150Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, leading to excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a tradeoff of bandwidth vs. stability.

Bandwidth Limiting

The bandwidth of the HFA1102 may be limited by connecting a resistor (R_{DAMP}) and capacitor in series from pin 8 to GND. The series resister is required to damp the interaction between the package parasitics and C_{COMP}. Typical bandwidths for various values of compensation capacitor are shown in the specification tables. Because the HFA1102 is already unity gain stable, the main reason for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. Additionally, compensating the HFA1102 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} offsets the bandwidth increase from the lower R_F, keeping the amplifier stable. Reducing R_F provides the double benefits of reduced DC errors ($-I_B \times R_F$) and reduced total noise ($i_{ni} \times R_F$ and $4KTR_F$).

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

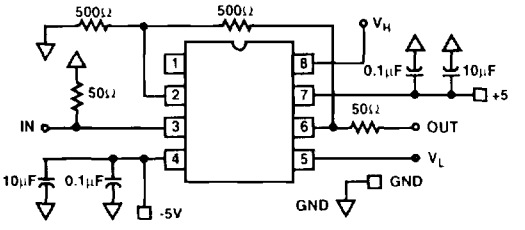
Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

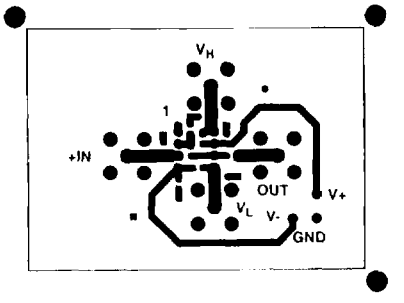
An example of a good high frequency layout is the Evaluation Board shown.

Evaluation Board

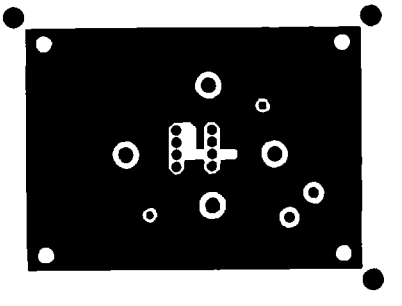
The HFA1102 may be evaluated using the HFA1130 Evaluation Board which is available from your local sales office. R_{DAMP} and C_{COMP} should be connected in series from the socket pin to the GND plane. The trace from pin 8 to the V_H connector should be cut near the socket to remove this parallel capacitance. The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT



Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils ±1mil
1600µm x 1130µm ±25.4µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiWType: Metal 2: AlCu (2%)
Thickness: Metal 1: 8kÅ ±0.4kÅThickness: Metal 2: 16kÅ ±0.8kÅ

GLASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

DIE ATTACH:

Material: Epoxy - Plastic DIP and SOIC

WORST CASE CURRENT DENSITY:

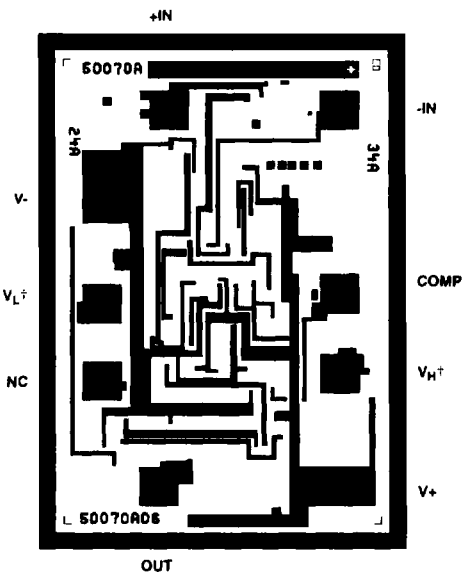
$0.909 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1102



† Output Clamping Function (V_H, V_L) is available to users of the HFA1102 in die form. Please refer to the HFA1130 data sheet for infomation regarding the operation and use of this function.