DATA SHEET

HM 65768B

4 K x 4
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  COMMERCIAL : 25/35/45/55 ns (max)
  MILITARY : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 200 mW (typ)
  STANDBY : 35 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

INTRODUCTION

The HM 65768B is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 385 mW.
The HM 65768B features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 77 % when the circuit is deselected.

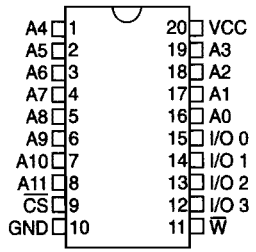
Each memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.
All inputs and outputs of the HM 65768 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65768B is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

7

INTERFACE

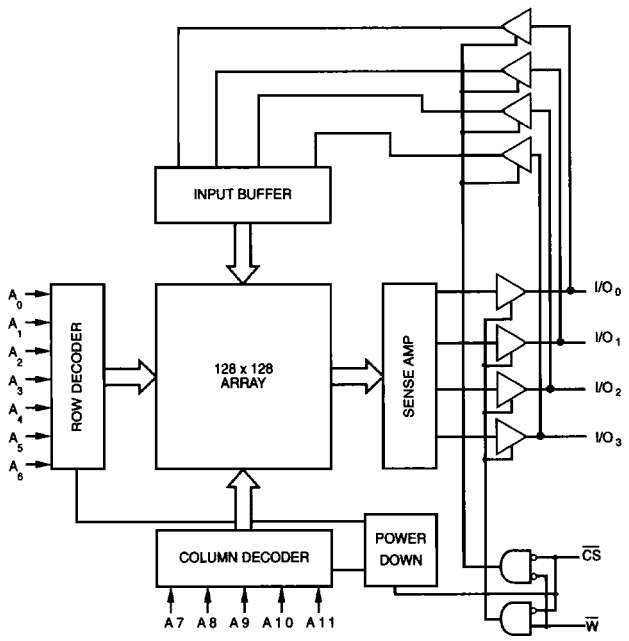
PIN CONFIGURATION

Plastic 300 mils, 20 pins, DIL.
Ceramic 300 mils, 20 pins, DIL.
SOIC 300 mils, 20 pins, DIL.
SOJ 300 mils, 20 pins.

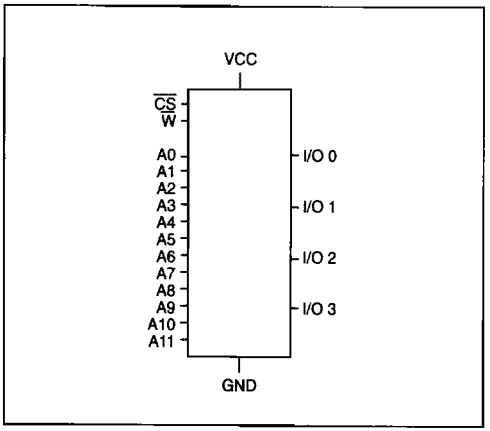


Pinout DIL 20 pins (top view)

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A11	: Address inputs	$\overline{CS}$	: Chip Select
I/O0-I/O3	: Input/Output	$\overline{W}$	: Write enable
Vcc	: Power		
Gnd	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA
Electro static discharge voltage > 2000 V
(MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

7

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 0.5	0.0	0.8	V
VIH	Input high voltage	2.2	–	5.5	V

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C – f = 1 MHz – Vcc = 5.0 V.

DC PARAMETERS

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION

SYMBOL		PARAMETER	65768B H-5	65768B K-5	65768B M-5	65768B N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	15	15	15	30	mA	max
ICCOP	(7)	Dynamic operating current	70	70	70	90	mA	max

CONSUMPTION FOR MILITARY (– 2) SPECIFICATION

SYMBOL		PARAMETER	65768B H-2	65768B K-2	65768B M-2	65768B N-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	30	20	20	20	mA	max
ICCOP	(7)	Dynamic operating current	80	70	70	90	mA	max

Notes : 6. $\overline{CS} \geq VIH$, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

7

AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a*) : +30 pF

AC TEST LOADS AND WAVEFORMS

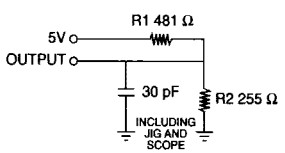


Figure 1 a

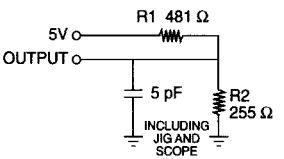


Figure 1 b

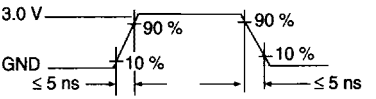
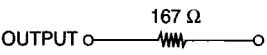


Figure 2

Equivalent to : THEVENIN EQUIVALENT



WRITE CYCLE : COMMERCIAL (– 5) SPECIFICATION

SYMBOL	PARAMETER	65768B H-5	65768B K-5	65768B M/N-5	UNIT	VALUE
TAVAV	Write Cycle time	25	35	40	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	35	ns	min
TDVWH (8)	Data set-up time	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	35	35	ns	min
TWLQZ (9)	Write low to high Z	10	15	20	ns	max
TWLWH	Write pulse width	20	30	35	ns	min
TWHAX	Address hold from end of write	2	2	2	ns	min
TWHDX (8)	Data hold time	0	3	3	ns	min
TWHQX	Write high to low Z	0	0	0	ns	min
TEHAX	Address hold from end $\overline{CS}$	3	3	3	ns	min

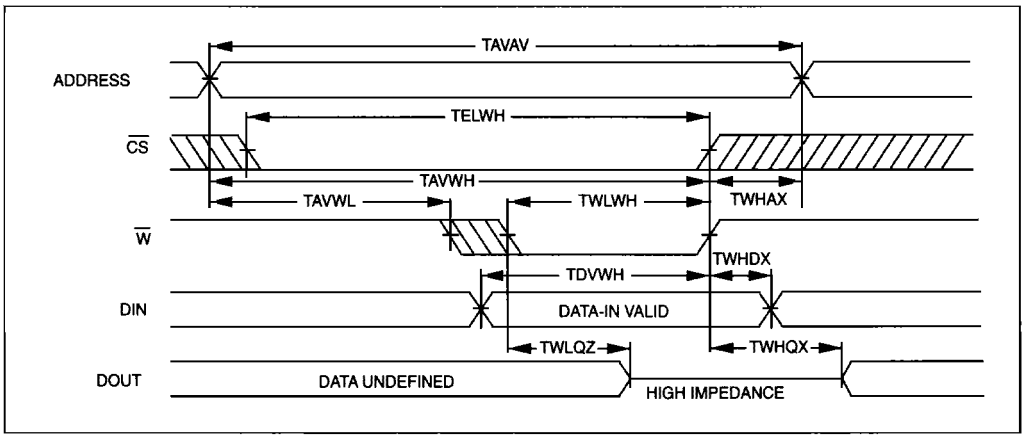
WRITE CYCLE : MILITARY (– 2) SPECIFICATION

SYMBOL	PARAMETER	65768B H-2	65768B K-2	65768B M-2	65768B N-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	40	40	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	35	35	ns	min
TDVWH (8)	Data set-up time	15	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	35	35	35	ns	min
TWLQZ (9)	Write low to high Z	10	15	20	20	ns	max
TWLWH	Write pulse width	20	30	35	35	ns	min
TWHAX	Address hold from end of write	2	2	2	2	ns	min
TWHDX (8)	Data hold time	0	0	3	3	ns	min
TWHQX	Write high to low Z	3	6	6	6	ns	min
TEHAX	Address hold from end $\overline{CS}$	3	3	3	3	ns	min

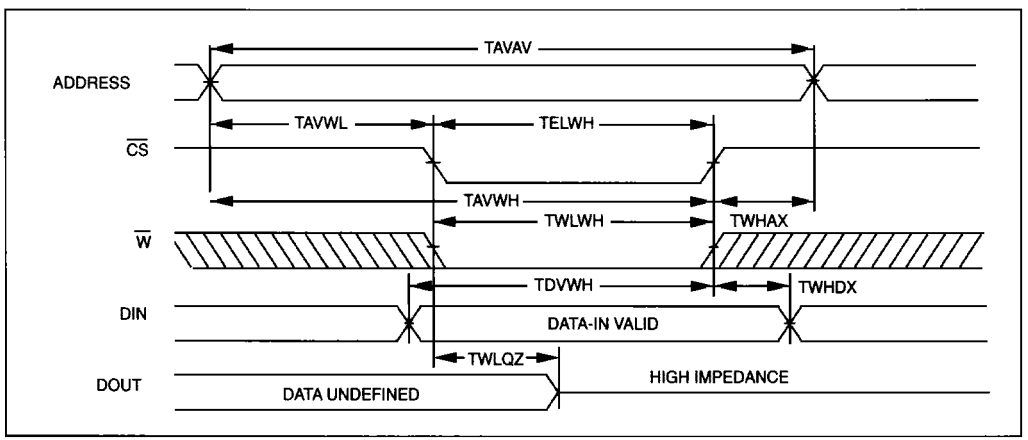
Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. TWLQZ and TEHQZ are specified with CL = 5 pF as in part (1b) of AC test loads.

7

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



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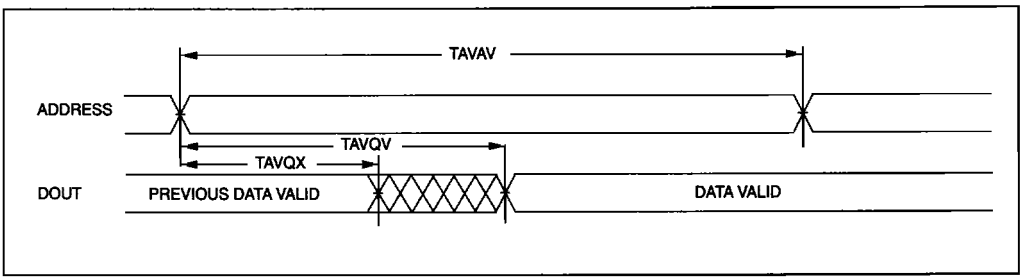
READ CYCLE : COMMERCIAL (– 5) SPECIFICATION

SYMBOL	PARAMETER	65768B H-5	65768B K-5	65768B M-5	65768B N-5	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ (9)	$\overline{CS}$ high to high Z	15	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	25	30	30	ns	max

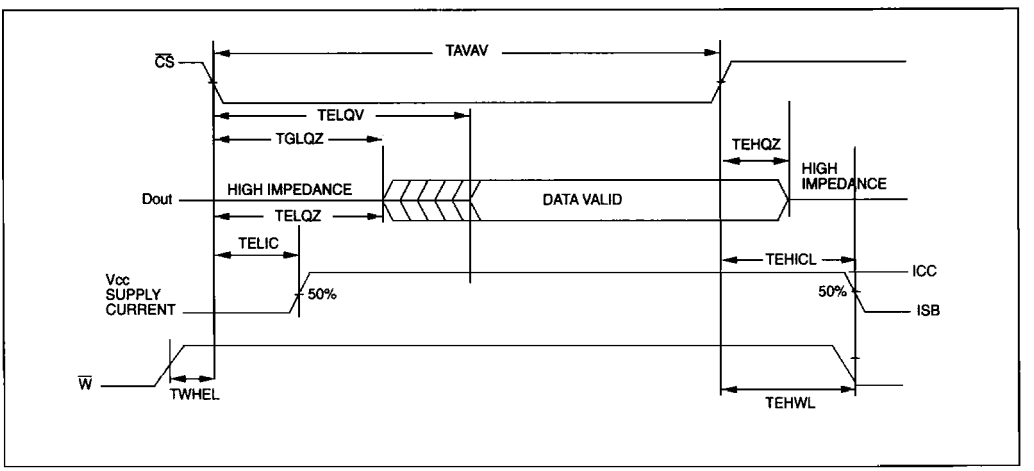
READ CYCLE : MILITARY (– 2) SPECIFICATION

SYMBOL	PARAMETER	65768B H-2	65768B K-2	65768B M-2	65768B N-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	ns	min
TEHQZ (9)	$\overline{CS}$ high to high Z	15	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	25	30	30	ns	max

READ CYCLE nb 1



READ CYCLE nb 2



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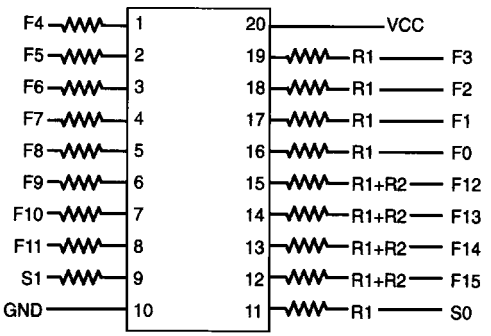
BURN-IN SCHEMATICS



R1 = 300 Ω per row
R2 = 2 KΩ per driver
FO = 25 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycles

ORDERING INFORMATION

PACKAGE	DEVICE TYPE	GRADE	LEVEL
HM 3 —	65768B	H	-5 : R

4 k x 4 high speed static RAM

0 - Chip form
1 - Ceramic 20 pins 300 mils
3 - Plastic 20 pins 300 mils
T - SOIC 20 pins 300 mils
U - SOJ 20 pins 300 mils

H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

- 2 : Military
- 5 : Commercial
- 6 : 100% 25°C Probe
/883 : MIL STD 883 Class B or S
DB : Dice Military program
R : Tape & Reel option
RD : Tape & Reel / Dry pack option
D : Dry pack option

7