

## **IEEE Floating Point Multiplier**

ADSP-3210

## **FEATURES**

Fully Compatible with IEEE Standard 754

Three Data Formats:

32-Bit Single-Precision Floating Point

64-Bit Double-Precision Floating Point

32-Bit Fixed Point

High Speed:

Single-Precision Throughput of 100ns/10 MEGAFLOPS

Double-Precision Throughout of

400ns/2.5 MEGAFLOPS

Fixed Point Throughput of 100ns/10MHz

Low Latency for Scalar Operations: 300ns Single-Precision Latency

600ns Double-Precision Latency

300ns Fixed-Point Latency

Two-Port Structure Supports Full Data Transfer Rate One Internal Pipeline Stage

Low-Power TTL-Compatible 1.5 Micron CMOS Technology

400mW Max Power Dissipation

Fully Registered I/O and Controls
Three-State Outputs with Separate Enables
100-Lead Pin Grid Array

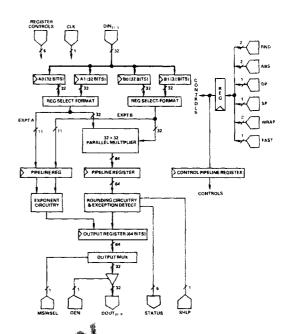
## GENERAL DESCRIPTION

The ADSP-3210 is a high-speed floating point multiplier. The ADSP-3210 and its companion ALU, the ADSP-3220 are basic building blocks for high-speed numerical processors. These devices offer a full set of operations on three data formats: 32-bit single-precision floating point, 64-bit double-precision floating point, and 32-bit twos-complement fixed point.

The ADSP-3210 provides a high-speed, low-power solution to floating point multiplication requirements. Pipelined results are produced every 100ns for single-precision floating point and fixed-point data formats. The direct operand feed mode low total latency of 300ns<sup>1</sup>. Pipelined double-precision floating point results are produced every 400ns. Maxim more dissipation is less than 400mW, worst case.

The ADSP-3210's data formats and coams point operations conform to the proposed IEEE Standard 754. The 1051 32 0 supports all four rounding modes in the standard for all three data formats. All four exception conditions—over tow, underfloinvalid operation, and inexact result—are flagged by dedicated status pins.

## ADSP-3210 IEEE FLOATING POINT MULTIPLIER



The ADSP 5210 ms a two-port structure: one 32-bit input port and one 32-bit tutput port. Two 32-bit registers are available for each of the A and B operands. Data inputs and outputs a fet at twice the cycle rate, allowing two 32-bit input operations and one 64-be on but operation on every cycle. All inputs and output are a second.

The CSF 3210 is available for both commercial and military sture ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts at a stable processed fully to MIL-STD-883, Class B.

setup + processing + output delay of most significant output ord.

