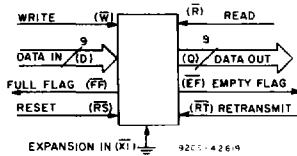


CD54/74AC7201, CD54/74AC7202 CD54/74ACT7201, CD54/74ACT7202



Parallel FIFO

CD54/74AC/ACT7201 - 512 x 9 Bit
CD54/74AC/ACT7202 - 1024 x 9 Bit

FUNCTIONAL DIAGRAM

Type Features:

- Asynchronous and simultaneous read/writes in multiprocessing and rate-buffer applications
- Fully expandable by both word depth and/or bit width

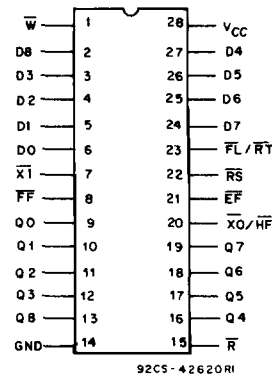
The RCA CD54/74AC7201 and CD54/74AC7202 and the CD54/74ACT7201 and CD54/74ACT7202 dual-port memories use the RCA ADVANCED CMOS technology. Data are loaded and emptied on a first-in, first-out (FIFO) basis. Full and empty flags are used to prevent data overflow and underflow, and expansion logic is provided for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers; no address information is required to load and unload data. Data are toggled in and out of the device through the use of Write (W) and Read (R) control pins.

The 9-bit wide data array allows control and parity bits to be used at the user's option. This device also features a Retransmit (RT) capability that allows for reset of the read pointer to its initial position when RT is pulsed LOW to allow for transmission from the beginning of data.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Balanced propagation delays
- AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 8 mA output drive current



TERMINAL ASSIGNMENT

TRUTH TABLE

RESET AND RETRANSMIT — SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	RS	RT	X1	READ POINTER	WRITE POINTER	EF	FF
Reset	0	X	0	Location Zero	Location Zero	0	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X
Read/Write	1	1	0	Increment*	Increment*	X	X

*Pointer will increment if flag is HIGH.

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