CY7C277
CY7C279

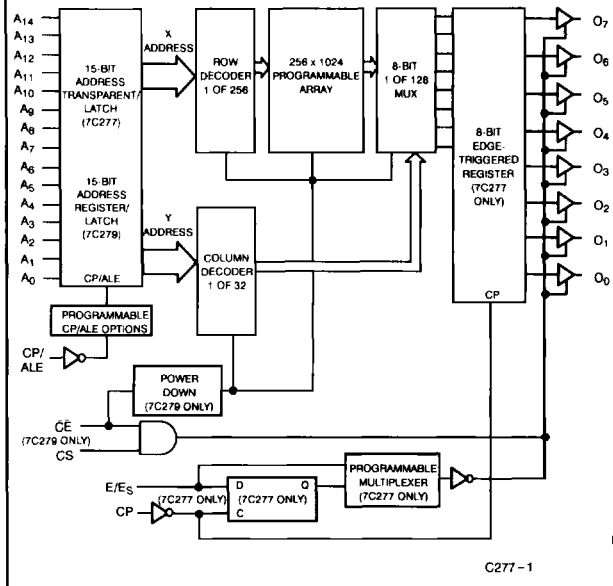
CYPRESS SEMICONDUCTOR

Reprogrammable 32K x 8 Registered PROM

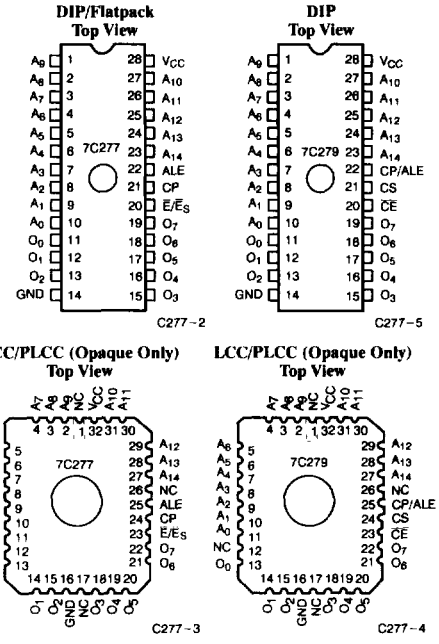
Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 30 ns (7C277) and 3 ns (7C279) max. set-up
  - 15 ns (7C277) and 35 ns (7C279) clock to output
- Low power
  - 660 mW (commercial)
  - 715 mW (military)
- Programmable address latch enable input
- Programmable synchronous or asynchronous output enable (7C277)
- On-chip edge-triggered output registers (7C277)
- Optional registered/latched address inputs (7C279)
- EPROM technology, 100% programmable
- Slim 300-mil, 28-pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

Logic Block Diagram



Pin Configurations



Selection Guides

		7C277-30	7C279-35	7C277-40	7C279-45	7C277-50	7C279-55
Maximum Access Time (ns)			35		45		55
Maximum Setup Time (ns)		30		40		50	
Maximum Clock to Output (ns)		15		20		25	
Maximum Operating Current (mA)	Com'l	120	120	120	120	120	120
	Military			130	130	130	130
Maximum Standby Current (mA)	Com'l		30		30		30
	Military				40		40

Functional Description

The CY7C277 and the CY7C279 are high-performance 32K word by 8-bit CMOS PROMs. When deselected, the 7C279 automatically powers down into a low-power standby mode. The 7C277 and the 7C279 both are packaged in the slim 28-pin 300-mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide algorithms.

The CY7C277 and the CY7C279 offer the advantages of low power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8-bit edge triggered output register. The $\overline{E}/E_S$ input provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the $\overline{E}/E_S$ pin operates as an asynchronous output enable. If the synchronous mode is selected, the $\overline{E}/E_S$ pin is sampled on the rising edge of CP to enable and disable the outputs. The 7C277 also provides a programmable bit to enable the Address Latch input. If this bit is not programmed, the device will ignore the ALE pin and the address will enter the device asynchronously. If the ALE function is selected, the address enters the PROM while the ALE pin is active, and is captured when ALE is deasserted. The user may define the polarity of the ALE signal, with the default being active HIGH.

On the 7C279, address registers are provided to easily interface with the Cypress 7C601 and other microprocessors that deliver addresses around a rising clock edge. A programmable bit is provided to select between latched and registered address inputs. The default is registered inputs, which will sample the address on the RISING EDGE of CP and load the address register. The latched address option will recognize any address changes while the ALE pin is active and load the address into the address latches on the deactivating edge of ALE. If the latched address option is selected, another programmable bit is provided for the user to select the polarity that will define ALE active, with the default being active HIGH.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	− 40°C to +85°C	5V ±10%
Military[2]	− 55°C to +125°C	5V ±10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.

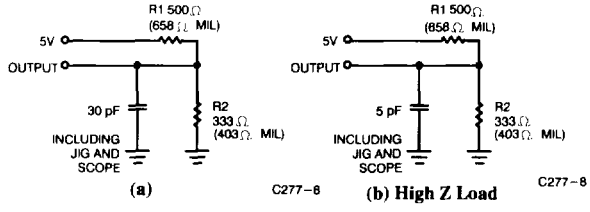
Electrical Characteristics Over the Operating Range[3, 4]

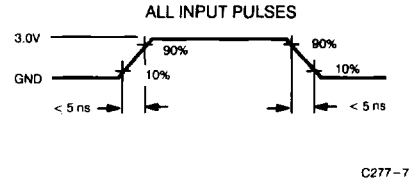
Parameters	Description	Test Conditions		7C277-30 7C279-35 Min.	7C277-30 7C279-35 Max.	7C277-40, 50 7C279-45, 55 Min.	7C277-40, 50 7C279-45, 55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$		−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Max., V_{IH} = 2.0V I_{OUT} = 0 mA		Note 6				
I_{OZ}	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$, Output Disabled[5]		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., CS ≥ V_{IH} I_{OUT} = 0 mA	Commercial		120		120	mA
			Military				130	
I_{SB}[7]	Standby Supply Current	V_{CC} = Max., CS ≥ V_{IH} I_{OUT} = 0 mA	Commercial		30		30	mA
			Military				40	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Capacitance[4]

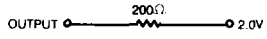
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[4]

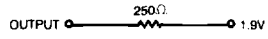




Equivalent to: THÉVENIN EQUIVALENT



Commercial



Military

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Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. See "Introduction to CMOS PROMs" in this Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Only the CY7C279 has a standby mode.

CY7C277 Switching Characteristics Over the Operating Range[3, 4]

Parameters	Description	7C277–30		7C277–40		7C277–50		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AL}	Address Setup to ALE Inactive	5		10		10		ns
t_{LA}	Address Hold from ALE Inactive	10		10		15		ns
t_{LL}	ALE Pulse Width	10		10		15		ns
t_{SA}	Address Setup to Clock HIGH	30		40		50		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		10		10		ns
t_{CO}	Clock HIGH to Output Valid		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{LZC}[8]	Output Low Z from Clock HIGH		15		20		30	ns
t_{HZC}[9]	Output High Z from Clock HIGH		15		20		30	ns
t_{LZE}[10]	Output Low Z from $\overline{E}$ LOW		15		20		30	ns
t_{HZE}[10]	Output High Z from $\overline{E}$ HIGH		15		20		30	ns

CY7C279 Switching Characteristics Over the Operating Range[3, 4]

Parameters	Description	7C279–35		7C279–45		7C279–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Data Valid (Latched Mode)		35		45		55	ns
t_{CO}	Clock to Output Valid (Registered Mode)		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20		20	ns
t_{ACS}	Chip Select Active to Output Valid		15		20		20	ns
t_{AR}	Address Setup to Clock Rise (Registered Mode)	3		10		10		ns
t_{RA}	Address Hold from Clock Rise (Registered Mode)	6		10		10		ns
t_{ADH}	Data Hold from Clock Rise (Registered Mode)	5		5		5		ns
t_{SU}	Address Setup to ALE Inactive (Latched Mode)	5		10		10		ns
t_{HD}	Address Hold from ALE Inactive (Latched Mode)	10		10		10		ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		40		50		60	ns
t_{OH}[11]	Output Hold from Address Change (Latched Mode)	0		0		0		ns
t_{PWA}	ALE Pulse Width	10		20		30		ns
t_{CESC}	Chip Enable Setup to Clock Rise	10		10		10		ns
t_{CESL}	Chip Enable Setup to Latch Close	10		10		10		ns
t_{CEV}	Chip Enable to ALE Active	40		50		60		ns

Notes:
8. Applies only when the synchronous ($\overline{E}_S$) function is used.
9. These parameters apply to the 7C279 only.
10. Applies only when the asynchronous ($\overline{E}$) function is used.
11. t_{AA} and t_{OH} apply only when the latched mode is selected.

Architecture Configuration Bits

Architecture Bit	Device	Architecture Verify $D_7 - D_0$		Function
ALE	7C277	D_1	0 = DEFAULT	Input Transparent
			1 = PGMED	Input Latched
ALE	7C279	D_1	0 = DEFAULT	Input Registered
			1 = PGMED	Input Latched
ALEP	7C277	D_2	0 = DEFAULT	ALE = Active HIGH
			1 = PGMED	ALE = Active LOW
ALEP	7C279	D_2	0 = DEFAULT	ALE = Active HIGH
			1 = PGMED	ALE = Active LOW
$\overline{E}/\overline{E}_S$	7C277	D_0	0 = DEFAULT	Asynchronous Output Enable ($\overline{E}$)
			1 = PGMED	Synchronous Output Enable ($\overline{E}_S$)

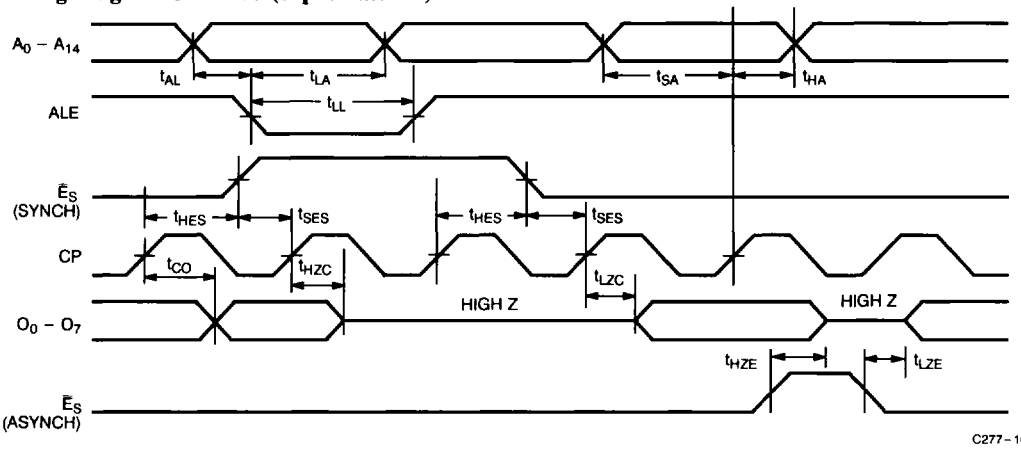
Bit Map

Programmer Address (Hex.)	RAM Data
0000	Data
.	.
.	.
.	.
7FFF	Data
8000	Control Byte

Architecture Byte (8000)

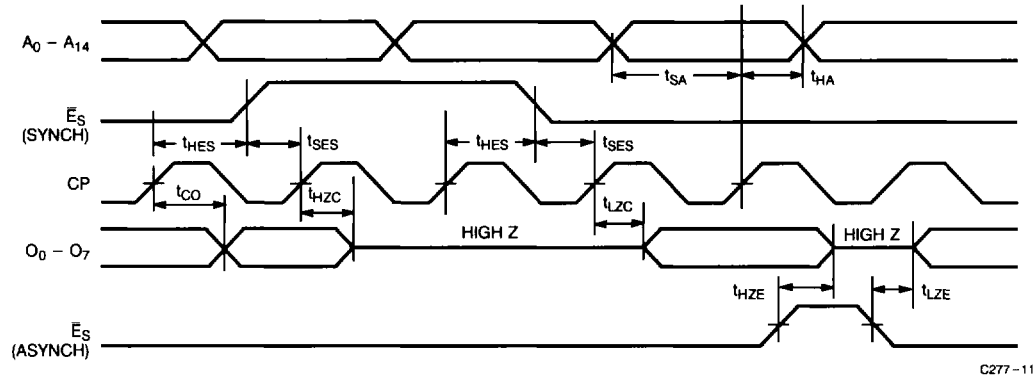
D_7							D_0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

Timing Diagram CY7C277 (Input Latched)[12]

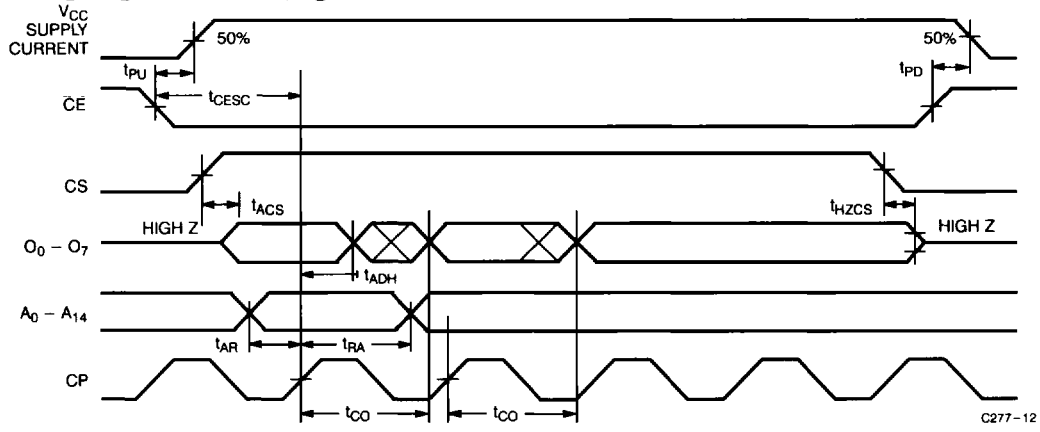


Notes:
12. ALE is shown with positive polarity.

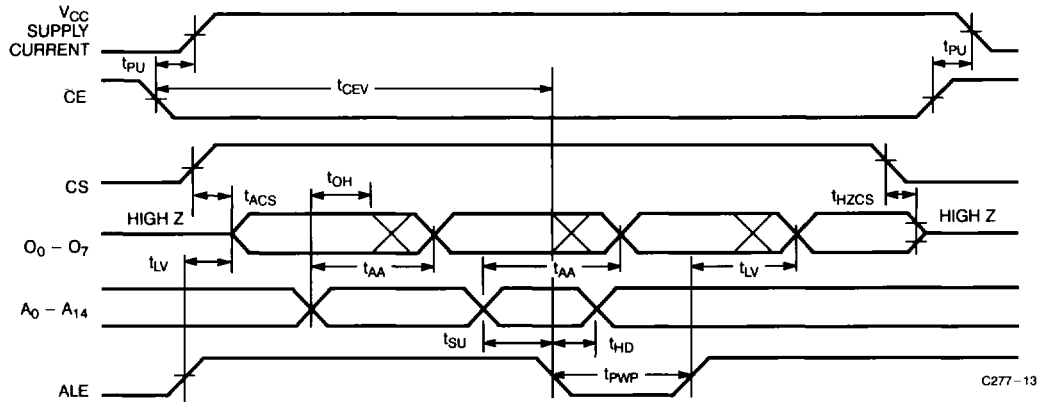
Timing Diagram CY7C277 (Input Transparent)



Timing Diagram CY7C279 (Registered)[12]



Timing Diagram CY7C279 (ALE)



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[13]				
	Read or Output Disable	$A_{14} - A_9$	$\overline{E}$, $\overline{E}_S$, or $\overline{CE}$	CP or CS	ALE or CP, ALE	$O_7 - O_8$
	Other	$A_{14} - A_9$	$\overline{VFY}$	$\overline{PGM}$	V_{PP}	$D_7 - D_8$
Read		$A_{14} - A_0$	V_{IL}	V_{IH}	V_{IL}	$O_7 - O_0$
Output Disable		$A_{14} - A_0$	V_{IH}	X	X	High Z
Program		$A_{14} - A_0$	V_{IHP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		$A_{14} - A_0$	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		$A_{14} - A_0$	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	$O_7 - O_0$

Notes:
13. X = "don't care" but not to exceed V_{CC} ±5%.

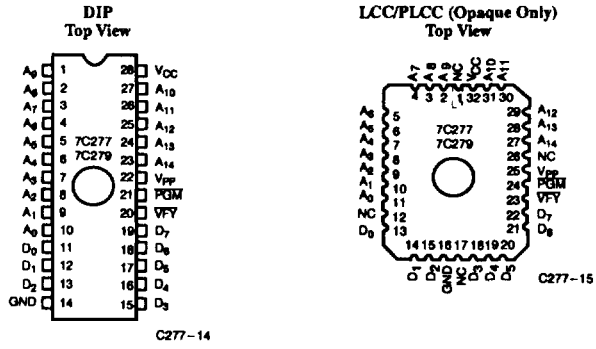
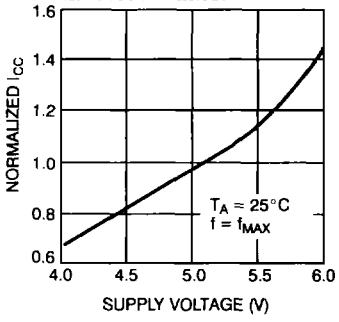


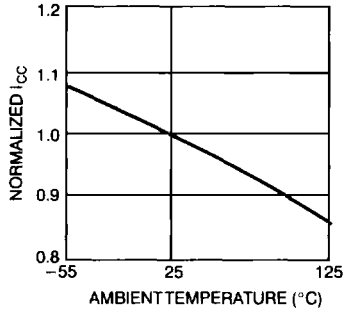
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

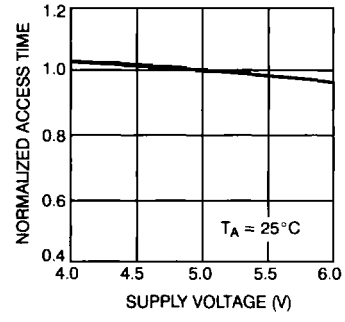
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



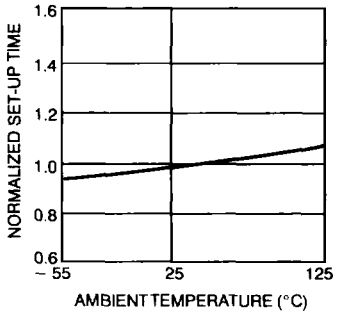
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



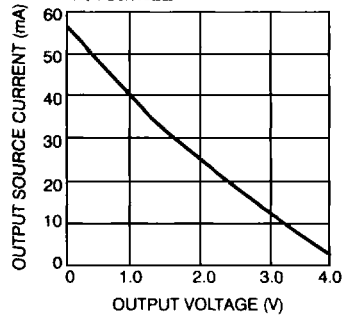
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



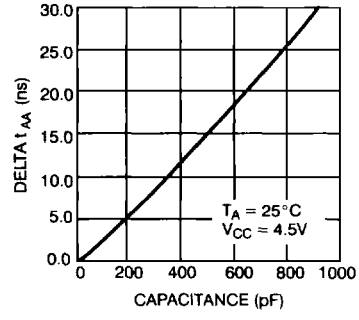
NORMALIZED SET-UP TIME vs. TEMPERATURE



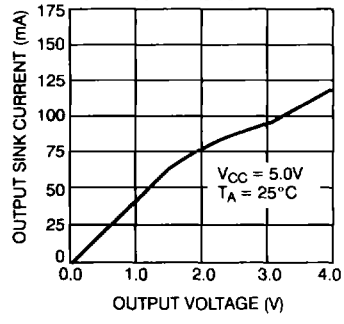
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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Ordering Information[14]

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C277-30DC	D22	Commercial
	CY7C277-30JC	J65	
	CY7C277-30PC	P21	
	CY7C277-30WC	W22	
40	CY7C277-40DC	D22	Commercial
	CY7C277-30JC	J65	
	CY7C277-30PC	P21	
	CY7C277-40WC	W22	
	CY7C277-40DMB	D22	Military
	CY7C277-40KMB	K74	
	CY7C277-40LMB	L55	
	CY7C277-40QMB	Q55	
	CY7C277-40TMB	T74	
	CY7C277-40WMB	W22	
50	CY7C277-50DC	D22	Commercial
	CY7C277-50JC	J65	
	CY7C277-50PC	P21	
	CY7C277-50WC	W22	
	CY7C277-50DMB	D22	Military
	CY7C277-50KMB	K74	
	CY7C277-50LMB	L55	
	CY7C277-50QMB	Q55	
	CY7C277-50TMB	T74	
	CY7C277-50WMB	W22	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C279-35DC	D22	Commercial
	CY7C279-35JC	J65	
	CY7C279-35PC	P21	
	CY7C279-35WC	W22	
45	CY7C279-45DC	D22	Commercial
	CY7C279-45JC	J65	
	CY7C279-45PC	P21	
	CY7C279-45WC	W22	
	CY7C279-45DMB	D22	Military
	CY7C279-45KMB	K74	
	CY7C279-45LMB	L55	
	CY7C279-45QMB	Q55	
	CY7C279-45TMB	T74	
	CY7C279-45WMB	W22	
55	CY7C279-55DC	D22	Commercial
	CY7C279-55JC	J65	
	CY7C279-55PC	P21	
	CY7C279-55WC	W22	
	CY7C279-55DMB	D22	Military
	CY7C279-55KMB	K74	
	CY7C279-55LMB	L55	
	CY7C279-55QMB	Q55	
	CY7C279-55TMB	T74	
	CY7C279-55WMB	W22	

Notes:
14. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[9]	1, 2, 3

Switching Characteristics

Device	Parameters	Subgroups
7C277	t_{SA}	7, 8, 9, 10, 11
	t_{HA}	7, 8, 9, 10, 11
	t_{CO}	7, 8, 9, 10, 11
7C279	t_{AR}	7, 8, 9, 10, 11
	t_{RA}	7, 8, 9, 10, 11
	t_{DHA}	7, 8, 9, 10, 11

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