

HM514410A/AL Series

T-46-23-18

1,048,576-Word × 4-Bit Dynamic RAM

HITACHI/ LOGIC/ARRAYS/MEM

Ordering Information

Type No.	Access time	Package
HM514410AS/ALS-7	70 ns	300-mil 20-pin plastic SOJ (CP-20D)
HM514410AS/ALS-8	80 ns	
HM514410AZ/ALZ-7	70 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514410AZ/ALZ-8	80 ns	

The Hitachi HM514410A/AL is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM514410A/AL has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514410A/AL offers fast page mode as a high speed access mode.

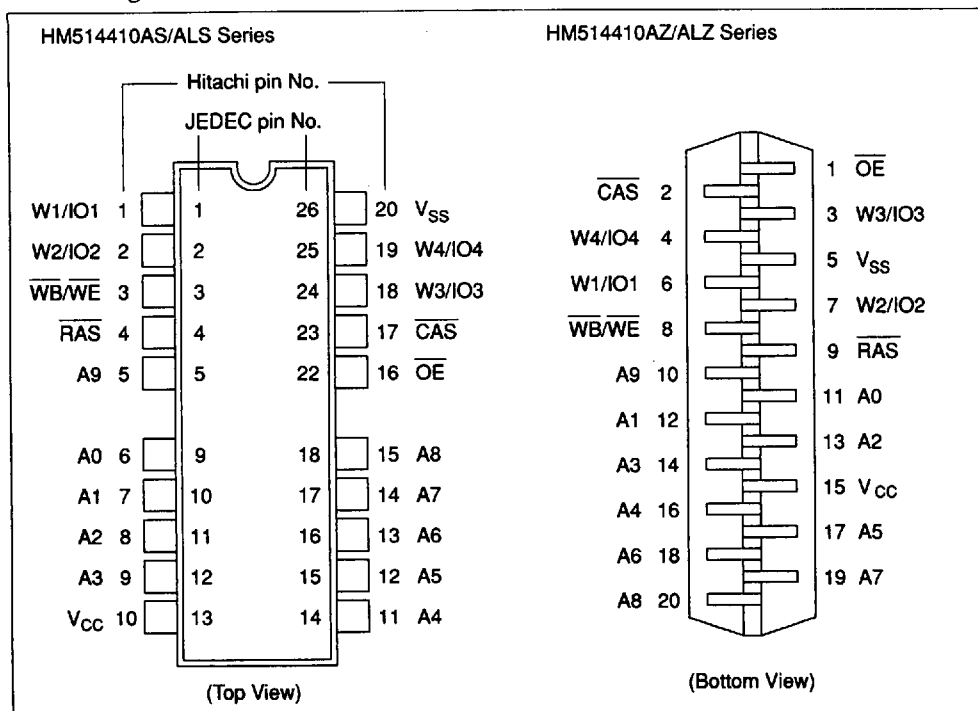
Multiplexed address input permits the HM514410A/AL to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Features

- Single 5 V (±10%)
- High speed
 - Access time: 70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 550 mW/495 mW (max)
 - Standby mode: 11 mW (max)
 - 0.83 mW (L-version)
- Fast page mode capability
- 1,024 refresh cycles: 16 ms
- 1,024 refresh cycles: 128 ms (L-version)
- 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- Test function
- Write per bit capability
- Battery back up operation (L-version)

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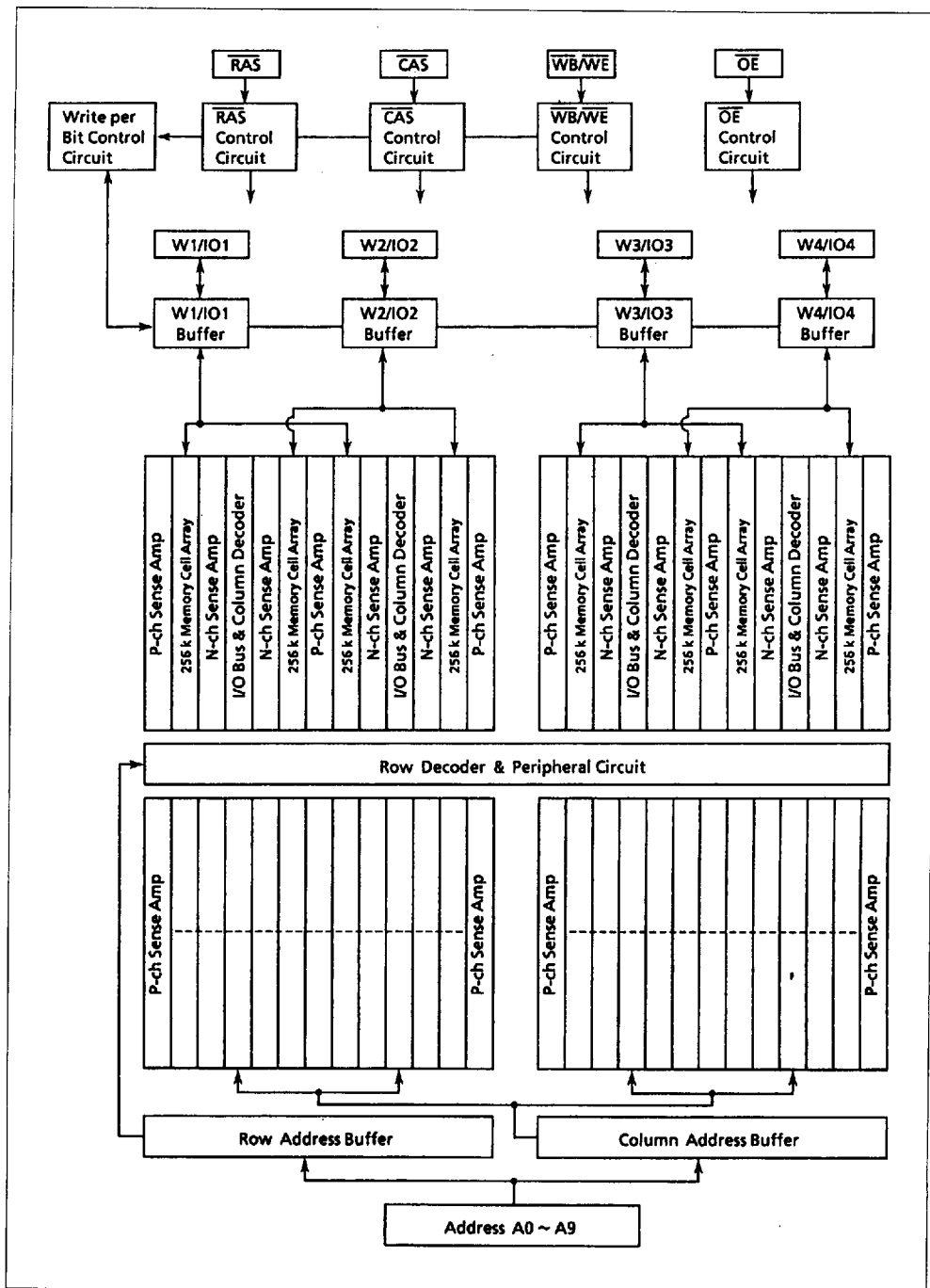
Pin Arrangement**Pin Description**

Pin Name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
W1/IO1 – W4/IO4	Write select/data-in/data-out
RAS	Row address strobe
CAS	Column address strobe
WB/WE	Write per bit/write enable
OE	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

HM514410A/AL Series

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Block Diagram



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Absolute Maximum Ratings

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Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
		4.0	—	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}

HM514410A/AL Series
DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I_{CC1}	—	100	—	90	mA	RAS, CAS cycling $t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface RAS, CAS = V_{IH} Dout = High-Z	
		—	1	—	1	mA	CMOS interface RAS, CAS $\geq$ $V_{CC} - 0.2\text{ V}$ Dout = High-Z	
Standby current (L-version)		—	150	—	150	μA	CMOS interface RAS, CAS = V_{IH} WE, OE, address, Din = V_{IH} or V_{IL} Dout = High-Z	4
RAS-only refresh current	I_{CC3}	—	100	—	90	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	5	—	5	mA	RAS = V_{IH} CAS = V_{IL} Dout = enable	1
CAS-before-RAS refresh current	I_{CC6}	—	100	—	90	mA	$t_{RC} = \min$	
Fast page mode current	I_{CC7}	—	100	—	90	mA	$t_{PC} = \min$	1, 3
Battery back up operation current (CBR refresh) (L-version)	I_{CC10}	—	200	—	200	μA	$t_{RC} = 125\text{ }\mu\text{s}$ $t_{RAS} \leq 1\text{ }\mu\text{s}$ WE = V_{IH} , CAS = V_{IL} , OE, address, Din = V_{IH} or V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 7\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed twice or less while RAS = V_{IL} .

3. Address can be changed once or less while CAS = V_{IH} .

4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$, $0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, data-out)	$C_{I/O}$	—	10	pF	1, 2

- Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $CAS = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *14, *15, *16

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate $+C_L$ (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
RAS precharge time	t_{RP}	50	—	60	—	ns	
RAS pulse width	t_{RAS}	70	10000	80	10000	ns	21
CAS pulse width	t_{CAS}	20	10000	20	10000	ns	22
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	ns	
RAS to CAS delay time	t_{RCD}	20	50	20	60	ns	8
RAS to column address delay time	t_{RAD}	15	35	15	40	ns	9
RAS hold time	t_{RSH}	20	—	20	—	ns	
CAS hold time	t_{CSH}	70	—	80	—	ns	
CAS to RAS precharge time	t_{CRP}	10	—	10	—	ns	
OE to Din delay time	t_{ODD}	20	—	20	—	ns	

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Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (cont)

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
OE delay time from Din	t_{DZO}	0	—	0	—	ns	
CAS setup time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
Access time from RAS	t_{RAC}	—	70	—	80	ns	2, 3, 17
Access time from CAS	t_{CAC}	—	20	—	20	ns	3, 4, 13, 17
Access time from Address	t_{AA}	—	35	—	40	ns	3, 5, 13, 17
Access time from OE	t_{OAC}	—	20	—	20	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to CAS	t_{RCH}	0	—	0	—	ns	20
Read command hold time to RAS	t_{RRH}	0	—	0	—	ns	20
Column address to RAS lead time	t_{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	20	ns	6
Output buffer turn-off to OE	t_{OFF2}	0	20	0	20	ns	6
CAS to Din delay time	t_{CDD}	20	—	20	—	ns	
OE pulse width	t_{OEP}	20	—	20	—	ns	

HM514410A/AL Series
Write Cycle
HITACHI/ LOGIC/ARRAYS/MEM
HM514410A-7 HM514410A-8

Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	ns	11

Read-Modify-Write Cycle
HM514410A-7 HM514410A-8

Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	200	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	95	—	105	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	ns	10
OE hold time from $\overline{WE}$	t_{OEh}	20	—	20	—	ns	

Refresh Cycle
HM514410A-7 HM514410A-8

Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	ns	

HM514410A/AL Series

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Fast Page Mode Cycle

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
Fast page mode cycle time	t _{PC}	45	—	50	—	ns	
Fast page mode $\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASC}	—	100000	—	100000	ns	12
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	40	—	45	ns	3, 13, 17
RAS hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
Fast page mode read modify-write cycle time	t _{PCM}	95	—	100	—	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPW}	65	—	70	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
Test mode $\overline{\text{WE}}$ setup time	t _{WS}	0	—	0	—	ns	
Test mode $\overline{\text{WE}}$ hold time	t _{WH}	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
$\overline{\text{CAS}}$ precharge time in counter test cycle	t _{CPT}	40	—	40	—	ns	

Write Per Bit *18, *19

Parameter	Symbol	HM514410A-7		HM514410A-8		Unit	Notes
		Min	Max	Min	Max		
Write per bit setup time	t_{WBS}	0	—	0	—	ns	
Write per bit hold time	t_{WBH}	15	—	15	—	ns	
Write per bit selection setup time	t_{WDS}	0	—	0	—	ns	
Write per bit selection hold time	t_{WDH}	15	—	15	—	ns	

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \geq t_{RAD}(\max)$.
 6. $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RAD}(\max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPW} \geq t_{CPW}(\min)$ the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to WE leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines RAS pulse width in fast page mode cycles.
 13. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μ s is required after power up followed by a minimum of eight initialization cycles (RAS -only refresh cycle or $\overline{CAS}$ -before- RAS refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- RAS refresh cycles is required.
 15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
 16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits — $CA0$. This test mode operation can be performed by WB/WE -and- $\overline{CAS}$ -before- RAS ($WCBR$) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by $WCBR$ refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a RAS -only refresh cycle or a $\overline{CAS}$ -before- RAS refresh cycle.

HM514410A/AL Series

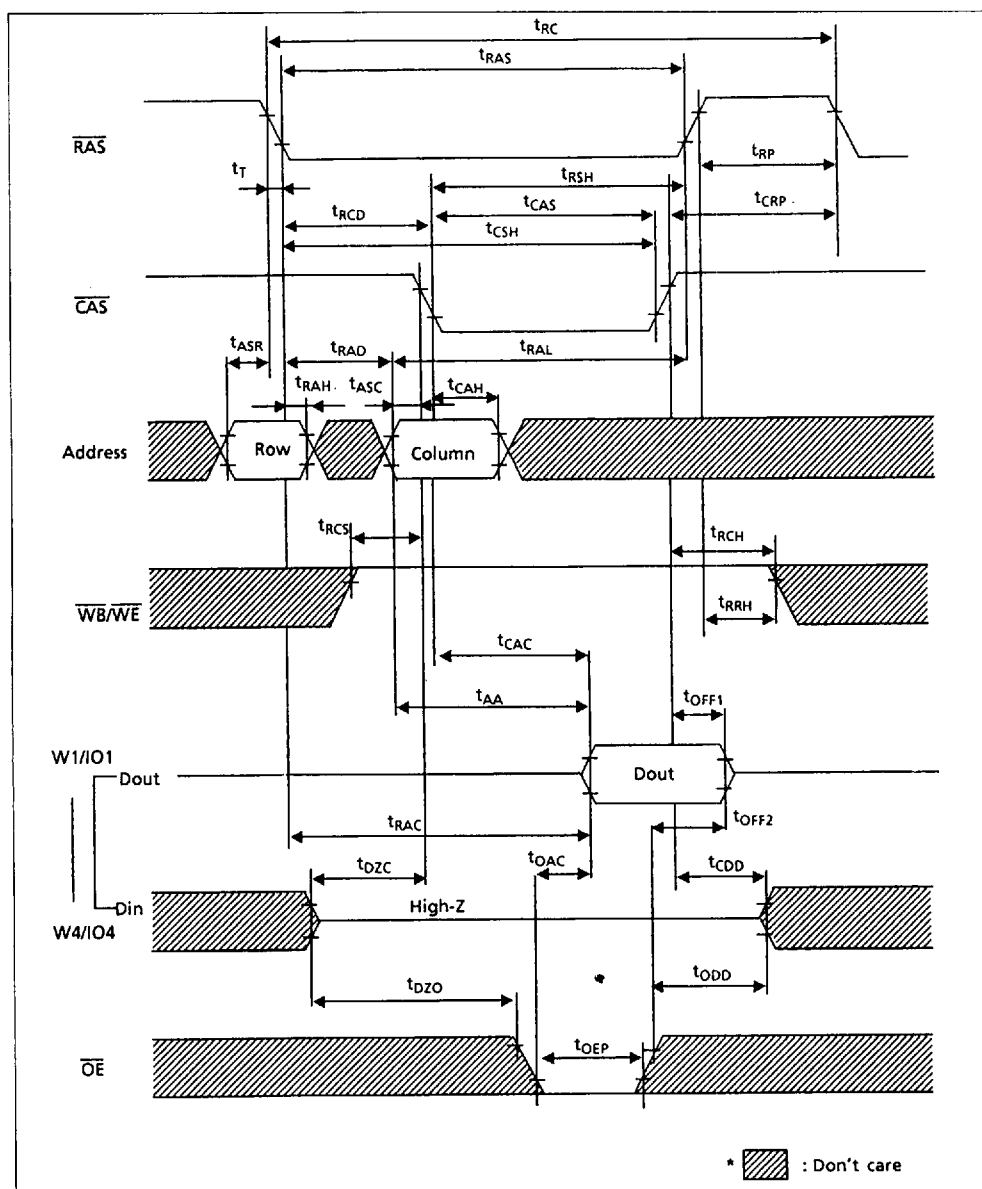
17. In a test mode read cycle, the value of t_{RAC} , t_{CAC} , t_{AA} , t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
19. The data bits to which the write operation is applied can be specified by keeping $W1/IO1$, $W2/IO2$, $W3/IO3$ and $W4/IO4$ high with setup and hold time referenced to the $\overline{RAS}$ negative transition.
20. Either t_{RCH} or t_{RRH} shall be satisfied.
21. $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle.
22. $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write cycle.

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Timing Waveforms

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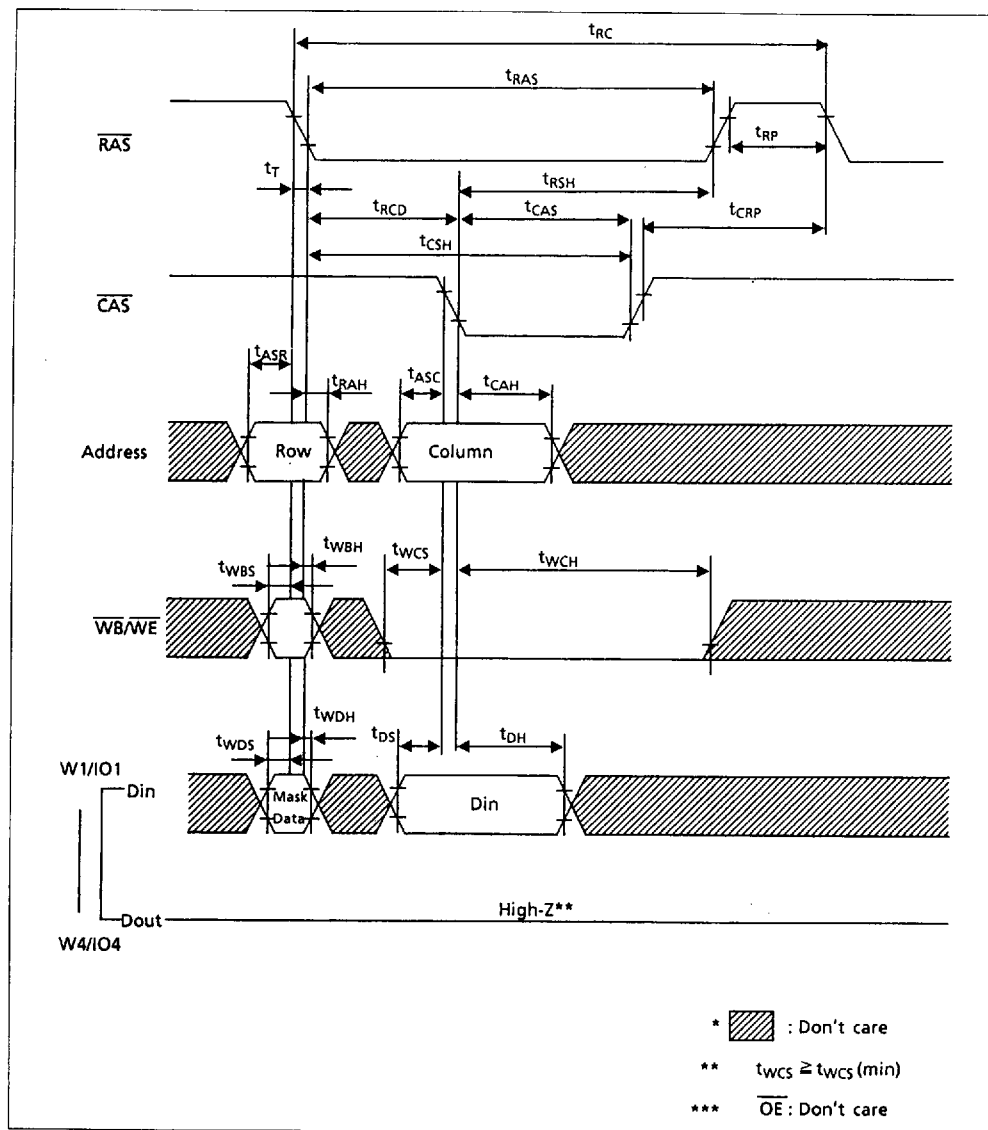
Read Cycle



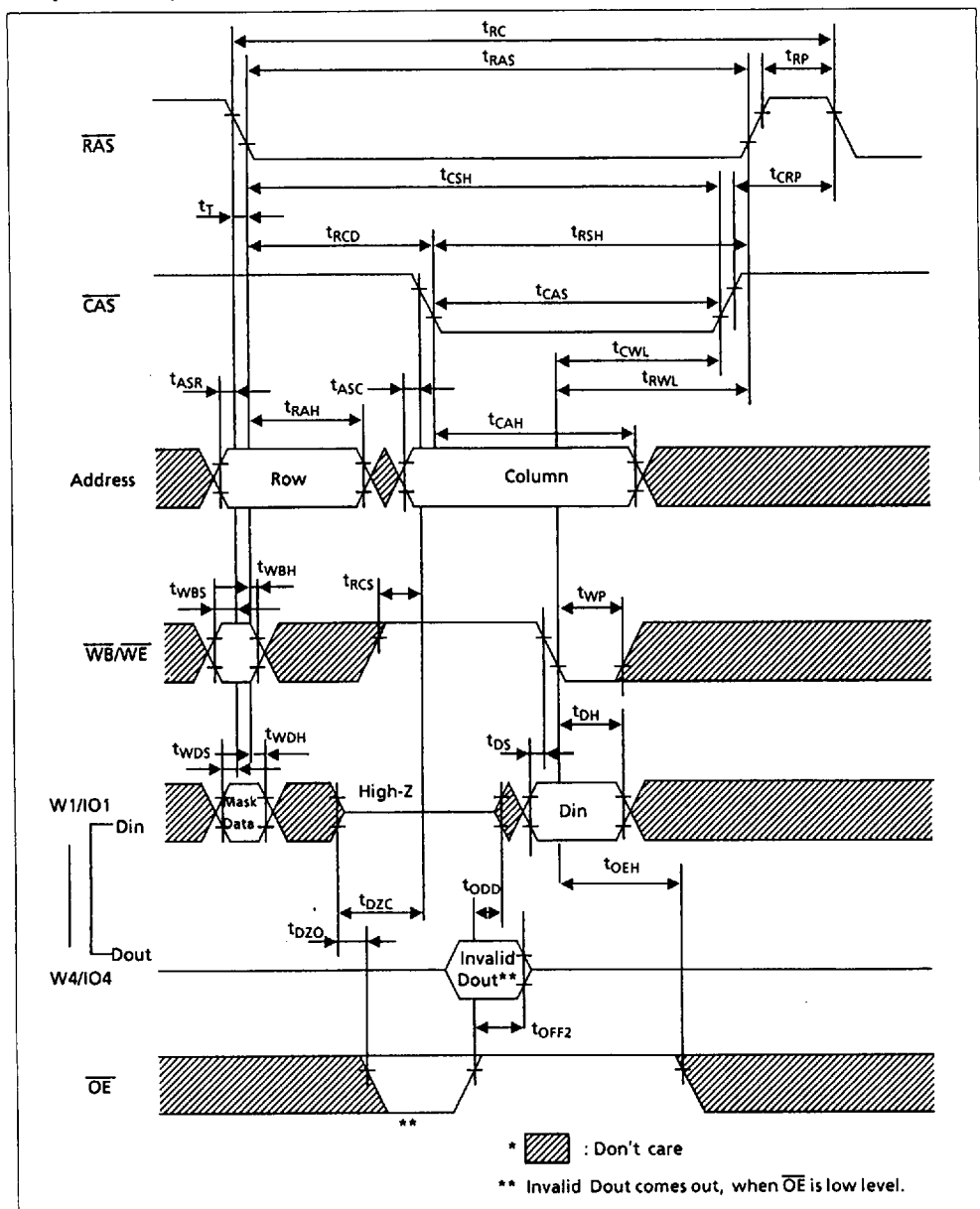
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Early Write Cycle

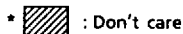


Delayed Write Cycle

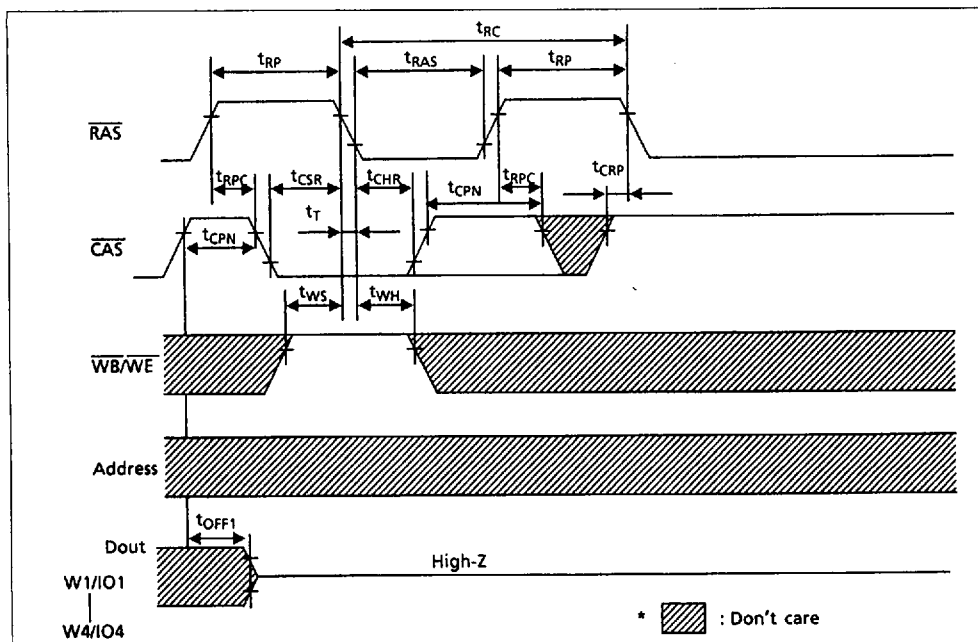


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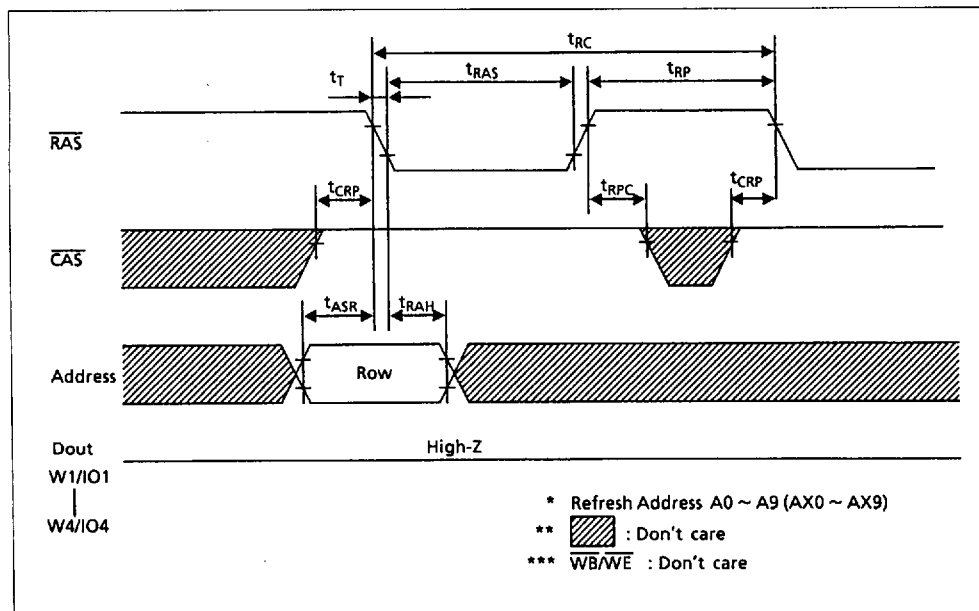
Read-Modify-Write Cycle



CAS-Before-RAS Refresh Cycle



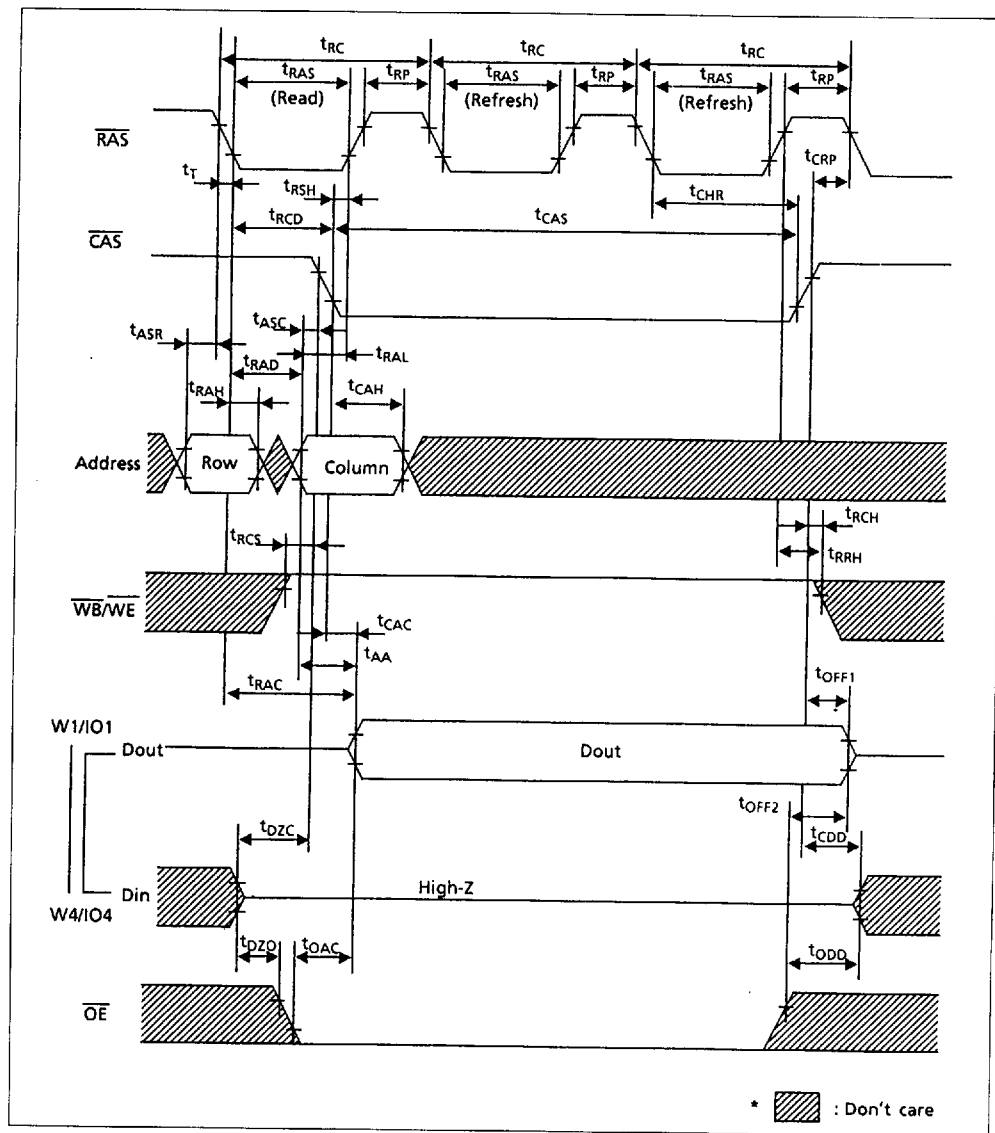
RAS-Only Refresh Cycle



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Hidden Refresh Cycle

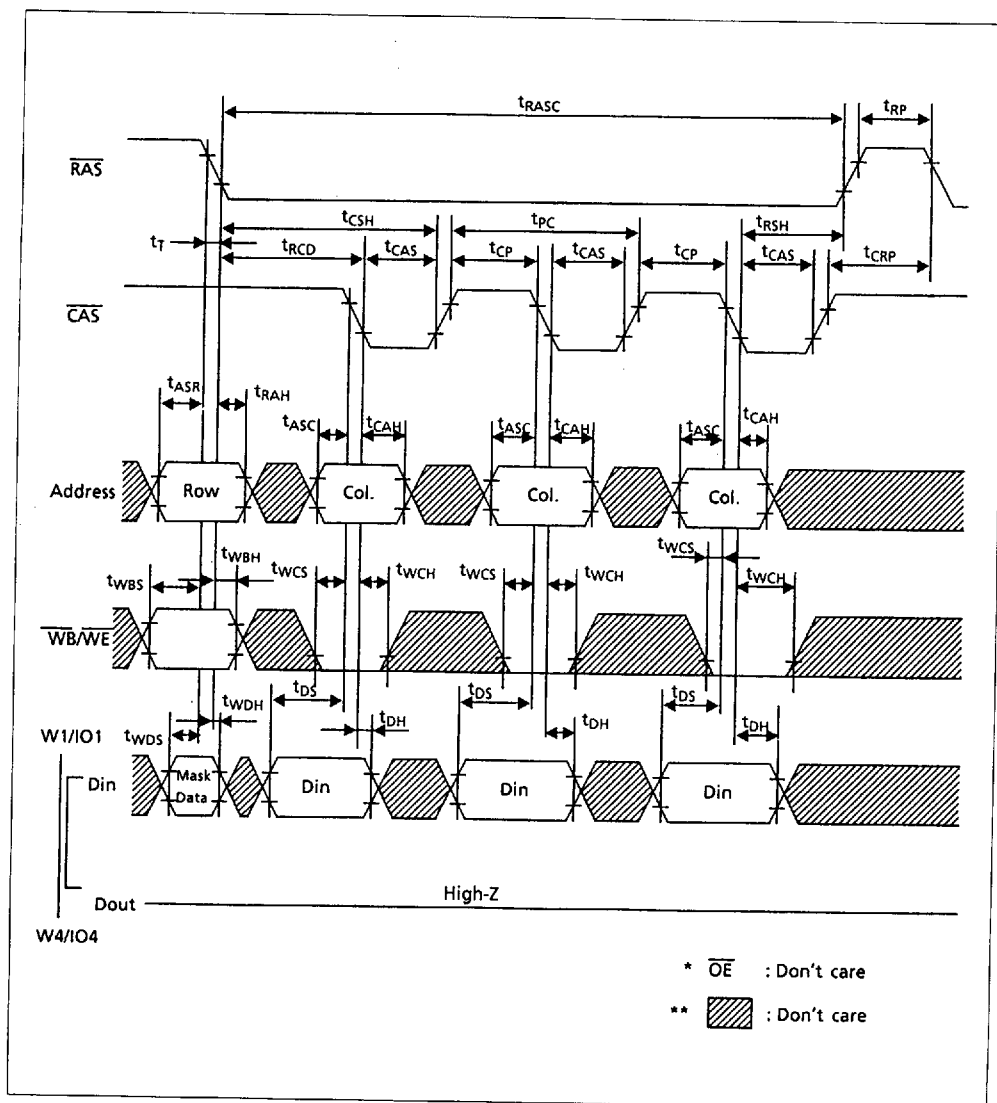




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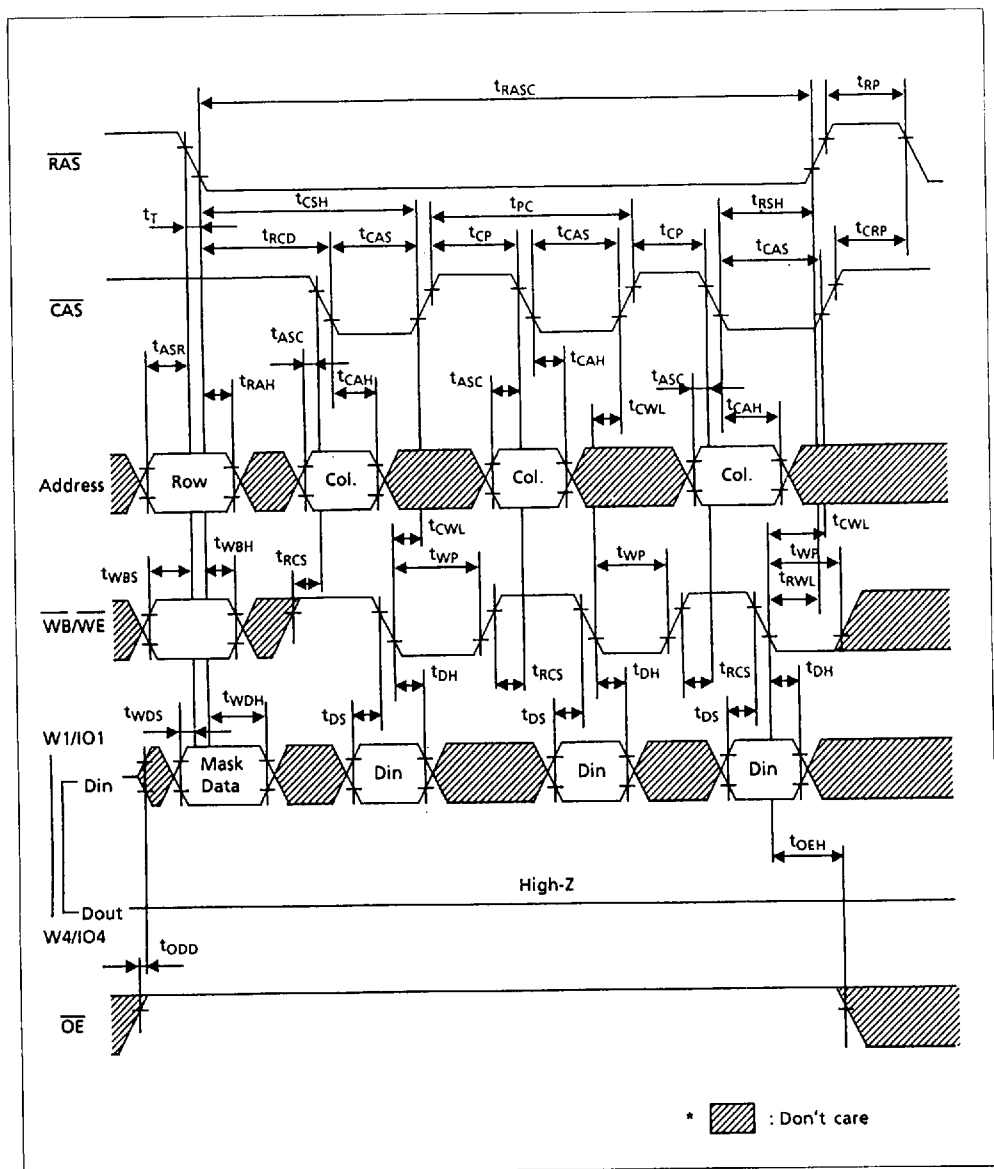
HITACHI/ LOGIC/ARRAYS/MEM —

Fast Page Mode Early Write Cycle



HITACHI/ LOGIC/ARRAYS/MEM **HM514410A/AL Series**

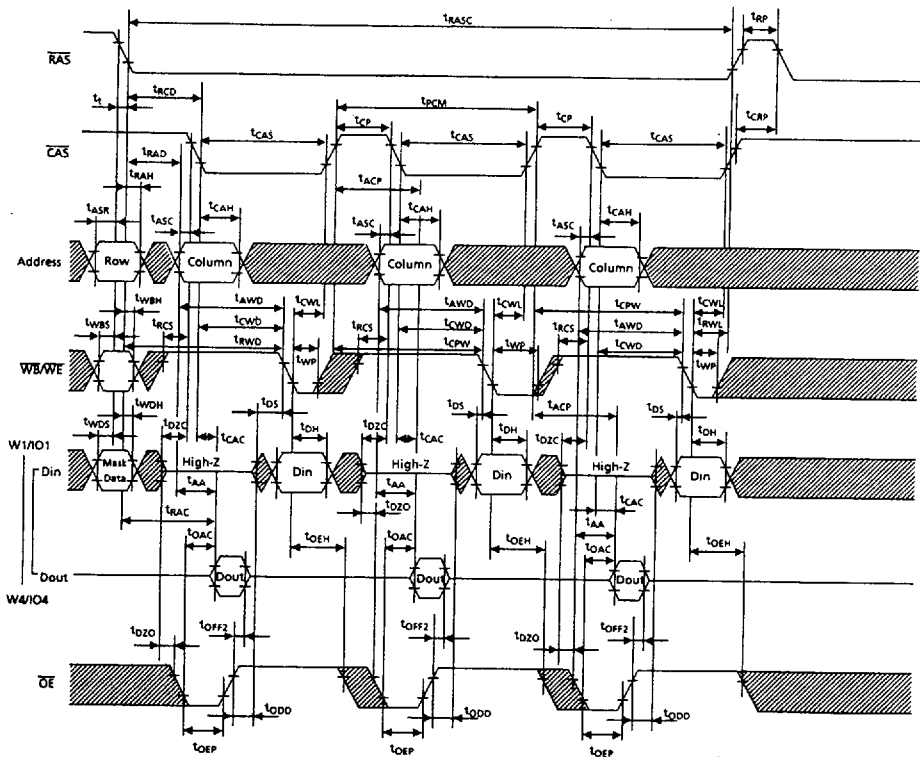
Fast Page Delayed Write Cycle



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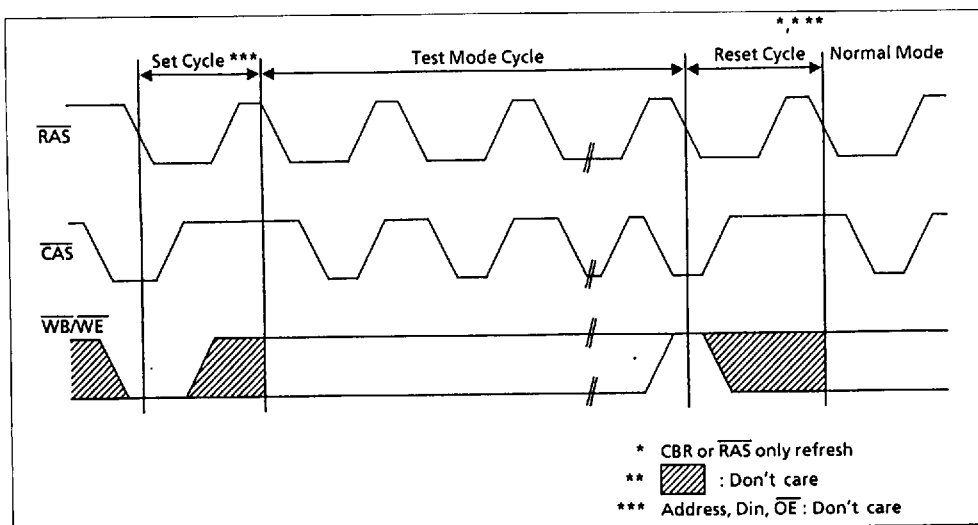
HITACHI/ LOGIC/ARRAYS/MEM -

Fast Page Mode Read-Modify-Write Cycle

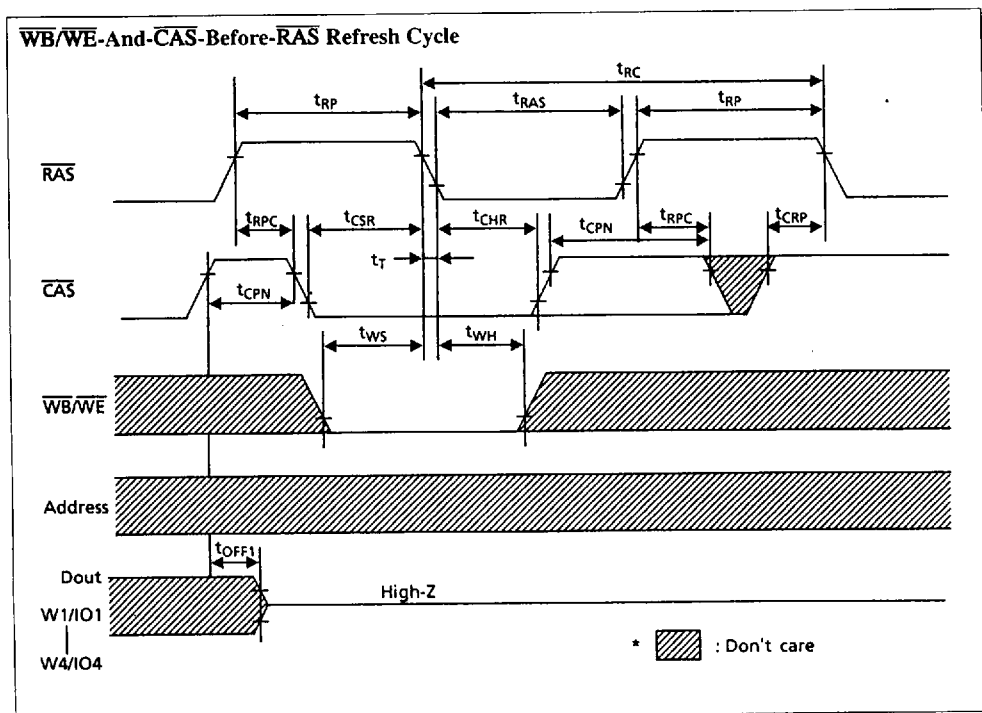


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Test Mode Cycle

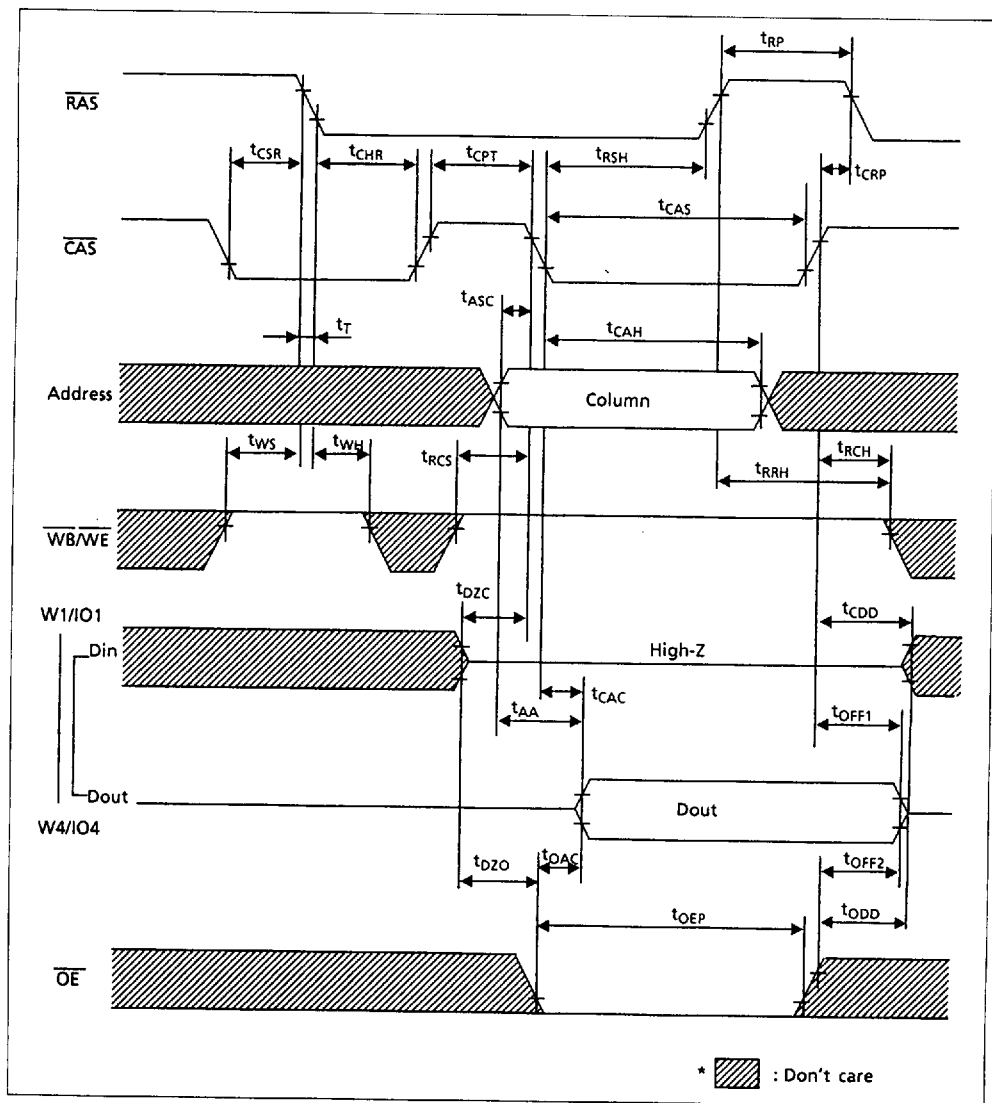


Test Mode Set Cycle



HM514410A/AL Series HITACHI/ LOGIC/ARRAYS/MEM —

CAS-Before-RAS Refresh Counter Check Cycle (Read)



CAS-Before-RAS Refresh Counter Check Cycle (Write)

