

HYS64D[16/32/64][300/301/320][G/H]U-5-C  
HYS72D[32/64][300/301/320][G/H]U-5-C  
HYS64D[16/32/64][300/301/320][G/H]U-6-C  
HYS72D[32/64][300/301/320][G/H]U-6-C

*184- Pin Unbuffered DDR SDRAM Modules  
UDIMM  
DDR SDRAM*



## Internet Data Sheet

*Rev. 1.11*

HYS[64/72]D[16/32/64][300/301/320][G/H]U-[5/6]-C  
Unbuffered DDR SDRAM ModulesHYS64D[16/32/64][300/301/320][G/H]U-5-C, HYS72D[32/64][300/301/320][G/H]U-5-C,  
HYS64D[16/32/64][300/301/320][G/H]U-6-C, HYS72D[32/64][300/301/320][G/H]U-6-C

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# 1 Overview

## 1.1 Features

- 184-Pin Unbuffered Double Data Rate SDRAM (ECC and non-parity) for PC and Server main memory applications
- One rank 16M x 64, 32M x 64, 32M x 72 and two ranks 64M x 64, 64M x 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) Single +2.5V (±0.2V) power supply and +2.6V (±0.1V) power supply for DDR400
- Built with 256 Mbit DDR SDRAM in P-TSOP168 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL\_2 compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- JEDEC standard MO-206 form factor: 133.35 mm x 31.75 mm x 4.00 mm max.
- JEDEC standard reference layout
- Gold plated contacts
- DDR400 Speed Grade supported

**Table 1 Performance**

Product Type Speed Code			-5	-6	Unit
Module Speed Grade			DDR400B	DDR333B	—
Component Module			PC3200-3033	PC2700-2533	—
Max. Clock Frequency	@ CL = 3	$f_{CK3}$	200	166	MHz
	@ CL = 2.5	$f_{CK2.5}$	166	166	MHz
	@ CL = 2	$f_{CK2}$	133	133	MHz

## 1.2 Description

The HYS64D[16/32/64][300/301/320][G/H]U-5-C, HYS72D[32/64][300/301/320][G/H]U-5-C, HYS64D[16/32/64][300/301/320][G/H]U-6-C and HYS72D[32/64][300/301/320][G/H]U-6-C are industry standard 184-Pin Unbuffered Double Data Rate SDRAM (UDIMM) organized as 16M x 64, 32M x 64 and 64M x 64 for non-parity and 32M x 72 and 64M x 72 for ECC main memory applications. The memory array is designed with 256Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial E<sup>2</sup>PROM device using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer



**Table 2 Ordering Information for Lead-Free Products**

Product Type <sup>2)</sup>	Compliance Code	Description	SDRAM Technology
<b>PC3200 (CL=3)</b>			
HYS64D16301GU-5-C	PC3200U-30330-C0	one rank 128MB DIMM	256 Mbit (×16)
HYS64D32300GU-5-C	PC3200U-30330-A0	one rank 256MB DIMM	256 Mbit (×8)
HYS72D32300GU-5-C	PC3200U-30330-A0	one rank 256MB ECC-DIMM	256 Mbit (×8)
HYS64D64320GU-5-C	PC3200U-30330-B0	two ranks 512MB DIMM	256 Mbit (×8)
HYS72D64320GU-5-C	PC3200U-30330-B0	two ranks 512MB ECC-DIMM	256 Mbit (×8)
<b>PC2700 (CL=2.5)</b>			
HYS64D16301GU-6-C	PC2700U-25330-C0	one rank 128MB DIMM	256 Mbit (×16)
HYS64D32300GU-6-C	PC2700U-25330-A0	one rank 256MB DIMM	256 Mbit (×8)
HYS72D32300GU-6-C	PC2700U-25330-A0	one rank 256MB ECC-DIMM	256 Mbit (×8)
HYS64D64320GU-6-C	PC2700U-25330-B0	two ranks 512MB DIMM	256 Mbit (×8)
HYS72D64320GU-6-C	PC2700U-25330-B0	two ranks 512MB ECC-DIMM	256 Mbit (×8)



**Table 3 Ordering Information for Lead-Free (RoHS<sup>1)</sup> Compliant Products)**

Product Type <sup>2)</sup>	Compliance Code	Description	SDRAM Technology
<b>PC3200 (CL=3)</b>			
HYS64D16301HU-5-C	PC3200U-30330-C0	one rank 128MB DIMM	256 Mbit (×16)
HYS64D32300HU-5-C	PC3200U-30330-A0	one rank 256MB DIMM	256 Mbit (×8)
HYS72D32300HU-5-C	PC3200U-30330-A0	one rank 256MB ECC-DIMM	256 Mbit (×8)
HYS64D64320HU-5-C	PC3200U-30330-B0	two ranks 512MB DIMM	256 Mbit (×8)
HYS72D64320HU-5-C	PC3200U-30330-B0	two ranks 512MB ECC-DIMM	256 Mbit (×8)
<b>PC2700 (CL=2.5)</b>			
HYS64D16301HU-6-C	PC2700U-25330-C0	one rank 128MB DIMM	256 Mbit (×16)
HYS64D32300HU-6-C	PC2700U-25330-A0	one rank 256MB DIMM	256 Mbit (×8)
HYS72D32300HU-6-C	PC2700U-25330-A0	one rank 256MB ECC-DIMM	256 Mbit (×8)
HYS64D64320HU-6-C	PC2700U-25330-B0	two ranks 512MB DIMM	256 Mbit (×8)
HYS72D64320HU-6-C	PC2700U-25330-B0	two ranks 512MB ECC-DIMM	256 Mbit (×8)

- 1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.
- 2) All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D32000HU-6-C, indicating rev. C dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example "PC2700"), the latencies and SPD code definition (for example "20330" means CAS latency of 2.0 clocks, Row-Column-Delay (RCD) latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definition version 0), and the Raw Card used for this module.



## 2 Pin Configuration

The pin configuration of the Unbuffered DDR SDRAM DIMM is listed by function in **Table 4** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 5** and **Table 6** respectively. The pin numbering is depicted in **Figure 1**.

**Table 4 Pin Configuration of UDIMM**

Pin#	Name	Pin Type	Buffer Type	Function
<b>Clock Signals</b>				
137	CK0	I	SSTL	<b>Clock Signals 2:0</b>
	NC	NC	—	
16	CK1	I	SSTL	<b>Complement Clock Signals 2:0</b>
76	CK2	I	SSTL	
138	$\overline{\text{CK0}}$	I	SSTL	<b>Complement Clock Signals 2:0</b>
	NC	NC	—	
17	$\overline{\text{CK1}}$	I	SSTL	<b>Complement Clock Signals 2:0</b>
75	$\overline{\text{CK2}}$	I	SSTL	
21	CKE0	I	SSTL	<b>Clock Enable Rank 0</b>
111	CKE1	I	SSTL	<b>Clock Enable Rank 1</b> <i>Note: 2-rank module</i>
	NC	NC	—	<i>Note: 1-rank module</i>
<b>Control Signals</b>				
157	$\overline{\text{S0}}$	I	SSTL	<b>Chip Select Rank 0</b>
158	$\overline{\text{S1}}$	I	SSTL	<b>Chip Select Rank 1</b> <i>Note: 2-rank module</i>
	NC	NC	—	<i>Note: 1-rank module</i>
154	$\overline{\text{RAS}}$	I	SSTL	<b>Row Address Strobe</b>
65	$\overline{\text{CAS}}$	I	SSTL	<b>Column Address Strobe</b>
63	$\overline{\text{WE}}$	I	SSTL	<b>Write Enable</b>
<b>Address Signals</b>				
59	BA0	I	SSTL	<b>Bank Address Bus 2:0</b>
52	BA1	I	SSTL	
48	A0	I	SSTL	<b>Address Bus 11:0</b>
43	A1	I	SSTL	
41	A2	I	SSTL	
130	A3	I	SSTL	
37	A4	I	SSTL	
32	A5	I	SSTL	
125	A6	I	SSTL	
29	A7	I	SSTL	

**Table 4 Pin Configuration of UDIMM (cont'd)**

Pin#	Name	Pin Type	Buffer Type	Function
122	A8	I	SSTL	<b>Address Bus 11:0</b>
27	A9	I	SSTL	
141	A10	I	SSTL	
	AP	I	SSTL	<b>Address Signal 12</b> <i>Note: Module based on 256 Mbit or larger dies</i>
118	A11	I	SSTL	
115	A12	I	SSTL	
	NC	NC	—	<i>Note: 128 Mbit based module</i>
167	A13	I	SSTL	<b>Address Signal 13</b> <i>Note: 1 Gbit based module</i>
	NC	NC	—	<i>Note: Module based on 512 Mbit or smaller dies</i>
<b>Data Signals</b>				
2	DQ0	I/O	SSTL	<b>Data Bus 63:0</b>
4	DQ1	I/O	SSTL	
6	DQ2	I/O	SSTL	
8	DQ3	I/O	SSTL	
94	DQ4	I/O	SSTL	
95	DQ5	I/O	SSTL	
98	DQ6	I/O	SSTL	
99	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
19	DQ10	I/O	SSTL	
20	DQ11	I/O	SSTL	
105	DQ12	I/O	SSTL	
106	DQ13	I/O	SSTL	
109	DQ14	I/O	SSTL	
110	DQ15	I/O	SSTL	
23	DQ16	I/O	SSTL	
24	DQ17	I/O	SSTL	
28	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
114	DQ20	I/O	SSTL	
117	DQ21	I/O	SSTL	



**Table 4 Pin Configuration of UDIMM (cont'd)**

Pin#	Name	Pin Type	Buffer Type	Function
121	DQ22	I/O	SSTL	<b>Data Bus 63:0</b>
123	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
35	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
126	DQ28	I/O	SSTL	
127	DQ29	I/O	SSTL	
131	DQ30	I/O	SSTL	
133	DQ31	I/O	SSTL	
53	DQ32	I/O	SSTL	
55	DQ33	I/O	SSTL	
57	DQ34	I/O	SSTL	
60	DQ35	I/O	SSTL	
146	DQ36	I/O	SSTL	
147	DQ37	I/O	SSTL	
150	DQ38	I/O	SSTL	
151	DQ39	I/O	SSTL	
61	DQ40	I/O	SSTL	
64	DQ41	I/O	SSTL	
68	DQ42	I/O	SSTL	
69	DQ43	I/O	SSTL	
153	DQ44	I/O	SSTL	
155	DQ45	I/O	SSTL	
161	DQ46	I/O	SSTL	
162	DQ47	I/O	SSTL	
72	DQ48	I/O	SSTL	
73	DQ49	I/O	SSTL	
79	DQ50	I/O	SSTL	
80	DQ51	I/O	SSTL	
165	DQ52	I/O	SSTL	
166	DQ53	I/O	SSTL	
170	DQ54	I/O	SSTL	
171	DQ55	I/O	SSTL	
83	DQ56	I/O	SSTL	
84	DQ57	I/O	SSTL	
87	DQ58	I/O	SSTL	
88	DQ59	I/O	SSTL	
174	DQ60	I/O	SSTL	
175	DQ61	I/O	SSTL	

**Table 4 Pin Configuration of UDIMM (cont'd)**

Pin#	Name	Pin Type	Buffer Type	Function
178	DQ62	I/O	SSTL	<b>Data Bus 63:0</b>
179	DQ63	I/O	SSTL	
44	CB0	I/O	SSTL	<b>Check Bit 0</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
45	CB1	I/O	SSTL	<b>Check Bit 1</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
49	CB2	I/O	SSTL	<b>Check Bit 2</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
51	CB3	I/O	SSTL	<b>Check Bit 3</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
134	CB4	I/O	SSTL	<b>Check Bit 4</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
135	CB5	I/O	SSTL	<b>Check Bit 5</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
142	CB6	I/O	SSTL	<b>Check Bit 6</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
144	CB7	I/O	SSTL	<b>Check Bit 7</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
5	DQS0	I/O	SSTL	<b>Data Strobe Bus 7:0</b>
14	DQS1	I/O	SSTL	
25	DQS2	I/O	SSTL	
36	DQS3	I/O	SSTL	
56	DQS4	I/O	SSTL	
67	DQS5	I/O	SSTL	
78	DQS6	I/O	SSTL	
86	DQS7	I/O	SSTL	
47	DQS8	I/O	SSTL	<b>Data Strobe 8</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>



**Table 4 Pin Configuration of UDIMM (cont'd)**

Pin#	Name	Pin Type	Buffer Type	Function
97	DM0	I	SSTL	<b>Data Mask Bus 7:0</b>
107	DM1	I	SSTL	
119	DM2	I	SSTL	
129	DM3	I	SSTL	
149	DM4	I	SSTL	
159	DM5	I	SSTL	
169	DM6	I	SSTL	
177	DM7	I	SSTL	
140	DM8	I	SSTL	<b>Data Mask 8</b> <i>Note: ECC type module</i>
	NC	NC	—	<i>Note: Non-ECC module</i>
<b>EEPROM</b>				
92	SCL	I	CMOS	<b>Serial Bus Clock</b>
91	SDA	I/O	OD	<b>Serial Bus Data</b>
181	SA0	I	CMOS	<b>Slave Address Select Bus 2:0</b>
182	SA1	I	CMOS	
183	SA2	I	CMOS	
<b>Power Supplies</b>				
1	$V_{REF}$	AI	—	<b>I/O Reference Voltage</b>
184	$V_{DDSPD}$	PWR	—	<b>EEPROM Power Supply</b>
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	$V_{DDQ}$	PWR	—	<b>I/O Driver Power Supply</b>

**Table 4 Pin Configuration of UDIMM (cont'd)**

Pin#	Name	Pin Type	Buffer Type	Function
7, 38, 46, 70, 85, 108, 120, 148, 168	$V_{DD}$	PWR	—	<b>Power Supply</b>
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	$V_{SS}$	GND	—	<b>Ground Plane</b>
<b>Other Pins</b>				
82	$V_{DDID}$	O	OD	$V_{DD}$ Identification
9, 10, 71, 90, 101, 102, 103, 113, 163, 173	NC	NC	—	<b>Not connected</b>

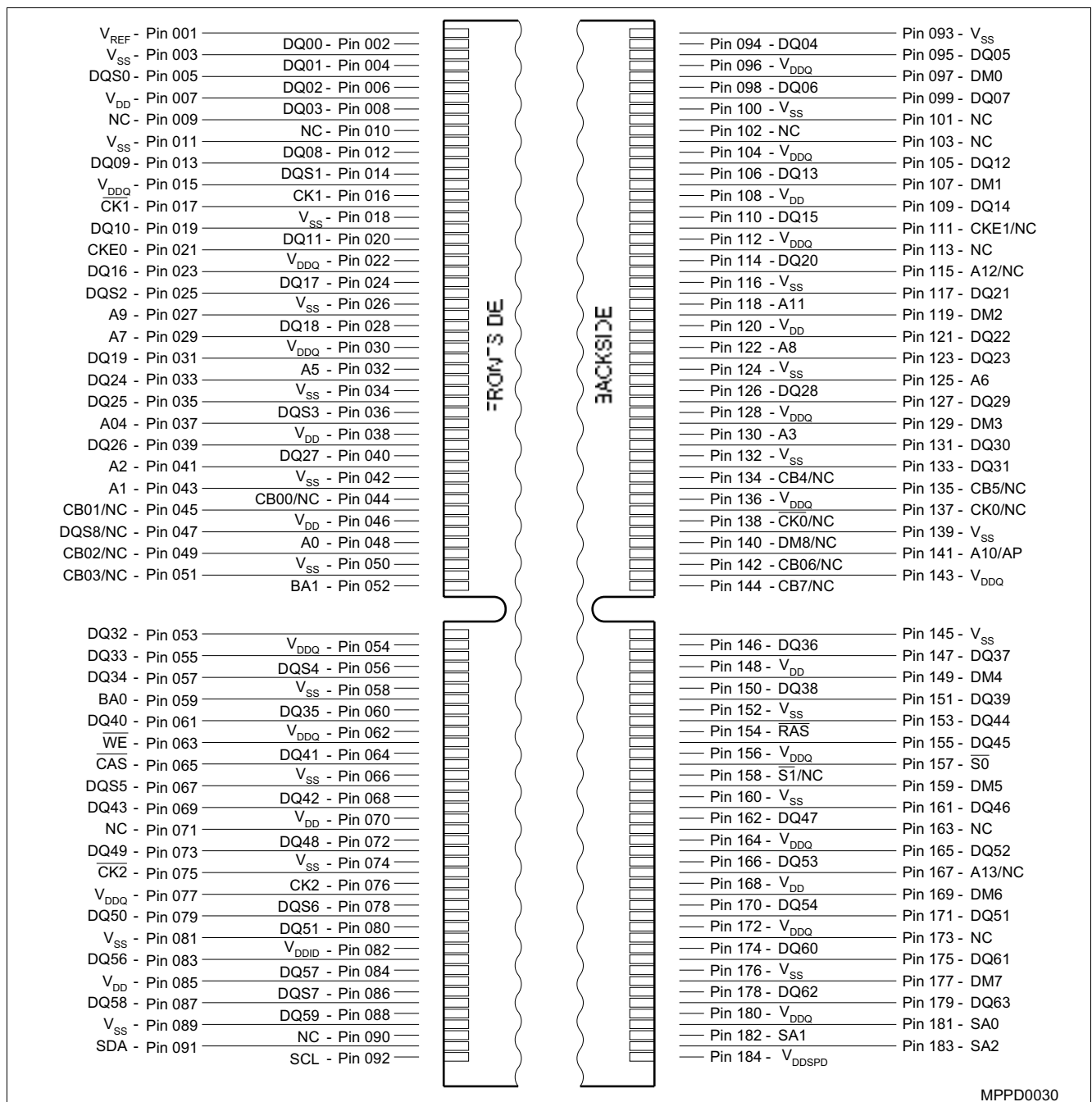


Table 5 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 6 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.



MPPD0030

Figure 1 Pin Configuration 184-Pin, UDIMM





**Table 7 Address Format**

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128MB	16M ×64	1	16M ×16	4	13/2/9	8K	64 ms	7.8 μs
256MB	32M ×64	1	32M ×8	8	13/2/10	8K	64 ms	7.8 μs
256MB	32M ×72	1	32M ×8	9	13/2/10	8K	64 ms	7.8 μs
512MB	64M ×64	2	32M ×8	16	13/2/10	8K	64 ms	7.8 μs
512MB	64M ×72	2	32M ×8	18	13/2/10	8K	64 ms	7.8 μs



### 3 Electrical Characteristics

#### 3.1 Operating Conditions

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Voltage on I/O pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	—	$V_{DDQ} + 0.5$	V	—
Voltage on inputs relative to $V_{SS}$	$V_{IN}$	-1	—	+3.6	V	—
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-1	—	+3.6	V	—
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-1	—	+3.6	V	—
Operating temperature (ambient)	$T_A$	0	—	+70	°C	—
Storage temperature (plastic)	$T_{STG}$	-55	—	+150	°C	—
Power dissipation (per SDRAM component)	$P_D$	—	1	—	W	—
Short circuit output current	$I_{OUT}$	—	50	—	mA	—

**Attention: Permanent damage to the device may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.**

Table 9 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/ Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
Device Supply Voltage	$V_{DD}$	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz
Device Supply Voltage	$V_{DD}$	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz <sup>2)</sup>
Output Supply Voltage	$V_{DDQ}$	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz <sup>3)</sup>
Output Supply Voltage	$V_{DDQ}$	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz <sup>2)3)</sup>
EEPROM supply voltage	$V_{DDSPD}$	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	$V_{SS}, V_{SSQ}$	0	—	0	V	—
Input Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	$f_{CK} \leq 166$ MHz <sup>4)</sup>
Input Reference Voltage	$V_{REF}$	$V_{DDQ} / 2 - 50$ mV	$V_{DDQ} / 2$	$V_{DDQ} / 2 + 50$ mV	V	$f_{CK} > 166$ MHz <sup>2)4)</sup>
I/O Termination Voltage (System)	$V_{TT}$	$V_{REF} - 0.04$	—	$V_{REF} + 0.04$	V	<sup>5)</sup>
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$	—	$V_{DDQ} + 0.3$	V	<sup>8)</sup>
Input Low (Logic0) Voltage	$V_{IL(DC)}$	-0.3	—	$V_{REF} - 0.15$	V	<sup>8)</sup>
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	-0.3	—	$V_{DDQ} + 0.3$	V	<sup>8)</sup>
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36	—	$V_{DDQ} + 0.6$	V	<sup>8)6)</sup>



**Table 9 Electrical Characteristics and DC Operating Conditions (cont'd)**

Parameter	Symbol	Values			Unit	Note/ Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
VI-Matching Pull-up Current to Pull-down Current	$V_{I_{Ratio}}$	0.71	—	1.4	—	<sup>7)</sup>
Input Leakage Current	$I_1$	-2	—	2	$\mu\text{A}$	Any input $0\text{ V} \leq V_{IN} \leq V_{DD}$ ; All other pins not under test = $0\text{ V}$ <sup>8)9)</sup>
Output Leakage Current	$I_{OZ}$	-5	—	5	$\mu\text{A}$	DQs are disabled; $0\text{ V} \leq V_{OUT} \leq V_{DDQ}$ <sup>8)</sup>
Output High Current, Normal Strength Driver	$I_{OH}$	—	—	-16.2	mA	$V_{OUT} = 1.95\text{ V}$ <sup>8)</sup>
Output Low Current, Normal Strength Driver	$I_{OL}$	16.2	—	—	mA	$V_{OUT} = 0.35\text{ V}$ <sup>8)</sup>

- 1)  $0\text{ }^\circ\text{C} \leq T_A \leq 70\text{ }^\circ\text{C}$
- 2) DDR400 conditions apply for all clock frequencies above 166 MHz
- 3) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- 4) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\%$   $V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise variations in  $V_{DDQ}$ .
- 5)  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in the DC level of  $V_{REF}$ .
- 6)  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
- 7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 8) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 9) Values are shown per DDR SDRAM component



### 3.2 Current Conditions and Specification

**Table 10**  $I_{DD}$  Conditions

Parameter	Symbol
<b>Operating Current 0</b> one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	$I_{DD0}$
<b>Operating Current 1</b> one bank; active/read/precharge; Burst Length = 4; see component data sheet.	$I_{DD1}$
<b>Precharge Power-Down Standby Current</b> all banks idle; power-down mode; $CKE \leq V_{IL,MAX}$	$I_{DD2P}$
<b>Precharge Floating Standby Current</b> $\overline{CS} \geq V_{IH,MIN}$ ; all banks idle; $CKE \geq V_{IH,MIN}$ ; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD2F}$
<b>Precharge Quiet Standby Current</b> $\overline{CS} \geq V_{IH,MIN}$ ; all banks idle; $CKE \geq V_{IH,MIN}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM; address and other control inputs stable at $\geq V_{IH,MIN}$ or $\leq V_{IL,MAX}$ .	$I_{DD2Q}$
<b>Active Power-Down Standby Current</b> one bank active; power-down mode; $CKE \leq V_{IL,MAX}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD3P}$
<b>Active Standby Current</b> one bank active; $\overline{CS} \geq V_{IH,MIN}$ ; $CKE \geq V_{IH,MIN}$ ; $t_{RC} = t_{RAS,MAX}$ ; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	$I_{DD3N}$
<b>Operating Current Read</b> one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50 % of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT} = 0$ mA	$I_{DD4R}$
<b>Operating Current Write</b> one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50 % of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	$I_{DD4W}$
<b>Auto-Refresh Current</b> $t_{RC} = t_{RFCMIN}$ ; burst refresh	$I_{DD5}$
<b>Self-Refresh Current</b> $CKE \leq 0.2$ V; external clock on	$I_{DD6}$
<b>Operating Current 7</b> four bank interleaving with Burst Length = 4; see component data sheet.	$I_{DD7}$



Table 11  $I_{DD}$  Specification for PC3200

Part Number & Organization	HYS64D16301HU-5-C HYS64D16301GU-5-C		HYS64D32300HU-5-C HYS64D32300GU-5-C		HYS72D32300HU-5-C HYS72D32300GU-5-C		HYS64D64320HU-5-C HYS64D64320GU-5-C		HYS72D64320HU-5-C HYS72D64320GU-5-C		Unit	Note <sup>1)2)</sup>
	128MB		256MB		256MB		512MB		512MB			
	×64		×64		×72		×64		×72			
	1 Rank		1 Rank		1 Rank		2 Ranks		2 Ranks			
	-5		-5		-5		-5		-5			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
$I_{DD0}$	300	360	560	720	630	810	864	1080	972	1215	mA	<sup>3)</sup>
$I_{DD1}$	380	440	640	800	720	900	944	1160	1062	1305	mA	<sup>3)4)</sup>
$I_{DD2P}$	16	20	32	40	36	45	64	80	72	90	mA	<sup>5)</sup>
$I_{DD2F}$	120	144	240	288	270	324	480	576	540	648	mA	<sup>5)</sup>
$I_{DD2Q}$	80	112	160	224	180	252	320	448	360	504	mA	<sup>5)</sup>
$I_{DD3P}$	52	72	104	144	117	162	208	288	234	324	mA	<sup>5)</sup>
$I_{DD3N}$	172	216	304	360	342	405	608	720	684	810	mA	<sup>5)</sup>
$I_{DD4R}$	400	480	680	800	765	900	984	1160	1107	1305	mA	<sup>3)4)</sup>
$I_{DD4W}$	400	520	720	840	810	945	1024	1200	1152	1350	mA	<sup>3)</sup>
$I_{DD5}$	560	760	1120	1520	1260	1710	1424	1880	1602	2115	mA	<sup>3)</sup>
$I_{DD6}$	6	11	11	22	13	25	22	45	25	50	mA	—
$I_{DD7}$	840	1000	1680	2000	1890	2250	1984	2360	2232	2655	mA	<sup>3)4)</sup>

- 1) Module  $I_{DD}$  values are calculated on the basis of component  $I_{DD}$  and can be measured differently depending on actual to DQ loading capacitance.
- 2) Test condition for maximum values:  $V_{DD} = 2.7 \text{ V}$ ,  $T_A = 10 \text{ °C}$
- 3) The module  $I_{DDx}$  values are calculated from the  $I_{DDx}$  values of the component data sheet as follows:  
 $m \times I_{DDx}[\text{component}] + n \times I_{DD3N}[\text{component}]$  with  $m$  and  $n$  number of components of rank 1 and 2;  $n=0$  for 1 rank modules
- 4) DQ I/O ( $I_{DDQ}$ ) currents are not included in the calculations (see note 1)
- 5) The module  $I_{DDx}$  values are calculated from the component  $I_{DDx}$  data sheet values as:  $(m + n) \times I_{DDx}[\text{component}]$



Table 12  $I_{DD}$  Specification for PC2700

Part Number & Organization	HYS64D16301HU-6-C HYS64D16301GU-6-C		HYS64D32300HU-6-C HYS64D32300GU-6-C		HYS72D32300HU-6-C HYS72D32300GU-6-C		HYS64D64320HU-6-C HYS64D64320GU-6-C		HYS72D64320HU-6-C HYS72D64320GU-6-C		Unit	Note <sup>1)2)</sup>
	128MB		256MB		256MB		512MB		512MB			
	×64		×64		×72		×64		×72			
	1 Rank		1 Rank		1 Rank		2 Ranks		2 Ranks			
	-6		-6		-6		-6		-6			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
$I_{DD0}$	260	300	480	600	540	675	736	904	828	1017	mA	<sup>3)</sup>
$I_{DD1}$	320	380	560	680	630	765	816	984	918	1107	mA	<sup>3)4)</sup>
$I_{DD2P}$	16	20	32	40	36	45	64	80	72	90	mA	<sup>5)</sup>
$I_{DD2F}$	100	340	200	240	225	270	400	480	450	540	mA	<sup>5)</sup>
$I_{DD2Q}$	68	96	136	192	153	216	272	384	306	432	mA	<sup>5)</sup>
$I_{DD3P}$	44	60	88	120	99	135	176	240	198	270	mA	<sup>5)</sup>
$I_{DD3N}$	144	180	256	304	288	342	512	608	576	684	mA	<sup>5)</sup>
$I_{DD4R}$	340	400	560	680	630	765	816	984	918	1107	mA	<sup>3)4)</sup>
$I_{DD4W}$	360	440	600	720	675	810	856	1024	963	1152	mA	<sup>3)</sup>
$I_{DD5}$	480	640	960	1280	1080	1440	1216	1584	1368	1782	mA	<sup>3)</sup>
$I_{DD6}$	6	11	11	22	13	25	44	22	25	25	mA	—
$I_{DD7}$	720	860	1440	1720	1620	1935	1696	2024	1908	2277	mA	<sup>3)4)</sup>

- 1) Module  $I_{DD}$  values are calculated on the basis of component  $I_{DD}$  and can be measured differently according to DQ loading capacity.
- 2) Test condition for maximum values:  $V_{DD} = 2.7 \text{ V}$ ,  $T_A = 10 \text{ °C}$
- 3) The module  $I_{DDx}$  values are calculated from the  $I_{DDx}$  values of the component data sheet as follows:  
 $m \times I_{DDx}[\text{component}] + n \times I_{DD3N}[\text{component}]$  with  $m$  and  $n$  number of components of rank 1 and 2;  $n=0$  for 1 rank modules
- 4) DQ I/O ( $I_{DDQ}$ ) currents are not included in the calculations (see note 1)
- 5) The module  $I_{DDx}$  values are calculated from the component  $I_{DDx}$  data sheet values as:  $(m + n) \times I_{DDx}[\text{component}]$



### 3.3 AC Characteristic

Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	-5		-6		Unit	Note/ Test Condition <sup>1)</sup>
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/CK	$t_{AC}$	-0.5	+0.5	-0.7	+0.7	ns	2)3)4)5)
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
Clock cycle time	$t_{CK}$	5	8	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
Auto precharge write recovery + precharge time	$t_{DAL}$	$(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$				$t_{CK}$	2)3)4)5)6)
DQ and DM input hold time	$t_{DH}$	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	$t_{DIPW}$	1.75	—	1.75	—	ns	2)3)4)5)
DQS output access time from CK/CK	$t_{DQSCK}$	-0.6	+0.6	-0.6	+0.6	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	$t_{CK}$	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	$t_{DQSQ}$	—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
Write command to 1 <sup>st</sup> DQS latching transition	$t_{DQSS}$	0.72	1.25	0.75	1.25	$t_{CK}$	2)3)4)5)
DQ and DM input setup time	$t_{DS}$	0.4	—	0.45	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
Clock Half Period	$t_{HP}$	min. ( $t_{CL}$ , $t_{CH}$ )	—	min. ( $t_{CL}$ , $t_{CH}$ )	—	ns	2)3)4)5)
Data-out high-impedance time from CK/CK	$t_{HZ}$	—	+0.7	-0.7	+0.7	ns	2)3)4)5)7)
Address and control input hold time	$t_{IH}$	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Control and Addr. input pulse width (each input)	$t_{IPW}$	2.2	—	2.2	—	ns	2)3)4)5)9)



Table 13 AC Timing - Absolute Specifications for PC3200 and PC2700 (cont'd)

Parameter	Symbol	-5		-6		Unit	Note/ Test Condition <sup>1)</sup>
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Address and control input setup time	$t_{IS}$	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)8)
Data-out low-impedance time from CK/ $\overline{CK}$	$t_{LZ}$	-0.7	+0.7	-0.7	+0.7	ns	2)3)4)5)7)
Mode register set command cycle time	$t_{MRD}$	2	—	2	—	$t_{CK}$	2)3)4)5)
DQ/DQS output hold time	$t_{QH}$	$t_{HP} - t_{QH}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
Data hold skew factor	$t_{QHS}$	—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
Active to Autoprecharge delay	$t_{RAP}$	$t_{RCD}$	—	$t_{RCD}$	—	ns	2)3)4)5)
Active to Precharge command	$t_{RAS}$	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	$t_{RC}$	55	—	60	—	ns	2)3)4)5)
Active to Read or Write delay	$t_{RCD}$	15	—	18	—	ns	2)3)4)5)
Average Periodic Refresh Interval	$t_{REFI}$	—	7.8	—	7.8	$\mu s$	2)3)4)5)10)
Auto-refresh to Active/Auto-refresh command period	$t_{RFC}$	65	—	72	—	ns	2)3)4)5)
Precharge command period	$t_{RP}$	15	—	18	—	ns	2)3)4)5)
Read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	2)3)4)5)
Read postamble	$t_{RPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)
Active bank A to Active bank B command	$t_{RRD}$	10	—	12	—	ns	2)3)4)5)
Write preamble	$t_{WPRE}$	0.25	—	0.25	—	$t_{CK}$	2)3)4)5)
Write preamble setup time	$t_{WPRES}$	0	—	0	—	ns	2)3)4)5)11)
Write postamble	$t_{WPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)12)
Write recovery time	$t_{WR}$	15	—	15	—	ns	2)3)4)5)
Internal write to read command delay	$t_{WTR}$	2	—	1	—	$t_{CK}$	2)3)4)5)
Exit self-refresh to non-read command	$t_{XSNR}$	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	2)3)4)5)

- 1)  $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{DD} = +2.5\text{ V} \pm 0.2\text{ V}$  (DDR333);  $V_{DDQ} = 2.6\text{ V} \pm 0.1\text{ V}$ ,  $V_{DD} = +2.6\text{ V} \pm 0.1\text{ V}$  (DDR400)
- 2) Input slew rate  $\geq 1\text{ V/ns}$  for DDR400, DDR333
- 3) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross: the input reference level for signals other than CK/ $\overline{CK}$ , is  $V_{REF}$ . CK/ $\overline{CK}$  slew rate are  $\geq 1.0\text{ V/ns}$ .
- 4) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is  $V_{TT}$ .





## Electrical Characteristics

- 6) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  is equal to the actual system clock cycle time.
- 7)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) Fast slew rate  $\geq 1.0$  V/ns, slow slew rate  $\geq 0.5$  V/ns and  $< 1$  V/ns for command/address and CK & CK slew rate  $> 1.0$  V/ns, measured between  $V_{IH(ac)}$  and  $V_{IL(ac)}$ .
- 9) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
- 11) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on  $t_{DQSS}$ .
- 12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.



## 4 SPD Contents

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

### List of SPD Code Tables

- Table 14 “SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-5-C” on Page 18
- Table 15 “SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-6-C” on Page 22
- Table 16 “SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-5-C” on Page 25
- Table 17 “SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-6-C” on Page 28

Table 14 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-5-C

Product Type		HYS64D16301GU-5-C	HYS64D32300GU-5-C	HYS72D32300GU-5-C	HYS64D64320GU-5-C	HYS72D64320GU-5-C
Organization		128MB	256MB	256MB	512MB	512MB
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U-30330	PC3200U-30330	PC3200U-30330	PC3200U-30330	PC3200U-30330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E <sup>2</sup> PROM	80	80	80	80	80
1	Total number of Bytes in E <sup>2</sup> PROM	08	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D	0D
4	Number of Column Addresses	09	0A	0A	0A	0A
5	Number of DIMM Ranks	01	01	01	02	02
6	Data Width (LSB)	40	40	48	40	48
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	$t_{CK} @ CL_{max}$ (Byte 18) [ns]	50	50	50	50	50
10	$t_{AC}$ SDRAM @ $CL_{max}$ (Byte 18) [ns]	50	50	50	50	50
11	Error Correction Support	00	00	02	00	02
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08



Table 14 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-5-C

Product Type		HYS64D16301GU-5-C	HYS64D32300GU-5-C	HYS72D32300GU-5-C	HYS64D64320GU-5-C	HYS72D64320GU-5-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
15	$t_{CCD}$ [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	CAS Latency	1C	1C	1C	1C	1C
19	CS Latency	01	01	01	01	01
20	Write Latency	02	02	02	02	02
21	DIMM Attributes	20	20	20	20	20
22	Component Attributes	C1	C1	C1	C1	C1
23	$t_{CK} @ CL_{max} -0.5$ (Byte 18) [ns]	60	60	60	60	60
24	$t_{AC}$ SDRAM @ $CL_{max} -0.5$ [ns]	50	50	50	50	50
25	$t_{CK} @ CL_{max} -1$ (Byte 18) [ns]	75	75	75	75	75
26	$t_{AC}$ SDRAM @ $CL_{max} -1$ [ns]	50	50	50	50	50
27	$t_{RPmin}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRDmin}$ [ns]	28	28	28	28	28
29	$t_{RCDmin}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RASmin}$ [ns]	28	28	28	28	28
31	Module Density per Rank	20	40	40	40	40
32	$t_{AS}, t_{CS}$ [ns]	60	60	60	60	60
33	$t_{AH}, t_{CH}$ [ns]	60	60	60	60	60
34	$t_{DS}$ [ns]	40	40	40	40	40
35	$t_{DH}$ [ns]	40	40	40	40	40
36 - 40	Not used	00	00	00	00	00
41	$t_{RCmin}$ [ns]	37	37	37	37	37
42	$t_{RFCmin}$ [ns]	41	41	41	41	41
43	$t_{CKmax}$ [ns]	28	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28	28
45	$t_{QHSmax}$ [ns]	50	50	50	50	50
46	Not used	00	00	00	00	00



Table 14 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-5-C

Product Type		HYS64D16301GU-5-C	HYS64D32300GU-5-C	HYS72D32300GU-5-C	HYS64D64320GU-5-C	HYS72D64320GU-5-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
47	DIMM PCB Height	00	00	00	00	00
48 - 61	Not used	00	00	00	00	00
62	SPD Revision	00	00	00	00	00
63	Checksum of Byte 0-62	E4	FD	0F	FE	10
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Part Number, Char 1	36	36	37	36	37
74	Part Number, Char 2	34	34	32	34	32
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	31	33	33	36	36
77	Part Number, Char 5	36	32	32	34	34
78	Part Number, Char 6	33	33	33	33	33
79	Part Number, Char 7	30	30	30	32	32
80	Part Number, Char 8	31	30	30	30	30
81	Part Number, Char 9	47	47	47	47	47
82	Part Number, Char 10	55	55	55	55	55
83	Part Number, Char 11	35	35	35	35	35
84	Part Number, Char 12	43	43	43	43	43
85	Part Number, Char 13	20	20	20	20	20
86	Part Number, Char 14	20	20	20	20	20
87	Part Number, Char 15	20	20	20	20	20



Table 14 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-5-C

Product Type		HYS64D16301GU-5-C	HYS64D32300GU-5-C	HYS72D32300GU-5-C	HYS64D64320GU-5-C	HYS72D64320GU-5-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00



Table 15 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-6-C

Product Type		HYS64D16301GU-6-C	HYS64D32300GU-6-C	HYS72D32300GU-6-C	HYS64D64320GU-6-C	HYS72D64320GU-6-C
Organization		128MB	256MB	256MB	512MB	512MB
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U-25330	PC2700U-25330	PC2700U-25330	PC2700U-25330	PC2700U-25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E <sup>2</sup> PROM	80	80	80	80	80
1	Total number of Bytes in E <sup>2</sup> PROM	08	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D	0D
4	Number of Column Addresses	09	0A	0A	0A	0A
5	Number of DIMM Ranks	01	01	01	02	02
6	Data Width (LSB)	40	40	48	40	48
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	$t_{CK} @ CL_{max}$ (Byte 18) [ns]	60	60	60	60	60
10	$t_{AC}$ SDRAM @ $CL_{max}$ (Byte 18) [ns]	70	70	70	70	70
11	Error Correction Support	00	00	02	00	02
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	$t_{CCD}$ [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	CAS Latency	0C	0C	0C	0C	0C
19	CS Latency	01	01	01	01	01
20	Write Latency	02	02	02	02	02
21	DIMM Attributes	20	20	20	20	20
22	Component Attributes	C1	C1	C1	C1	C1
23	$t_{CK} @ CL_{max} -0.5$ (Byte 18) [ns]	75	75	75	75	75
24	$t_{AC}$ SDRAM @ $CL_{max} -0.5$ [ns]	70	70	70	70	70
25	$t_{CK} @ CL_{max} -1$ (Byte 18) [ns]	00	00	00	00	00
26	$t_{AC}$ SDRAM @ $CL_{max} -1$ [ns]	00	00	00	00	00
27	$t_{RPmin}$ [ns]	48	48	48	48	48



Table 15 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-6-C

Product Type		HYS64D16301GU-6-C	HYS64D32300GU-6-C	HYS72D32300GU-6-C	HYS64D64320GU-6-C	HYS72D64320GU-6-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
28	$t_{RRDmin}$ [ns]	30	30	30	30	30
29	$t_{RCDmin}$ [ns]	48	48	48	48	48
30	$t_{RASmin}$ [ns]	2A	2A	2A	2A	2A
31	Module Density per Rank	20	40	40	40	40
32	$t_{AS}, t_{CS}$ [ns]	75	75	75	75	75
33	$t_{AH}, t_{CH}$ [ns]	75	75	75	75	75
34	$t_{DS}$ [ns]	45	45	45	45	45
35	$t_{DH}$ [ns]	45	45	45	45	45
36 - 40	Not used	00	00	00	00	00
41	$t_{RCmin}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFCmin}$ [ns]	48	48	48	48	48
43	$t_{CKmax}$ [ns]	30	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D	2D
45	$t_{QHSmax}$ [ns]	55	55	55	55	55
46	Not used	00	00	00	00	00
47	DIMM PCB Height	00	00	00	00	00
48 - 61	Not used	00	00	00	00	00
62	SPD Revision	00	00	00	00	00
63	Checksum of Byte 0-62	E8	01	13	02	14
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx



Table 15 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]GU-6-C

Product Type		HYS64D16301GU-6-C	HYS64D32300GU-6-C	HYS72D32300GU-6-C	HYS64D64320GU-6-C	HYS72D64320GU-6-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
73	Part Number, Char 1	36	36	37	36	37
74	Part Number, Char 2	34	34	32	34	32
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	31	33	33	36	36
77	Part Number, Char 5	36	32	32	34	34
78	Part Number, Char 6	33	33	33	33	33
79	Part Number, Char 7	30	30	30	32	32
80	Part Number, Char 8	31	30	30	30	30
81	Part Number, Char 9	47	47	47	47	47
82	Part Number, Char 10	55	55	55	55	55
83	Part Number, Char 11	36	36	36	36	36
84	Part Number, Char 12	43	43	43	43	43
85	Part Number, Char 13	20	20	20	20	20
86	Part Number, Char 14	20	20	20	20	20
87	Part Number, Char 15	20	20	20	20	20
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00





Table 16 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-5-C

Product Type		HYS64D16301HU-5-C	HYS64D32300HU-5-C	HYS72D32300HU-5-C	HYS64D64320HU-5-C	HYS72D64320HU-5-C
Organization		128MB	256MB	256MB	512MB	512MB
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U-30330	PC3200U-30330	PC3200U-30330	PC3200U-30330	PC3200U-30330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E <sup>2</sup> PROM	80	80	80	80	80
1	Total number of Bytes in E <sup>2</sup> PROM	08	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D	0D
4	Number of Column Addresses	09	0A	0A	0A	0A
5	Number of DIMM Ranks	01	01	01	02	02
6	Data Width (LSB)	40	40	48	40	48
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	$t_{CK} @ CL_{max}$ (Byte 18) [ns]	50	50	50	50	50
10	$t_{AC}$ SDRAM @ $CL_{max}$ (Byte 18) [ns]	50	50	50	50	50
11	Error Correction Support	00	00	02	00	02
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	$t_{CCD}$ [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	CAS Latency	1C	1C	1C	1C	1C
19	CS Latency	01	01	01	01	01
20	Write Latency	02	02	02	02	02
21	DIMM Attributes	20	20	20	20	20
22	Component Attributes	C1	C1	C1	C1	C1
23	$t_{CK} @ CL_{max} -0.5$ (Byte 18) [ns]	60	60	60	60	60
24	$t_{AC}$ SDRAM @ $CL_{max} -0.5$ [ns]	50	50	50	50	50
25	$t_{CK} @ CL_{max} -1$ (Byte 18) [ns]	75	75	75	75	75
26	$t_{AC}$ SDRAM @ $CL_{max} -1$ [ns]	50	50	50	50	50
27	$t_{RPmin}$ [ns]	3C	3C	3C	3C	3C



Table 16 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-5-C

Product Type		HYS64D16301HU-5-C	HYS64D32300HU-5-C	HYS72D32300HU-5-C	HYS64D64320HU-5-C	HYS72D64320HU-5-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
<b>Label Code</b>		<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>	<b>PC3200U-30330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
28	$t_{RRDmin}$ [ns]	28	28	28	28	28
29	$t_{RCDmin}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RASmin}$ [ns]	28	28	28	28	28
31	Module Density per Rank	20	40	40	40	40
32	$t_{AS}, t_{CS}$ [ns]	60	60	60	60	60
33	$t_{AH}, t_{CH}$ [ns]	60	60	60	60	60
34	$t_{DS}$ [ns]	40	40	40	40	40
35	$t_{DH}$ [ns]	40	40	40	40	40
36 - 40	Not used	00	00	00	00	00
41	$t_{RCmin}$ [ns]	37	37	37	37	37
42	$t_{RFCmin}$ [ns]	41	41	41	41	41
43	$t_{CKmax}$ [ns]	28	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28	28
45	$t_{QHSmax}$ [ns]	50	50	50	50	50
46	Not used	00	00	00	00	00
47	DIMM PCB Height	00	00	00	00	00
48 - 61	Not used	00	00	00	00	00
62	SPD Revision	00	00	00	00	00
63	Checksum of Byte 0-62	E4	FD	0F	FE	10
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx



Table 16 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-5-C

Product Type		HYS64D16301HU-5-C	HYS64D32300HU-5-C	HYS72D32300HU-5-C	HYS64D64320HU-5-C	HYS72D64320HU-5-C
<b>Organization</b>		128MB	256MB	256MB	512MB	512MB
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
<b>Label Code</b>		PC3200U-30330	PC3200U-30330	PC3200U-30330	PC3200U-30330	PC3200U-30330
<b>JEDEC SPD Revision</b>		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
73	Part Number, Char 1	36	36	37	36	37
74	Part Number, Char 2	34	34	32	34	32
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	31	33	33	36	36
77	Part Number, Char 5	36	32	32	34	34
78	Part Number, Char 6	33	33	33	33	33
79	Part Number, Char 7	30	30	30	32	32
80	Part Number, Char 8	31	30	30	30	30
81	Part Number, Char 9	48	48	48	48	48
82	Part Number, Char 10	55	55	55	55	55
83	Part Number, Char 11	35	35	35	35	35
84	Part Number, Char 12	43	43	43	43	43
85	Part Number, Char 13	20	20	20	20	20
86	Part Number, Char 14	20	20	20	20	20
87	Part Number, Char 15	20	20	20	20	20
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00



Table 17 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-6-C

Product Type		HYS64D16301HU-6-C	HYS64D32300HU-6-C	HYS72D32300HU-6-C	HYS64D64320HU-6-C	HYS72D64320HU-6-C
Organization		128MB	256MB	256MB	512MB	512MB
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U-25330	PC2700U-25330	PC2700U-25330	PC2700U-25330	PC2700U-25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E <sup>2</sup> PROM	80	80	80	80	80
1	Total number of Bytes in E <sup>2</sup> PROM	08	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D	0D
4	Number of Column Addresses	09	0A	0A	0A	0A
5	Number of DIMM Ranks	01	01	01	02	02
6	Data Width (LSB)	40	40	48	40	48
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	$t_{CK} @ CL_{max}$ (Byte 18) [ns]	60	60	60	60	60
10	$t_{AC}$ SDRAM @ $CL_{max}$ (Byte 18) [ns]	70	70	70	70	70
11	Error Correction Support	00	00	02	00	02
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	$t_{CCD}$ [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	CAS Latency	0C	0C	0C	0C	0C
19	CS Latency	01	01	01	01	01
20	Write Latency	02	02	02	02	02
21	DIMM Attributes	20	20	20	20	20
22	Component Attributes	C1	C1	C1	C1	C1
23	$t_{CK} @ CL_{max} -0.5$ (Byte 18) [ns]	75	75	75	75	75
24	$t_{AC}$ SDRAM @ $CL_{max} -0.5$ [ns]	70	70	70	70	70
25	$t_{CK} @ CL_{max} -1$ (Byte 18) [ns]	00	00	00	00	00
26	$t_{AC}$ SDRAM @ $CL_{max} -1$ [ns]	00	00	00	00	00
27	$t_{RPmin}$ [ns]	48	48	48	48	48



Table 17 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-6-C

Product Type		HYS64D16301HU-6-C	HYS64D32300HU-6-C	HYS72D32300HU-6-C	HYS64D64320HU-6-C	HYS72D64320HU-6-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
28	$t_{RRDmin}$ [ns]	30	30	30	30	30
29	$t_{RCDmin}$ [ns]	48	48	48	48	48
30	$t_{RASmin}$ [ns]	2A	2A	2A	2A	2A
31	Module Density per Rank	20	40	40	40	40
32	$t_{AS}, t_{CS}$ [ns]	75	75	75	75	75
33	$t_{AH}, t_{CH}$ [ns]	75	75	75	75	75
34	$t_{DS}$ [ns]	45	45	45	45	45
35	$t_{DH}$ [ns]	45	45	45	45	45
36 - 40	Not used	00	00	00	00	00
41	$t_{RCmin}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFCmin}$ [ns]	48	48	48	48	48
43	$t_{CKmax}$ [ns]	30	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D	2D
45	$t_{QHSmax}$ [ns]	55	55	55	55	55
46	Not used	00	00	00	00	00
47	DIMM PCB Height	00	00	00	00	00
48 - 61	Not used	00	00	00	00	00
62	SPD Revision	00	00	00	00	00
63	Checksum of Byte 0-62	E8	01	13	02	14
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx



Table 17 SPD Codes for HYS[64/72]D[16/32/64][300/301/320]HU-6-C

Product Type		HYS64D16301HU-6-C	HYS64D32300HU-6-C	HYS72D32300HU-6-C	HYS64D64320HU-6-C	HYS72D64320HU-6-C
<b>Organization</b>		<b>128MB</b>	<b>256MB</b>	<b>256MB</b>	<b>512MB</b>	<b>512MB</b>
		×64	×64	×72	×64	×72
		<b>1 Rank (×16)</b>	<b>1 Rank (×8)</b>	<b>1 Rank (×8)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>	<b>PC2700U-25330</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>	<b>Rev. 0.0</b>
Byte#	Description	HEX	HEX	HEX	HEX	HEX
73	Part Number, Char 1	36	36	37	36	37
74	Part Number, Char 2	34	34	32	34	32
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	31	33	33	36	36
77	Part Number, Char 5	36	32	32	34	34
78	Part Number, Char 6	33	33	33	33	33
79	Part Number, Char 7	30	30	30	32	32
80	Part Number, Char 8	31	30	30	30	30
81	Part Number, Char 9	48	48	48	48	48
82	Part Number, Char 10	55	55	55	55	55
83	Part Number, Char 11	36	36	36	36	36
84	Part Number, Char 12	43	43	43	43	43
85	Part Number, Char 13	20	20	20	20	20
86	Part Number, Char 14	20	20	20	20	20
87	Part Number, Char 15	20	20	20	20	20
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00



## 5 Package Outlines

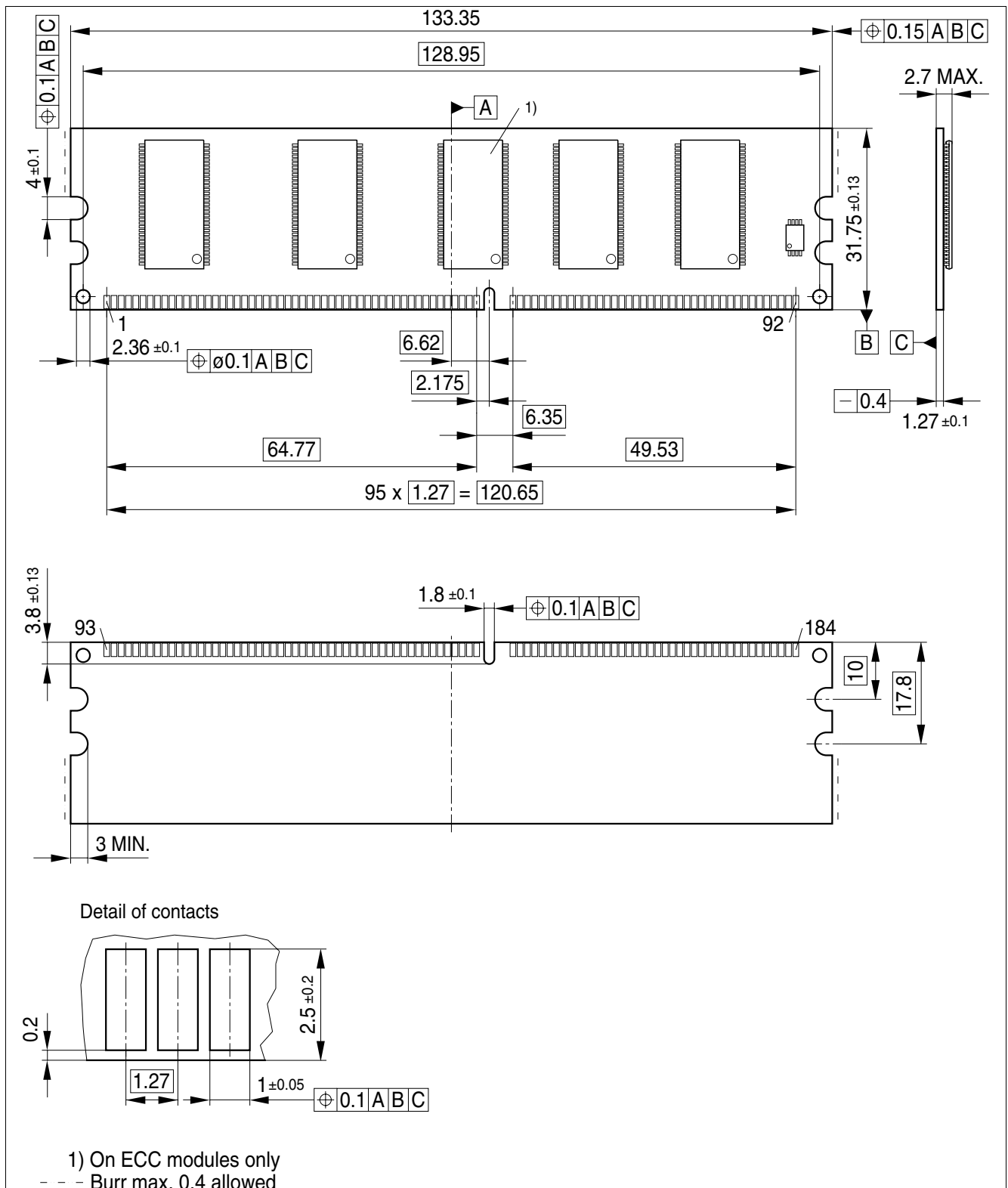


Figure 2 Package Outlines - Raw Card C 128 MByte, 1 Rank Module

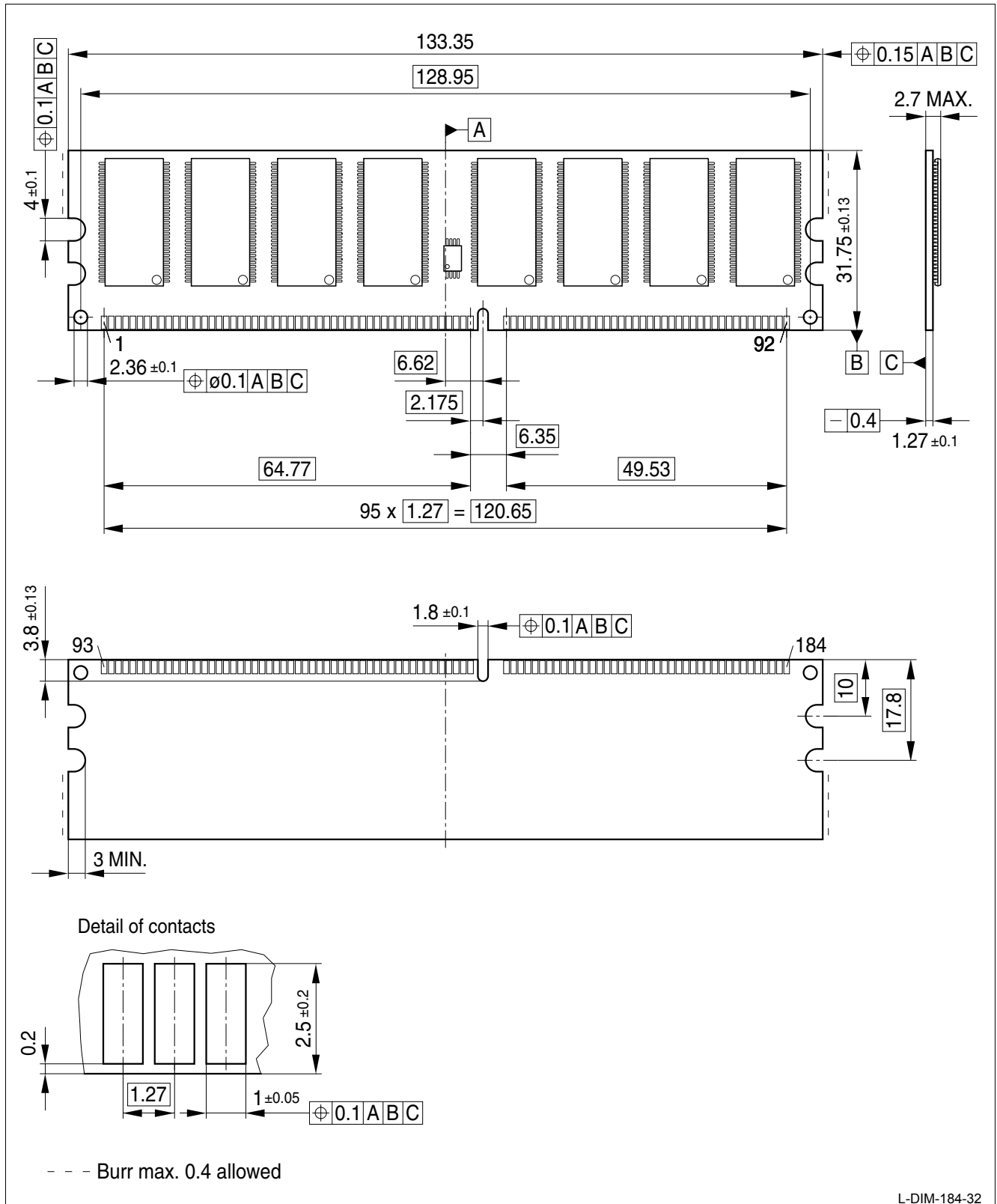


Figure 3 Package Outline - Raw Card A 256 MByte, 1 Rank Module

L-DIM-184-32



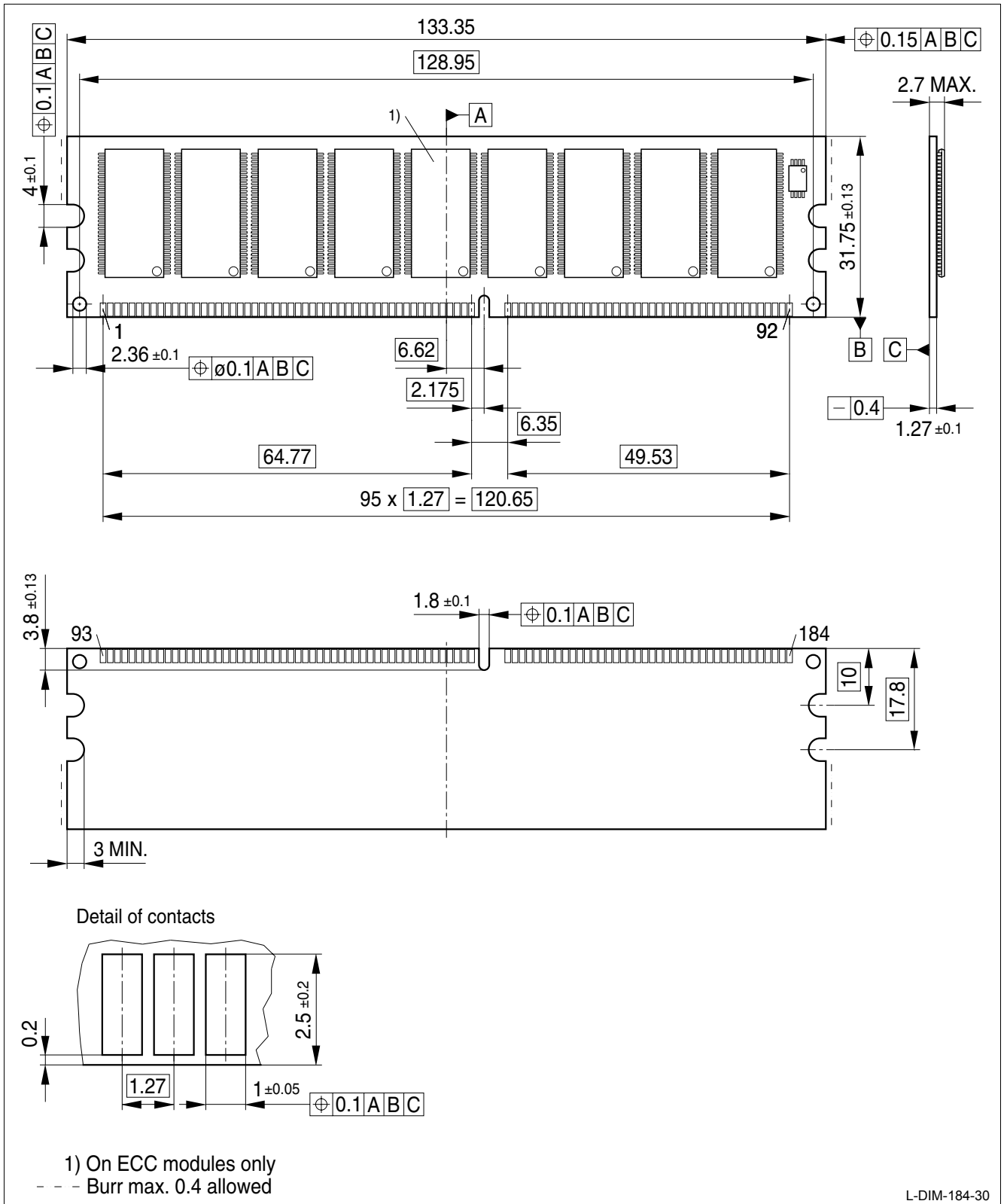


Figure 4 Package Outline - Raw Card A 256 MByte, 1 Rank ECC Module

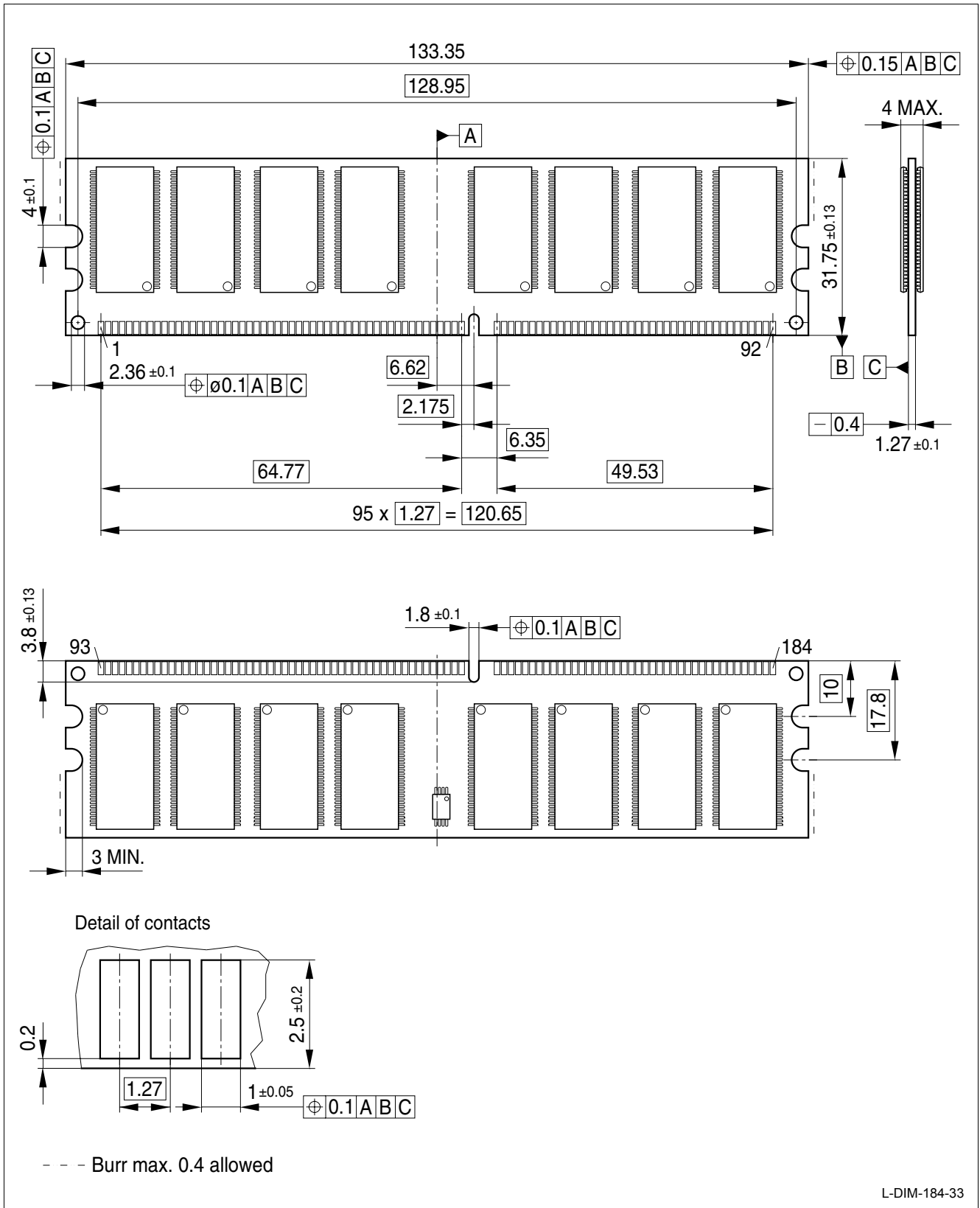


Figure 5 Package Outline - Raw Card B 512 MByte, 2 Ranks Module

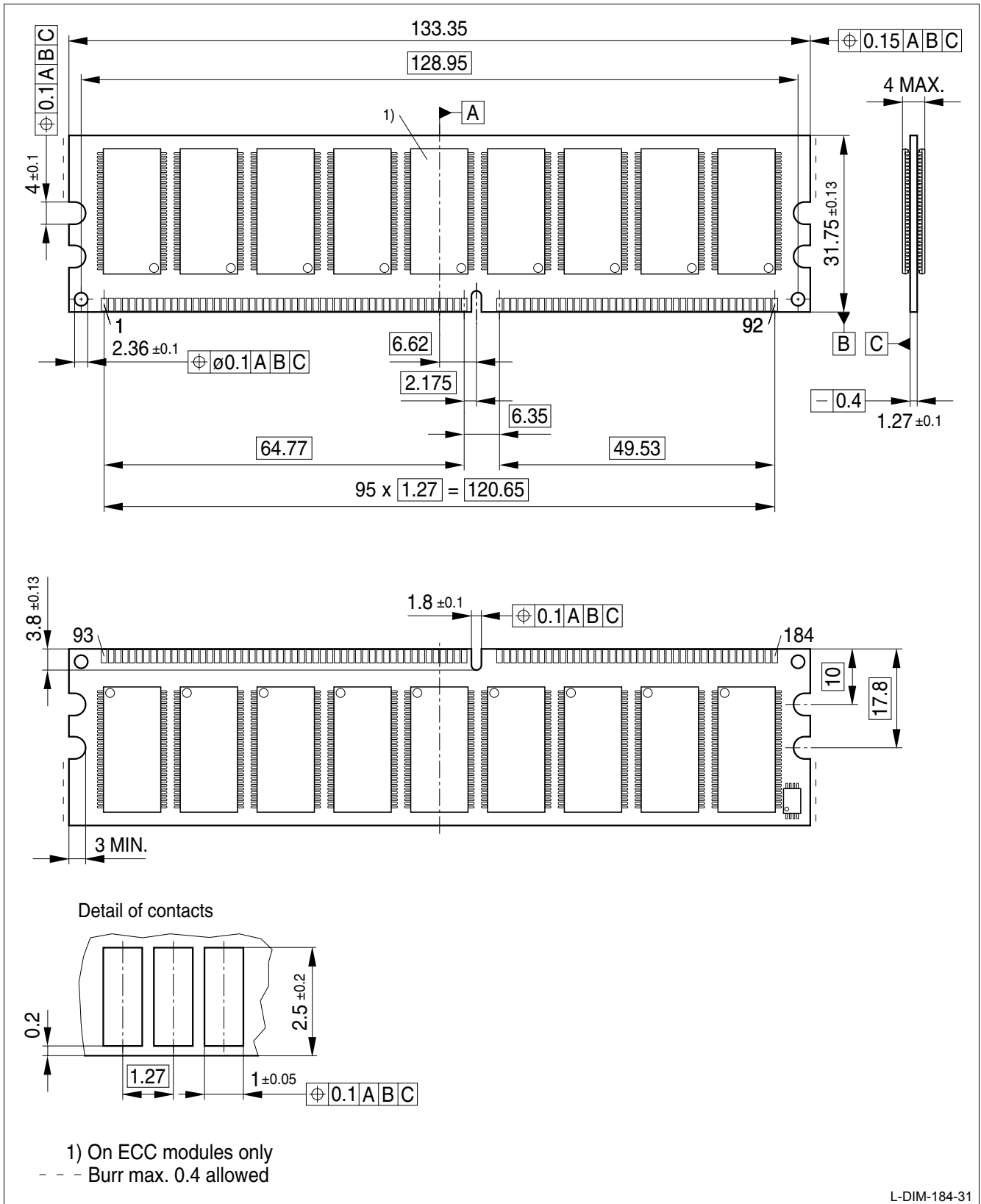


Figure 6 Package Outline - Raw Card B 512 MByte, 2 Ranks ECC Module



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