

128K x 8 LOW POWER CMOS STATIC RAM

JULY 1996

FEATURES

- High-speed access time: 35, 45, 55, 70 ns
- Low active power: 450 mW (typical)
- Low standby power: 150 μ W (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and $\overline{CE2}$) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V ($\pm 10\%$) power supply

DESCRIPTION

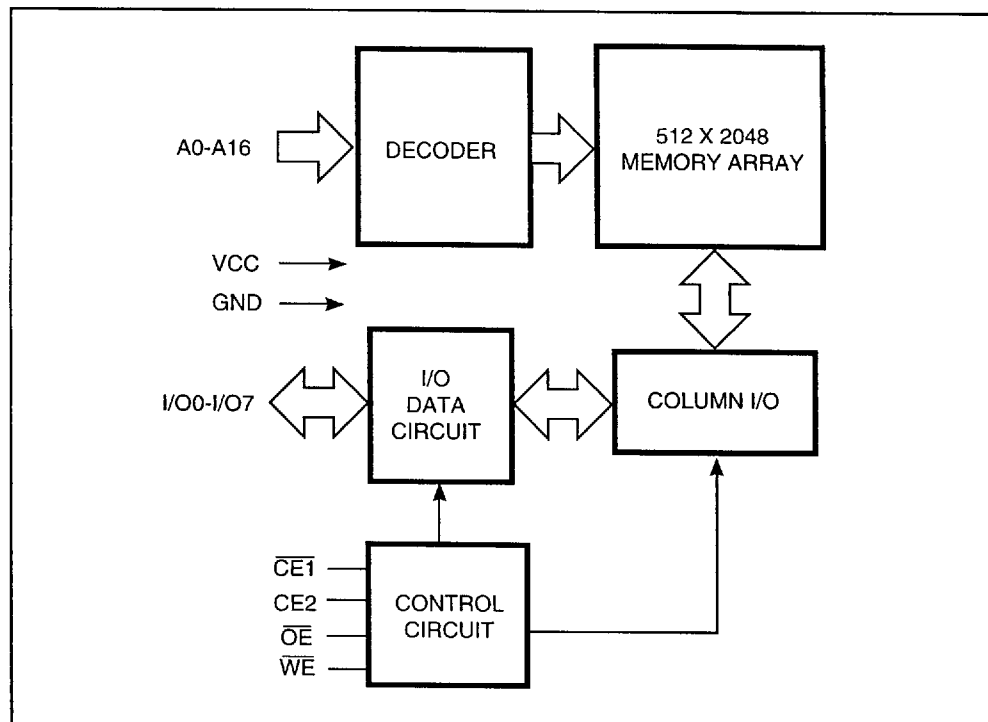
The ISSI IS62C1024L is a low power, 131,072-word by 8-bit CMOS static RAM. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or $\overline{CE2}$ is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and $\overline{CE2}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62C1024L is available in 32-pin 600-mil plastic DIP, 525-mil plastic SOP and TSOP (type 1) packages.

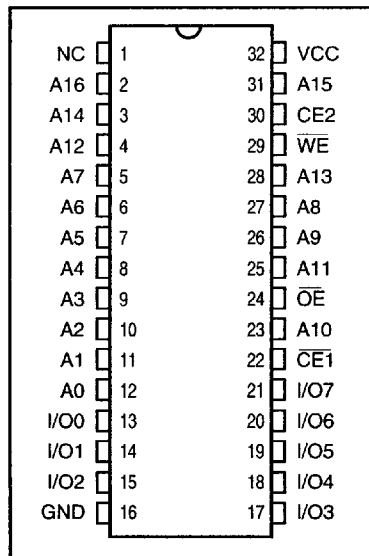
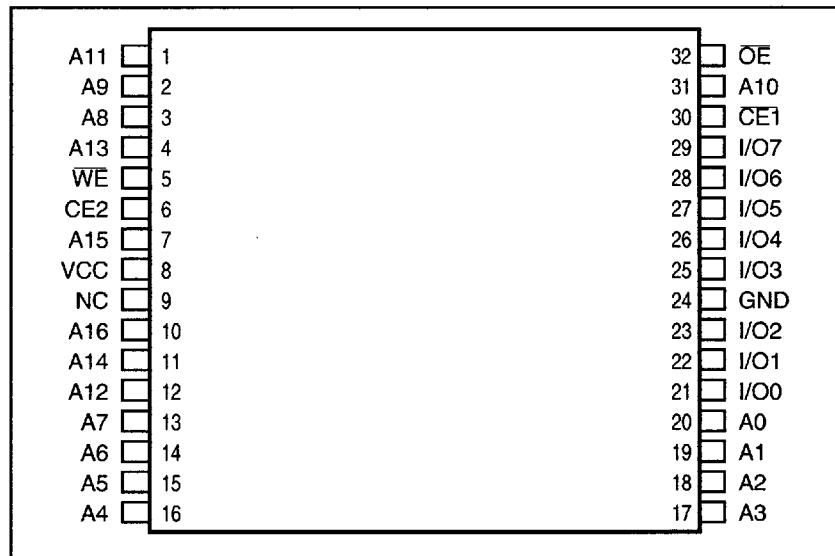
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION
32-Pin SOP and DIP

PIN CONFIGURATION
32-Pin TSOP (Type 1)

PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	Isb1, Isb2
(Power-down)	X	X	L	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	H	High-Z	Icc
Read	H	L	H	L	DOUT	Icc
Write	L	L	H	X	DIN	Icc

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-45 to +85	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.5	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	Com. Ind.	-2 10	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC}	Com. Ind.	-2 10	μA

Notes:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-35 ns		-45 ns		-55 ns		-70 ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX}	Com. Ind.	— 100 110	— 90 100	— 80 90	— 70 80	— 10 10	— 10 15	— 10 15	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE1} \geq V_{IH}$, or CE2 ≤ V _{IL} , f = 0	Com. Ind.	— 10 15	— 10 15	— 10 15	— 10 15	— 10 15	— 10 15	— 10 15	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE1} \leq V_{CC} - 0.2V$, CE2 ≤ 0.2V, V _{IN} > V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com. Ind.	— 500 750	— 500 750	— 500 750	— 500 750	— 500 750	— 500 750	— 500 750	μA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-35		-45		-55		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	35	—	45	—	55	—	70	ns
t_{ACE2}	$\overline{CE2}$ Access Time	—	35	—	45	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	10	—	20	—	25	—	35	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	10	0	15	0	20	0	25	ns
$t_{LZCE1}^{(2)}$	$\overline{CE1}$ to Low-Z Output	3	—	5	—	7	—	10	—	ns
$t_{LZCE2}^{(2)}$	$\overline{CE2}$ to Low-Z Output	3	—	5	—	7	—	10	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE1}$ or $\overline{CE2}$ to High-Z Output	0	10	0	15	0	20	0	25	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

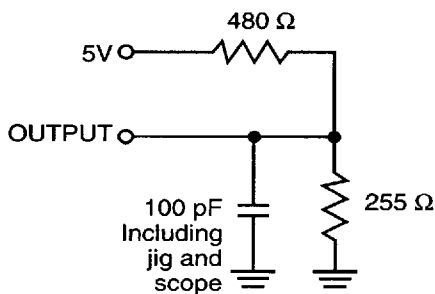


Figure 1a.

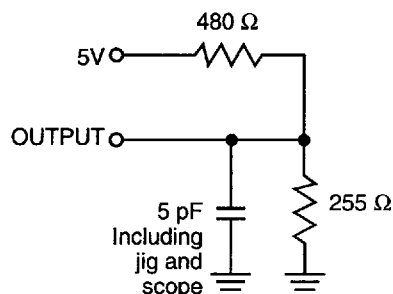
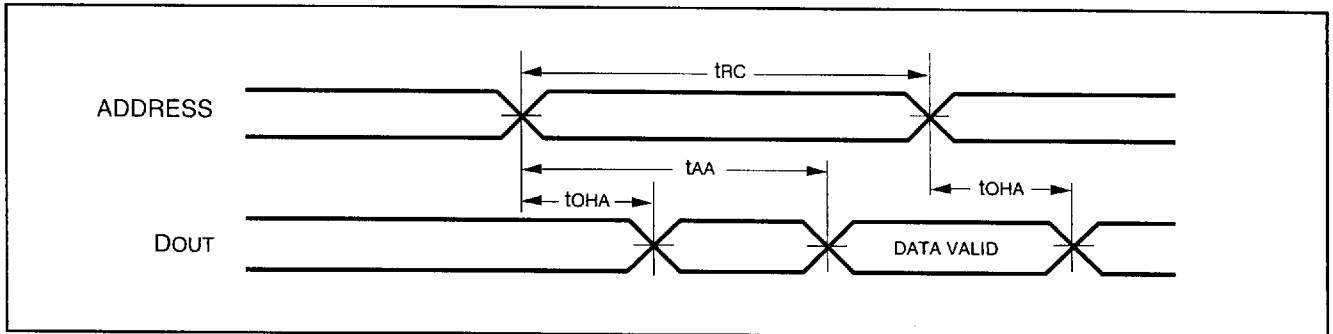
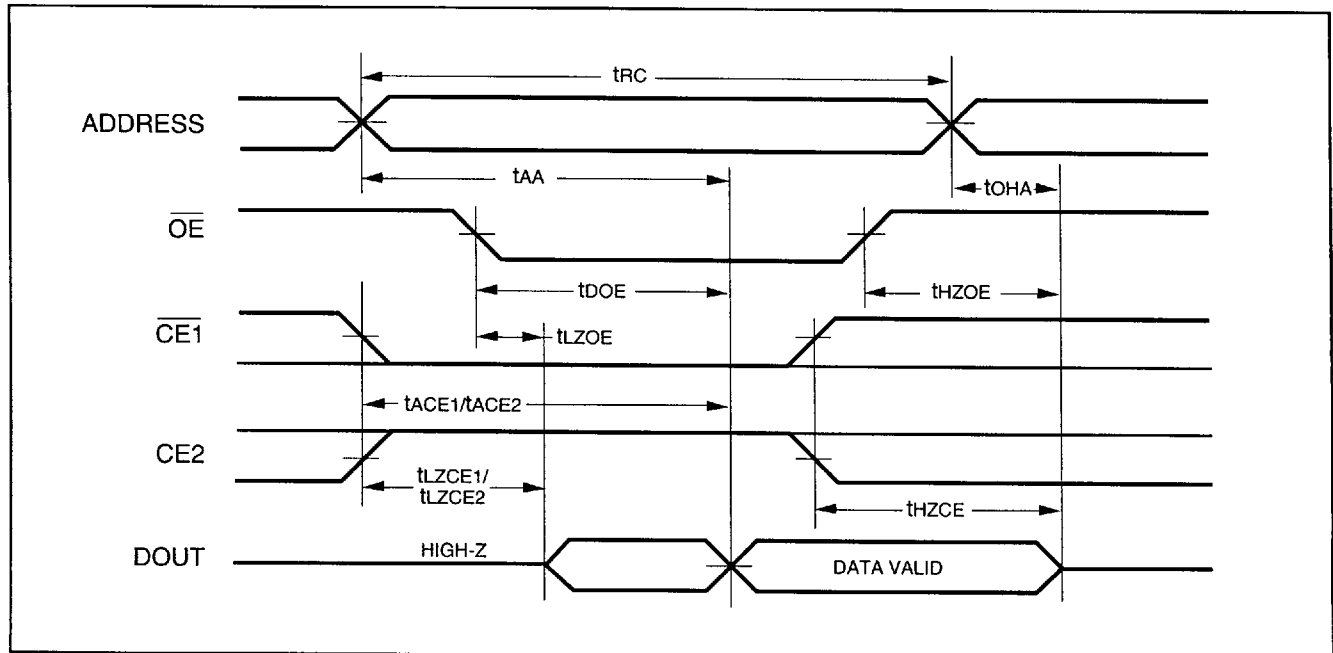


Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)READ CYCLE NO. 2^(1,3)**Notes:**

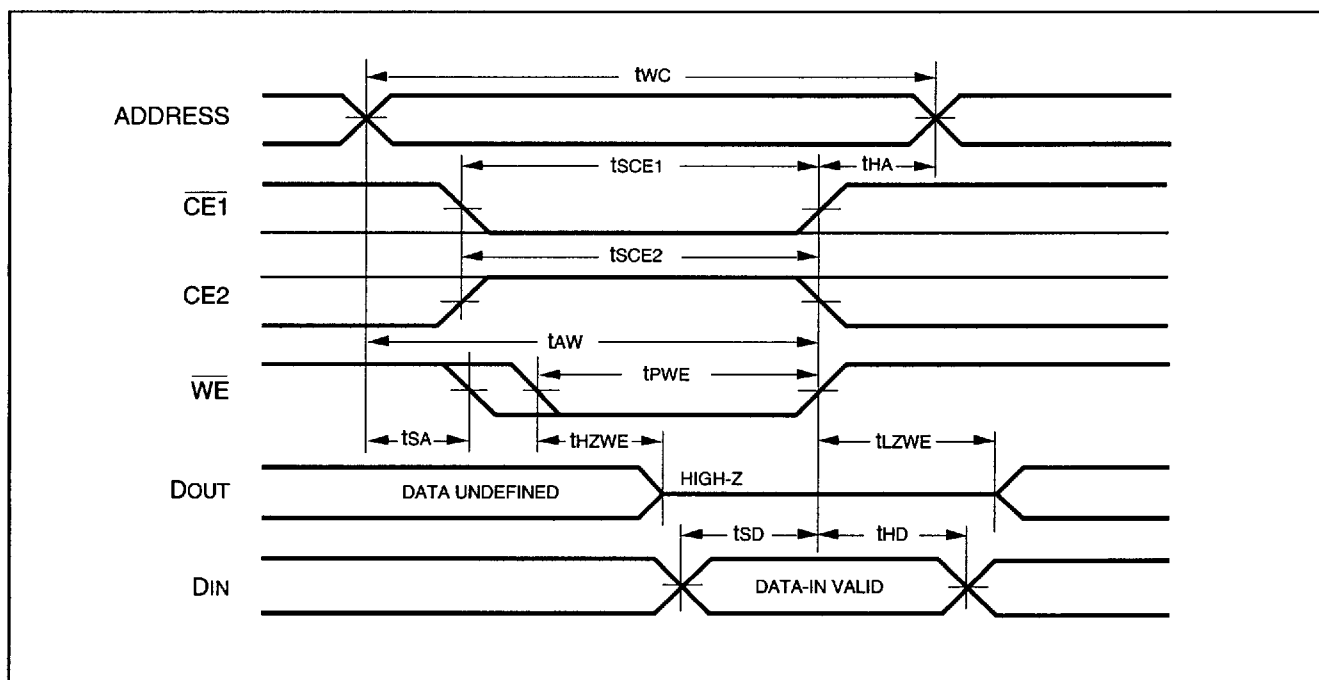
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and $CE2$ HIGH transitions.

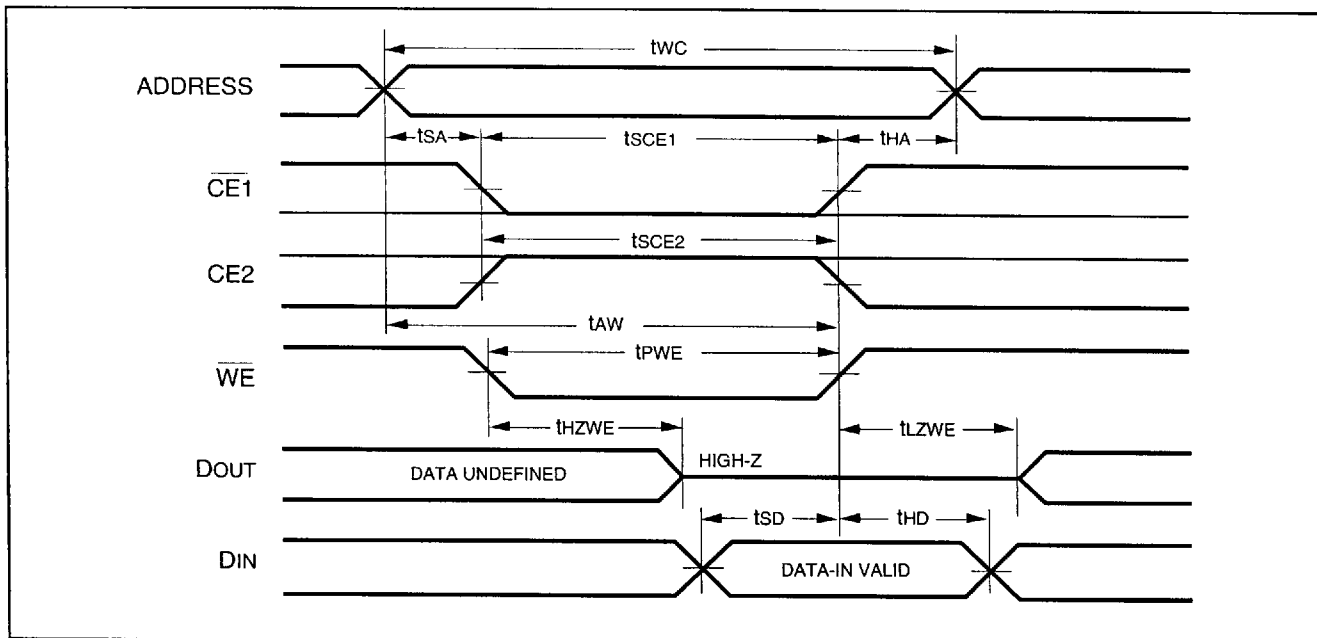
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range, Standard and Low Power)

Symbol	Parameter	-35		-45		-55		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	35	—	45	—	55	—	70	—	ns
t _{SCE1}	$\overline{CE1}$ to Write End	25	—	35	—	50	—	60	—	ns
t _{SCE2}	CE2 to Write End	25	—	35	—	50	—	60	—	ns
t _{AW}	Address Setup Time to Write End	25	—	35	—	45	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWE⁽⁴⁾}	$\overline{WE}$ Pulse Width	25	—	35	—	40	—	50	—	ns
t _{SD}	Data Setup to Write End	20	—	25	—	25	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE⁽²⁾}	$\overline{WE}$ LOW to High-Z Output	—	10	—	15	—	20	—	25	ns
t _{LZWE⁽²⁾}	$\overline{WE}$ HIGH to Low-Z Output	3	—	5	—	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE1 LOW, CE2 HIGH and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with OE HIGH.

AC WAVEFORMS**WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)^(1,2)**

WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)^(1,2)**Notes:**

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

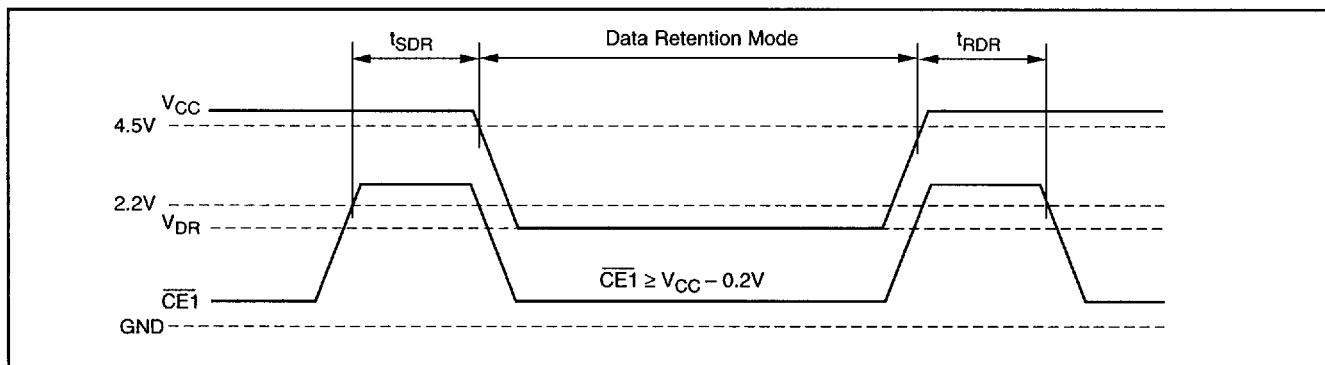
Speed (ns)	Order Part No.	Package
35	IS62C1024L-35W	600-mil Plastic DIP
35	IS62C1024L-35Q	525-mil Plastic SOP
35	IS62C1024L-35T	TSOP, Type 1
45	IS62C1024L-45W	600-mil Plastic DIP
45	IS62C1024L-45Q	525-mil Plastic SOP
45	IS62C1024L-45T	TSOP, Type 1
55	IS62C1024L-55W	600-mil Plastic DIP
55	IS62C1024L-55Q	525-mil Plastic SOP
55	IS62C1024L-55T	TSOP, Type 1
70	IS62C1024L-70W	600-mil Plastic DIP
70	IS62C1024L-70Q	525-mil Plastic SOP
70	IS62C1024L-70T	TSOP, Type 1

ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

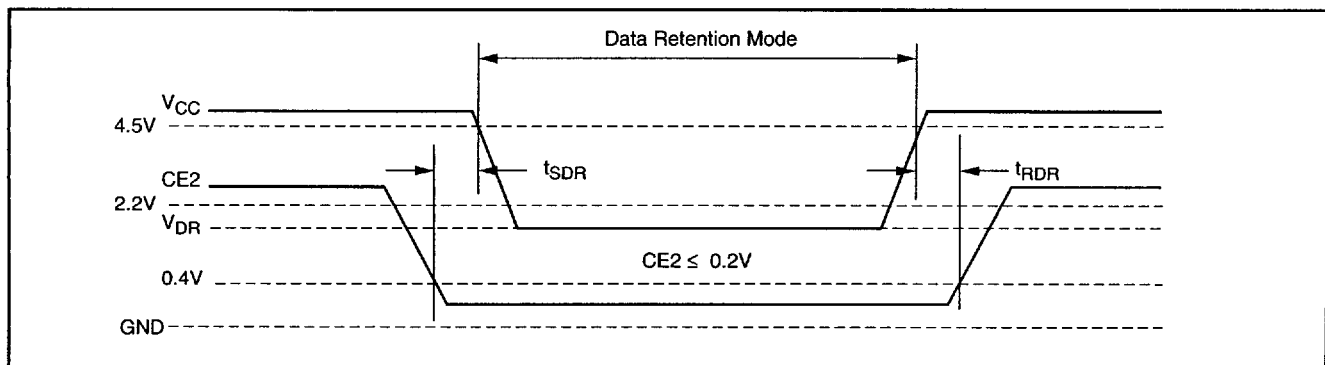
Speed (ns)	Order Part No.	Package
35	IS62C1024L-35WI	600-mil Plastic DIP
35	IS62C1024L-35QI	525-mil Plastic SOP
35	IS62C1024L-35TI	TSOP, Type 1
45	IS62C1024L-45WI	600-mil Plastic DIP
45	IS62C1024L-45QI	525-mil Plastic SOP
45	IS62C1024L-45TI	TSOP, Type 1
55	IS62C1024L-55WI	600-mil Plastic DIP
55	IS62C1024L-55QI	525-mil Plastic SOP
55	IS62C1024L-55TI	TSOP, Type 1
70	IS62C1024L-70WI	600-mil Plastic DIP
70	IS62C1024L-70QI	525-mil Plastic SOP
70	IS62C1024L-70TI	TSOP, Type 1

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	See Data Retention Waveform	2.0	5.5	V
I_{DR}	Data Retention Current	$V_{CC} = 3.0V, \overline{CE1} \geq V_{CC} - 0.2V$	Com. Ind.	250 400	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

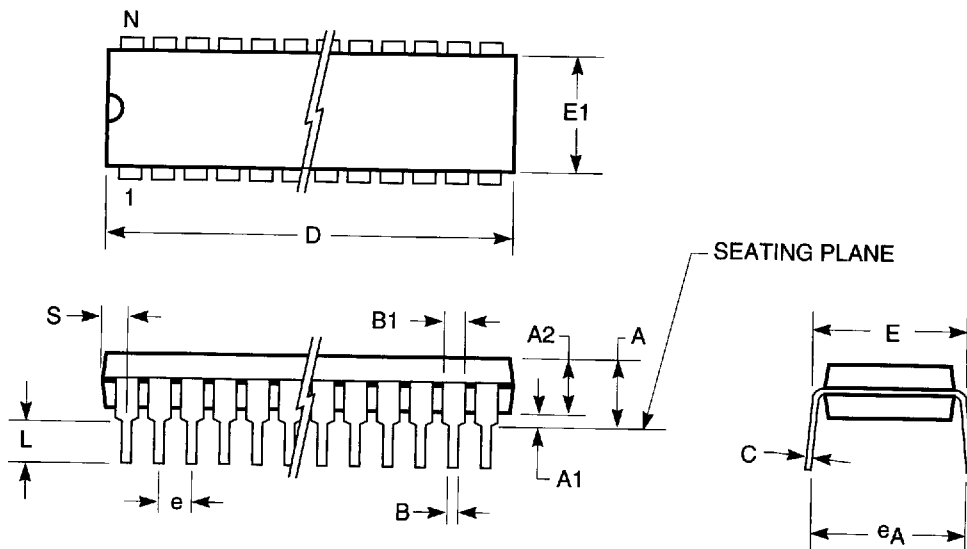
DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)

DATA RETENTION WAVEFORM (CE2 Controlled)



400-mil Plastic DIP

Package Code: M



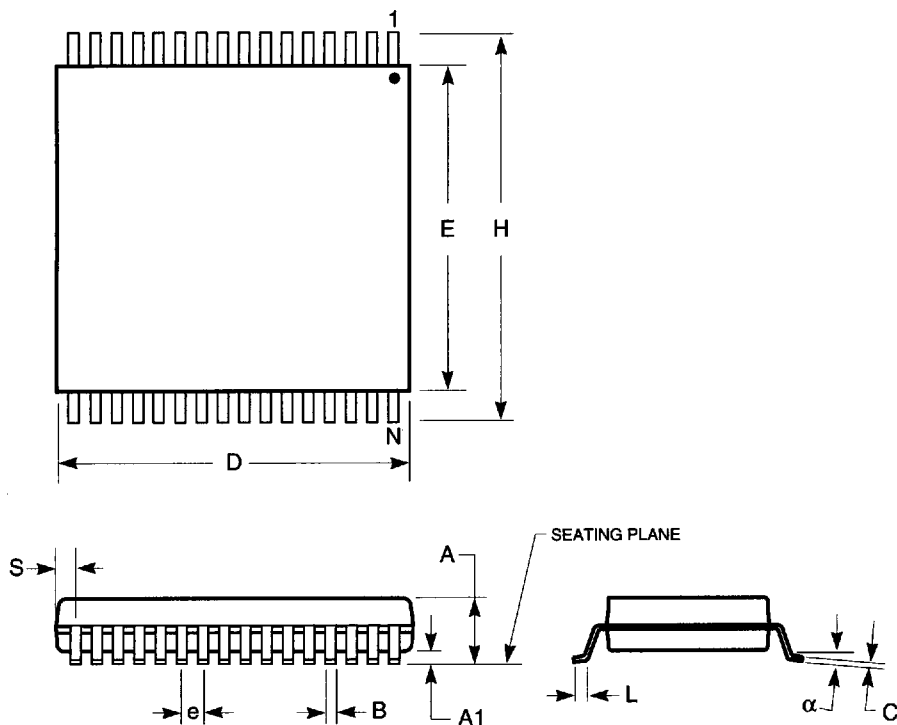
400-mil Plastic DIP (M)				
Inches				
Symbol	Min	Max	Min	Max
Ref. Std.				
N	28		32	
A	—	0.210	—	0.200
A1	0.015	—	0.015	—
A2	0.145	0.155	0.145	0.155
B	0.016	0.022	0.016	0.022
B1	0.058	0.064	0.058	0.064
C	0.008	0.015	0.008	0.015
D	—	1.520	—	1.620
E	0.400	0.420	0.400	0.420
E1	0.275	0.295	0.380	0.390
eA	0.430	0.470	0.430	0.470
e	0.100	BSC	0.100	BSC
L	0.115	0.160	0.120	0.140
S	—	0.070	—	0.065

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP - 32 pins

Package Code: T



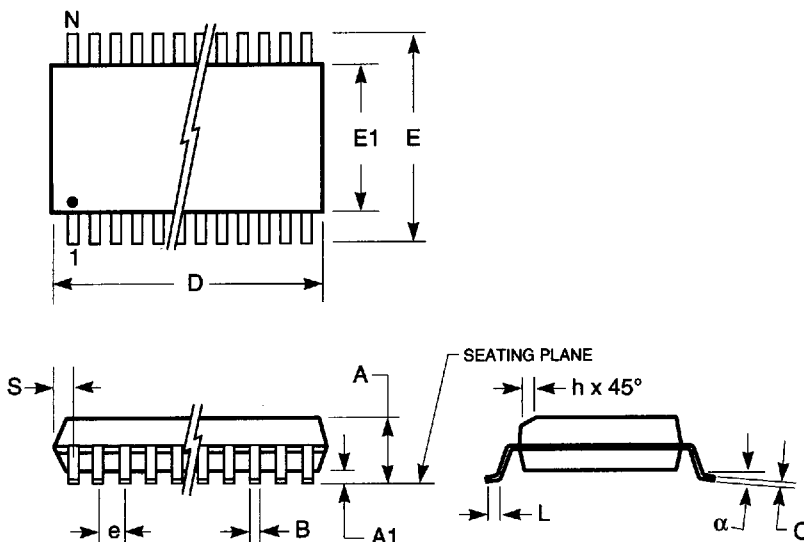
Plastic TSOP (T)			
Inches			
Symbol	Min	Max	
Ref. Std.			
N	32		
A	—	0.047	
A1	0.002	0.010	
B	0.007	0.009	
C	0.006	0.014	
D	0.311	0.319	
E	0.720	0.728	
H	0.780	0.795	
e	0.020	BSC	
L	0.016	0.025	
α	0°	8°	

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

450-mil Plastic SOP

Package Code: U



450-mil Plastic SOP (U)		
Inches		
Symbol	Min	Max
Ref. Std.		
No. Leads	28	
A	—	0.112
A1	0.004	0.014
B	0.014	0.020
C	0.010	—
D	0.708	0.718
E	0.453	0.477
E1	0.326	0.336
e	0.050 BSC	
h	0.012	0.020
L	0.028	0.045
α	0°	8°
S	0.023	0.047

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.