Data Sheet | April 14, 2008 | FN6684.0

Integrated TFT LCD Supply and Logic Driver

The ISL97648 represents a high power, integrated LCD supply IC which is targeted at Notebook, Monitor and TV LCD displays. The ISL97648 integrates a level shift with charge sharing function, boost converter for A_{VDD} generation of high power with HVS and temperature sensor, 4 high power V_{COM} amplifiers, and I^2C LCD VCOM digital calibrator.

The ISL97648 integrates a high-performance boost converter with 2.7A FET for generating A_{VDD} supply up to 18V.

The ISL97648 has a high voltage TFT-LCD logic driver with +40V and -25V output swing capability. It is capable of delivering 100mA output peak current into 5nF of capacitive load. To simplify external circuitry, the ISL97648 integrates additional logic circuits.

The integrated HVS circuit is used to provide high voltage stress testing of the LCD panel for production purpose.

An on-board temperature sensor is also provided for system thermal management control.

The 4 integrated amplifiers feature high slew-rate and high output current capability. They are permanently enabled when A_{VDD} is present.

The VCOM voltage of an LCD panel needs to be adjusted to remove flicker. This part provides a digital interface to control the sink-current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external VCOM buffer amplifier. The desired VCOM setting is loaded from an external source via a standard 2 wire I^2C serial interface. At power-up the part automatically comes up at last programmed setting in an on-board 7-bit EEPROM.

The ISL97648 is packaged in a 56 Ld, 8mmx8mm TQFN package and is specified for operation over the -40°C to +85°C temperature range.

Features

- 2.6V to 5.5V input supply
- Integrated 2.7A Boost Converter
- 1.4MHz Switching Frequency
- Level Shifter
  - Up to 332kHz Input Logic Frequency
  - +40V to -25V Output Swing Capability
  - 100mA Output Peak Current
  - TTL-Compatible Logic Input
- Four High Speed V_{COM} Amplifiers
- ±5°C Accuracy Thermal Sensor Over the -40°C to +150°C Temperature Range.
- I^2C Calibrator
  - 128-Step Adjustable Sink Current Output
  - Output Adjustment SET Pin
- 56 Ld 8mmx8mm TQFN Package
- Pb-Free (RoHS Compliant)

Applications

- LCD-Notebook, Monitor and TV
- Industrial/medical LCD Displays

Ordering Information

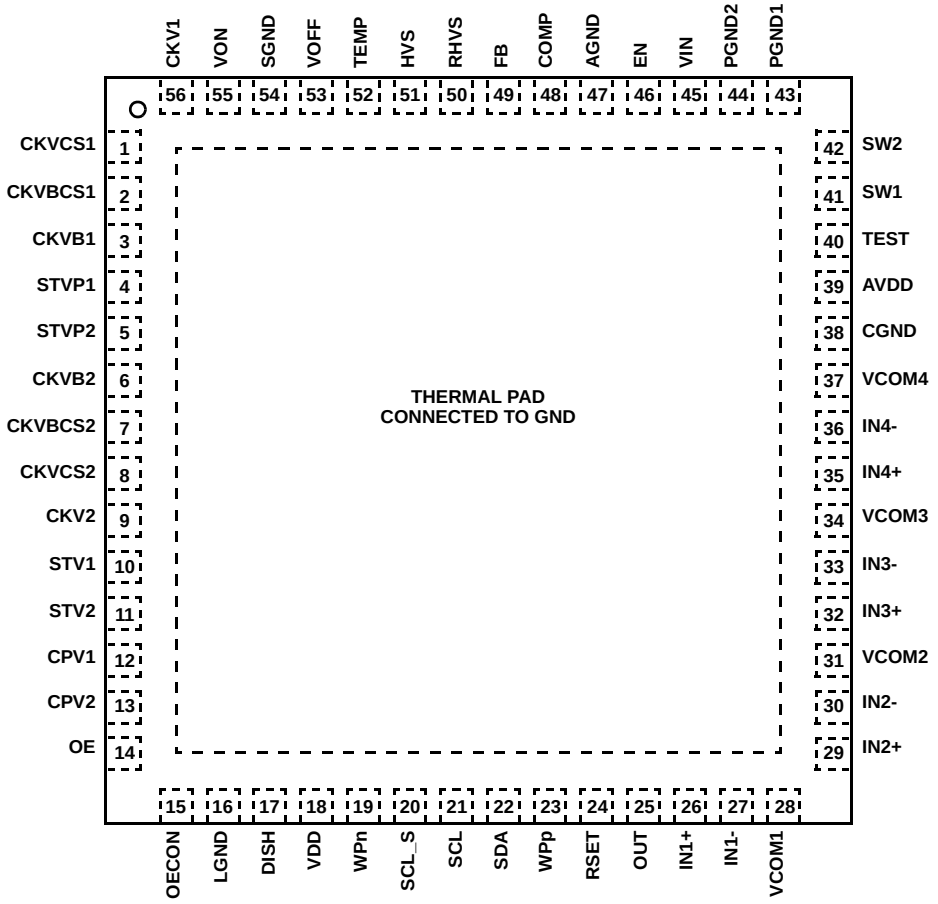
PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97648IRTZ	97648IRTZ	56 Ld 8x8 TQFN	L56.8x8D
ISL97648IRTZ-T*	97648IRTZ	56 Ld 8x8 TQFN	L56.8x8D
ISL97648IRTZ-TK*	97648IRTZ	56 Ld 8x8 TQFN	L56.8x8D

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL97648
(56 LD TQFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

All Other Pins except the following . . . . . -0.3V to +6.5V
VIN to PGND, AGND, and LGND . . . . . -0.3V to 6.5V
VDD to PGND, AGND, and LGND. 6.5V
SW to PGND, AGND, and LGND . . . . . -0.3V to 22V
EN, FB, COMP, TEMP, HVS, RHVS to PGND, AGND, and LGND . . . . . -0.3V to 6.5V
IN1+, IN1-, and VCOM1 to PGND, AGND, and LGND . -0.3V to 20V
IN2+, IN2-, and VCOM2 to PGND, AGND, and LGND . -0.3V to 20V
IN3+, IN3-, and VCOM3 to PGND, AGND, and LGND . -0.3V to 20V
IN4+, IN4-, and VCOM4 to PGND, AGND, and LGND . -0.3V to 20V
AVDD to PGND, AGND, and LGND . . . . . -0.3V to 22V
DISH to PGND, AGND, and LGND . . . . . -3.6V to 5.5V
OECON to PGND, AGND, and LGND. . . . . -0.3V to 5.5V
V_{ON} to PGND, AGND, and LGND. 44V
$V_{OFF}$to PGND, AGND, and LGND . . . . . -28V
V_{CKV1}, V_{CKV2}, V_{CKVB1}, V_{CKVB2}, V_{CKVCS1}, V_{CKVCS2}, $V_{CKVBCS1}$, $V_{CKVBCS2}$, STVP1,STVP2 to PGND, AGND, and LGND . . . . . -28V to 44V
SDA, SCL, SCLS-S, W_{pn}, W_{pp} to PGND, AGND, and LGND . . . . . -0.3V to 4V
OUT to PGND, AGND, and LGND. 20V
Voltage between PGND, AGND, and LGND . . . . . +-0.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TQFN Package (Notes 1, 2).	48.33	12.07

Functional Junction Temperature ($T_{JUNCTION}$). . . -40°C to +125°C
Storage Temperature ($T_{STORAGE}$) . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Operating Temperature (T_A) . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

VDD = V_{IN} = 3.3V, A_{VDD} = 12V, V_{ON} = 20V, V_{OFF} = -14V, T_A from -40°C to +85°C, Fcpv1 and Fcpv2 = 105kHz, unless otherwise specified. Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	V_{DD} Supply Range -- Operating		2.25		3.6	V
	V_{DD} Supply Range -- EEPROM Programming		2.6		3.6	V
V_{IN}	Analog Supply Voltage		2.2	3.3	5.5	V
AVDD	AVDD Output Voltage		5		18	V
V_{ON}	Positive Supply Voltage			25	40	V
V_{OFF}	Negative Supply Voltage		-25	-15		V
I_{IN_Q}	Input Quiescent Current	Not switching (OVP active)			3	mA
		Pin EN to ground			1	µA
BOOST						
$r_{(DS)ON}$	Switch ON-resistance	V_{IN} = 2.7V, I_{SW} = 1A		200	450	mΩ
$\Delta V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	2.2V < V_{IN} < 5.5V, I_{OUT} = 200mA, V_{AVDD} = 8V, L = 6.8µH, C_{OUT} = 10µF		2.9	5	mV/V
$\Delta V_{AVDD}/\Delta I_{OUT}$	Load Regulation	50mA < I_{OUT} < 0.5A, V_{IN} = 3.3V, V_{AVDD} = 7.8V, L = 6.8µH			90	mV/A
V_{FB}	Boost Feedback Voltage	Closed loop: V_{AVDD} = 8V, L = 6.8µH, I_{OUT} = 200mA, T_A = +25°C	1.205	1.230	1.255	V
I_B	FB Pin Bias Current				0.1	µA
I_{RHVS}	RHVS Pin Leakage Current	HVS pin to ground			100	nA
Res_{HVS}	HVS Pin Resistor	HVS pin to ground	105	130	155	Ω
V_{IH} HVS	Input Voltage HIGH	V_{IN} = 2.2V	1.5			V
V_{IL} HVS	Input Voltage LOW				0.44	V

Electrical Specifications VDD = V_{IN} = 3.3V, A_{VDD} = 12V, V_{ON} = 20V, V_{OFF} = -14V, T_A from -40°C to +85°C, Fcpv1 and Fcpv2 = 105kHz, unless otherwise specified. Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	Soft-Start Time			10		ms
D_{max}	Max Duty Cycle		80	85		%
D_{min}	Min Duty Cycle			15	20	%
F_{OSC}	Oscillator Switching Frequency	V_{AVDD} = 8V, I_{OUT} = 200mA, L = 6.8µH, D = ZHC750, C_{OUT} = 30µF	1.1	1.38	1.5	MHz
I_L	Switch Leakage Current				10	µA
T_{SH}	Thermal Shutdown Threshold	Activation threshold		150		°C
		De-activation threshold		130		°C
Th_{EN}	Enable Threshold	Output High	0.7		1.1	V
I_{EN}	Enable Pin Current				0.1	µA
I_{OCP}	Overcurrent Protection in the Power MOS	L = 6.8µH	2.2	2.7	3.2	A
OVP	Overvoltage Protection on Threshold		18.5		21.5	V
OVP_HYS	Overvoltage Protection Hysteresis			2		V
UVLO	Undervoltage Protection on Threshold		2.0	2.1	2.2	V
UVLO_HYS	UVLO Hysteresis			100		mV
VCOM AMPLIFIERS R_{LOAD} = 10kΩ, C_{LOAD} = 10pF, unless otherwise stated						
I_{SAMP}	Supply Current	4 Op amps combined	8		18	mA
V_{SAMP}	Supply Voltage		5	8	18.5	V
CMRR	Common Mode Rejection Ratio		50	70		dB
PSRR	Power Supply Rejection Ratio		70	85		dB
VOH	Output Voltage Swing High	I_{OUT} (source) = 5mA		A_{VDD} - 0.05		V
		I_{OUT} (source) = 50mA		A_{VDD} - 0.5		V
VOL	Output Voltage Swing Low	I_{OUT} (sink) = 5mA		0.05		V
		I_{OUT} (sink) = 50mA		0.5		V
V_{OFFSET}	Input Offset Voltage $(V_{IN+}) - (V_{IN-}) = V_{OFFSET}$		-15		15	mV
BW	Bandwidth	-3dB gain point		30		MHz
I_B	INx+, INx-, (x = 1, 2, 3, 4)		-1000	100	1000	nA
SR	Slew Rate			40		V/µs
I_{SC}	Output Short Circuit Current		150	250		mA
TEMPERATURE SENSOR, T_A = +25°C						
I_{TEMP}	Drive Current	For +1°C additional error		70		µA
V_{TEMP}	Offset Output Voltage at T_J = +100°C			1.600		V
$T_{ACCURACY}$	Temperature Accuracy	+50°C < T_J < +150°C		±5		°C
T_{RATIO}	Temperature Coefficient			9.5		mV/°C
LEVEL SHIFT, T_A = +25°C**,** 4.7nF in series with 50Ω loadings on CKV1, CKV2, CKVB1, CKVB2						
V_{ON}	Positive Supply Voltage			25	40	V
V_{OFF}	Negative Supply Voltage		-25	-15		V
F_{CPV}	Operating Frequency on CPV1, CPV2 Inputs			105	166	kHz
F_{OE}	Operating Frequency on OE Input			210	332	kHz

Electrical Specifications VDD = V_{IN} = 3.3V, A_{VDD} = 12V, V_{ON} = 20V, V_{OFF} = -14V, T_A from -40°C to +85°C, Fcpv1 and Fcpv2 = 105kHz, unless otherwise specified. Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	VDD Average Supply Current (V_{AVDD} < 4V)	CPV1 = CPV2 = 0, STV = 0, OE = 105kHz		500	1000	µA
I_{CPV1}	CPV1 Input Current	CPV1 = 1	-0.1		0.1	µA
		CPV1 = 0	-0.1		0.1	µA
I_{CPV2}	CPV2 Input Current	CPV2 = 1	-0.1		0.1	µA
		CPV2 = 0	-0.1		0.1	µA
I_{STV1}	STV1 Input Current	STV1 = 1	-0.1		0.1	µA
		STV1 = 0	-0.1		0.1	µA
I_{STV2}	STV2 Input Current	STV2 = 1	-0.1		0.1	µA
		STV2 = 0	-0.1		0.1	µA
I_{OE}	OE Input Current	OE = 1	-0.1		0.1	µA
		OE = 0	-0.1		0.1	µA
I_{OECON}	OECON Input Current	OE = 1	-1		1	µA
		OE = 0	-1		1	µA
I_{VDD}	VDD Quiescent Current (V_{AVDD} < 4V)	CPV1 = CPV2 = 0, STV = 0, OE = 0		250	500	µA
$IV_{ON\_quiescent}$	V_{ON} Quiescent Current (V_{AVDD} < 4V)	CPV1 = CPV2 = 0, STV = 0, OE = 0		700	1100	µA
$IV_{OFF\_quiescent}$	V_{ON} Quiescent Current (V_{AVDD} < 4V)	CPV1 = CPV2 = 0, STV = 0, OE = 0		600	1000	µA
UVLO	UVLO on VON	Activation threshold			13	V
		De-activation threshold	10			V
V_{IL} Level Shift	Low Input Voltage CPV1, CPV2, STV, OE				0.4	V
V_{IH} Level Shift	High Input Voltage CPV1, CPV2, STV, OE		70% V_{DD}			V
$V_{threshold}$	OECON Threshold Voltage	STV = 0, OE = 3.3V	1.6	1.7		V
V_{OL} Level Shift	Low Output Voltage CKV1, CKV2, CKVB1, CKVB2, STVP	No load			-13.5	V
V_{OH} Level Shift	High Output Voltage CKV1, CKV2, CKVB1, CKVB2, STVP	No load	19.5			V
t_r_CKV	CKV Rise Time	CKV rise time from +6V to +17V			0.73	µs
t_f_CKV	CKV Fall Time	CKV fall time from 0V to -11V			0.73	µs
t_r_STVP	STVP Rise Time	STVP rise time from -7V to +13V, C_{LOAD} = 4.7nF and in series with R_{LOAD} = 200Ω			0.5	µs
t_f_STVP	STVP Fall Time	STVP fall time from +13V to -7V, C_{LOAD} = 4.7nF and in series with R_{LOAD} = 200Ω			0.28	µs
t_d-OE-CKV+	CKV Rising Edge Delay Time	OE rising above 1.65V to CKV crossing + 11.5V			0.68	µs
t_d-OE-CKV-	CKV Falling Edge Delay Time	OE rising above 1.65V to CKV crossing - 5.5V			0.68	µs
t_d-STVP+	STVP Rising Edge Delay Time	STV crossing 1.65V to STVP crossing + 3V,			0.48	µs
t_d-STVP-	STVP Falling Edge Delay Time	OE rising above 1.65V to CKV crossing - 5.5V			0.35	µs
t_d-CKV-CS+	CKV_CS Rising Edge Delay Time	CPV falling below 1.65V to CKV crossing - 11V		1.6	2.44	µs
t_d-CKV-CS-	CKV_CS Falling Edge Delay Time	CPV falling below 1.65V to CKV crossing + 17V		1.6	2.44	µs
I^2C DC SPECIFICATION A_{VDD} = 10V, V_{OUT} = 5V, R_{SET} = 24.9kΩ						
A_{VDD}	A_{VDD} Supply Range	VDD range 2.6V to 3.6V	4.5		18	V
		VDD range 2.25V to 3.6V	4.5		13	V
$-I_{DD\_DCP}$	V_{DD} Supply Current	(Note 5)		50		µA

Electrical Specifications VDD = V_{IN} = 3.3V, A_{VDD} = 12V, V_{ON} = 20V, V_{OFF} = -14V, T_A from -40°C to +85°C, Fcpv1 and Fcpv2 = 105kHz, unless otherwise specified. Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{AVDD_DCP}	AVDD Supply Current	(Note 3)		25		µA
SET_{VR}	SET Voltage Resolution			7		Bits
SET_{DN}	SET Differential Non-linearity	Monotonic Over-Temperature			±1	LSB
SET_{ZSE}	SET Zero-Scale Error				±2	LSB
SET_{FSE}	SET Full-Scale Error				±8	LSB
ISET	SET Current	Through R_{SET} (Note 6)		20		µA
SET_{ER}	SET External Resistance	To GND, A_{VDD} = 18V	10		200	kΩ
		To GND, A_{VDD} = 4.5V	2.25		45	kΩ
A_{VDD} to SET	A_{VDD} to SET Voltage Attenuation	(Note 4)		1:20		V/V
OUT_{St}	OUT Settling Time	To ±0.5 LSB Error Band (Note 4)		8		µs
V_{OUT}	OUT Voltage Range		VSET + 0.5V		AVDD	V
SET_{VD}	SET Voltage Drift	(Note 4)		<10		mV
VIH_S	SDA, SCL, SCL_S, WPn Input Logic High		0.7* VDD			V
VIL_S	SDA, SCL, SCL_S, WPn Input Logic Low				0.3* VDD	V
	SDA, SCL, SCL_S, WPn Hysteresis	(Note 4)		0.22*VDD		V
IL_{WPN}	WPn IL			30	37	µA
VOH_S	SDA, SCL Output Logic High	@ 3mA	0.4			V
VOL_S	SDA, SCL Output Logic Low	@ 3mA			0.4	V
VOH_{WPP}	WPp Output Logic High	@ 3mA	VDD - 0.4			V
VOL_{WPP}	WPp Output Logic Low	@ 3mA	0.4			V
t_{DWPP}	WPp Delay				100	ns
R_{SCL}	SCL_S to SCL ON-resistance				75	Ω
t_S	Delay From SCL_S to SCL				60	ns
I^2C						
F_{SCL}	SCL Clock Frequency		0		400	kHz
t_{SCH}	I^2C Clock High Time		0.6			µs
t_{SCL}	I^2C Clock Low Time		1.3			µs
t_{DSP}	I^2C Spike Rejection Filter Pulse Width		0		50	ns
t_{SDS}	I^2C Data Set-up Time		100			ns
t_{SDH}	I^2C Data Hold Time		0		900	ns
t_{ICR}	I^2C SDA, SCL Input Rise Time	Dependent on Load (Note 4)		20 + 0.1*Cb	1000	ns
t_{ICF}	I^2C SDA, SCL Input Fall Time	(Note 4)		20 + 0.1*Cb	300	ns
t_{BUF}	I^2C Bus Free Time Between Stop and Start		1.3			µs
t_{STS}	I^2C Repeated Start Condition Set-up		0.6			µs
t_{STH}	I^2C Repeated Start Condition Hold		0.6			µs
t_{SPS}	I^2C Stop Condition Set-up		0.6			µs
Cb	I^2C Bus Capacitive Load	(Note 4)			400	pF
C_{SDA}	Capacitance on SDA	(Note 4)			10	pF

Electrical Specifications VDD = V_{IN} = 3.3V, A_{VDD} = 12V, V_{ON} = 20V, V_{OFF} = -14V, T_A from -40°C to +85°C, Fcpv1 and Fcpv2 = 105kHz, unless otherwise specified. Unless otherwise specified, parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
C_S	Capacitance on SCL, SCL_S	WPn = 0 (Note 4)			10	pF
		WPn = 1 (Note 4)			22	pF
t_W	Write Cycle Time				100	ms

NOTES:

3. Tested at A_{VDD} = 18V.
4. Limits established by characterization and are not production tested.
5. Simulated maximum current draw when programming EEPROM is 23mA, should be considered when designing Power Supply.
6. A typical current of 20µA is calculated using the A_{VDD} = 10V and R_{SET} = 24.9kΩ. The maximum suggested SET Current should be 120µA.

Timing Diagrams

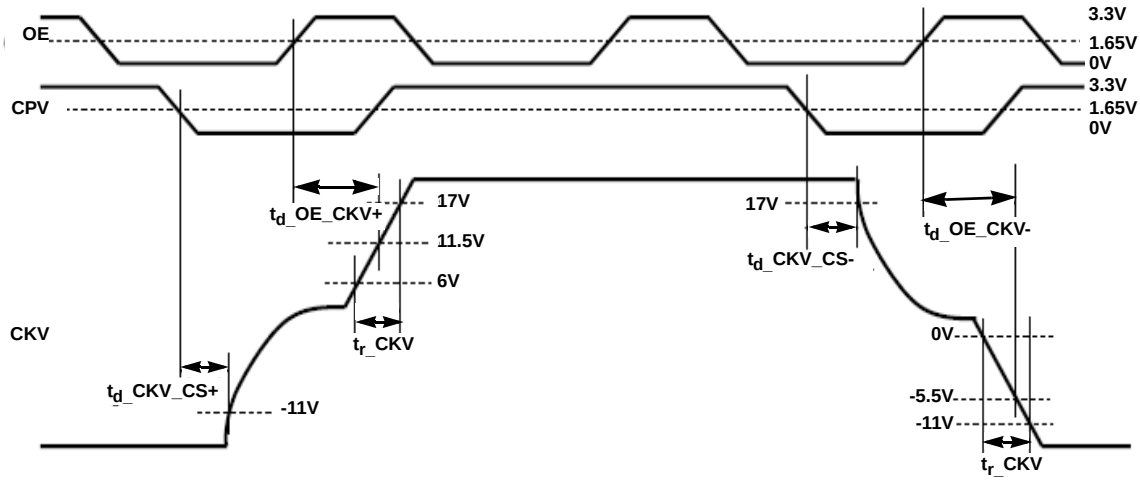


FIGURE 1. TIMING DIAGRAM OF OE, CPV, AND CKV

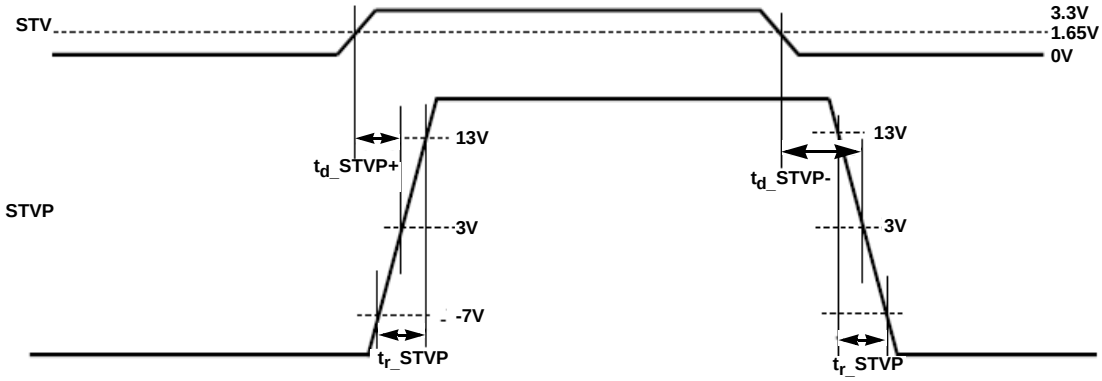
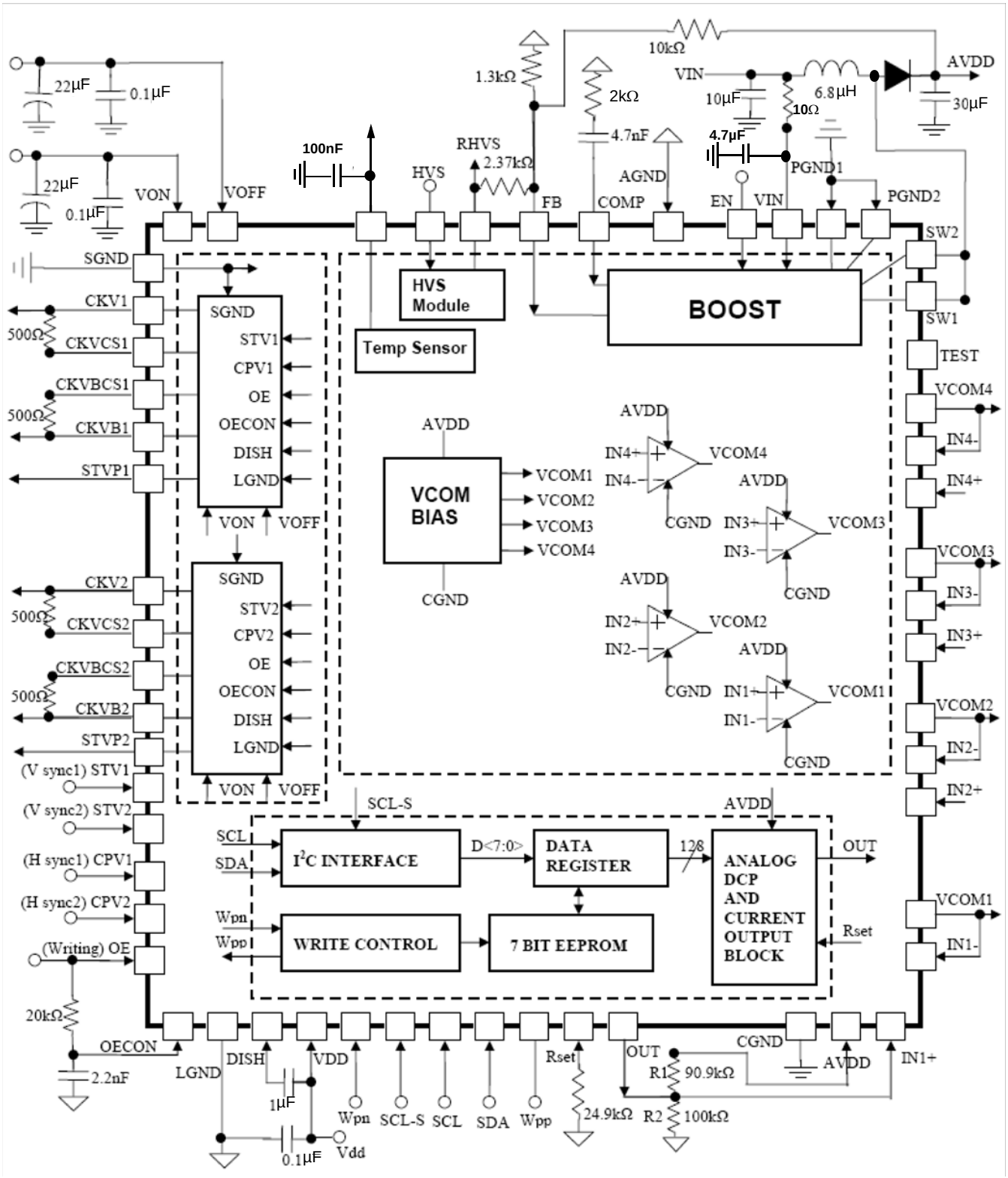


FIGURE 2. TIMING DIAGRAM OF STV AND STVP

Typical Application Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	CKVCS1	Discharge switch input 1, CKV1 charge share
2	CKVBCS1	Discharge switch input 1, CKVB1 charge share
3	CKVB1	High voltage output 1 , scan clock even
4	STVP1	High voltage output 1, scan start pulse 1
5	STVP2	High voltage output 2, scan start pulse 2
6	CKVB2	High voltage output 2, scan clock even
7	CKVBCS2	Discharge switch input 2, CKVB2 charge share
8	CKVCS2	Discharge switch input 2, CKV2 charge share
9	CKV2	High voltage output 2, scan clock odd
10	STV1	V_{SYNC} timing, V_{SYNC1}
11	STV2	V_{SYNC} timing, V_{SYNC2}
12	CPV1	H_{SYNC} timing, H_{SYNC} clock 1
13	CPV2	H_{SYNC} timing, H_{SYNC} clock 2
14	OE	H_{SYNC} timing, H_{SYNC} clock 3
15	OECON	OE disable input, OE blank
16	LGND	Logic GND
17	DISH	Discharge function input, V_{OFF} discharge
18	VDD	Logic power supply for scan driver and module calibrator
19	WPn	Write Protection Active Low. CMOS Level.
20	SCL_S	Serial Clock Input.
21	SCL	Serial Clock Input for internal and inter-IC use.
22	SDA	I^2C Serial Data Input/Output.
23	WPp	Write Protection Active High. CMOS Level.
24	RSET	Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AVDD/20) divided by RSET.
25	OUT	Adjustable Sink Current Output Pin. The current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maxim adjustable sink current setting.
26	IN1+	Op amp 1 non-inverting input
27	IN1-	Op amp 1 inverting input
28	VCOM1	Op amp 1 output
29	IN2+	Op amp 2 non-inverting input
30	IN2-	Op amp 2 inverting input
31	VCOM2	Op amp 2 output
32	IN3+	Op amp 3 non-inverting input
33	IN3-	Op amp 3 inverting input
34	VCOM3	Op amp 3 output
35	IN4+	Op amp 4 non-inverting input
36	IN4-	Op amp 4 inverting input
37	VCOM4	Op amp 4 output

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
38	CGND	VCOM GND
39	AVDD	VCOM amplifier positive supply pin
40	TEST	Test Pin
41	SW1	Boost switch output 1
42	SW2	Boost switch output 2
43	PGND1	Boost ground pins
44	PGND2	Boost ground pins
45	VIN	Boost supply voltage
46	EN	Chip Enable
47	AGND	Analog GND
48	COMP	Boost compensation pin
49	FB	A_{VDD} boost feedback pin
50	RHVS	Voltage set pin for HVS test
51	HVS	High-voltage stress input select pin
52	TEMP	Temperature sensor output voltage
53	VOFF	Negative supply
54	SGND	Scan driver GND
55	VON	Positive supply
56	CKV1	High voltage output 1 , scan clock odd

Typical Performance Curves

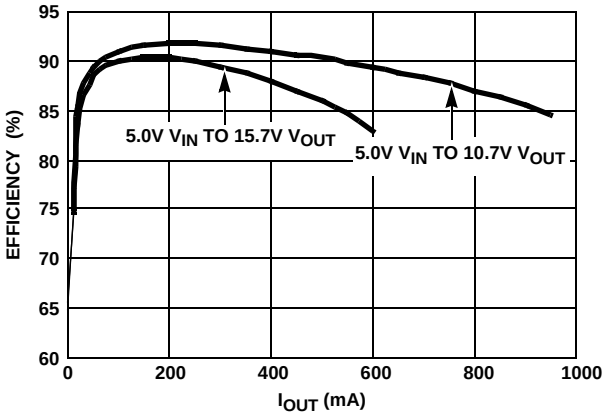


FIGURE 3. BOOST EFFICIENCY @ VIN = 5V

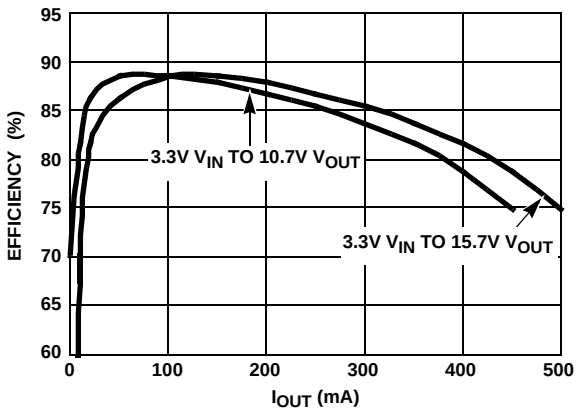


FIGURE 4. BOOST EFFICIENCY @ VIN = 3.3V

Typical Performance Curves (Continued)

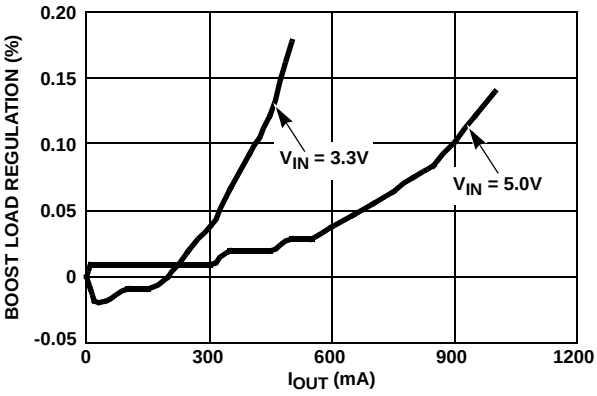


FIGURE 5. BOOST LOAD REGULATION @ AVDD = 10.7V

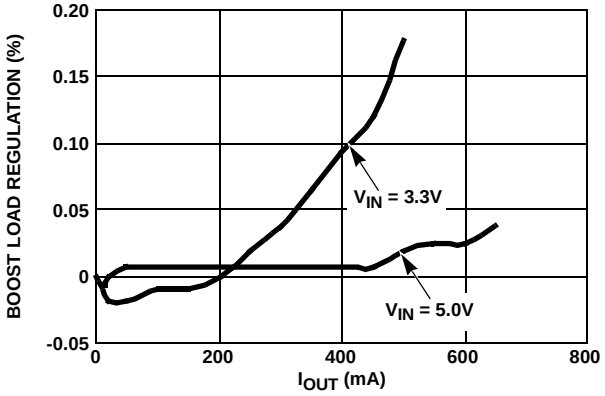


FIGURE 6. BOOST LOAD REGULATION @ AVDD = 15.7V

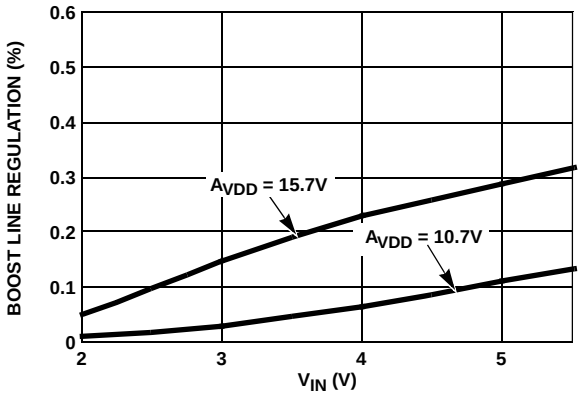


FIGURE 7. BOOST LINE REGULATION @ I_{OUT} = 50mA

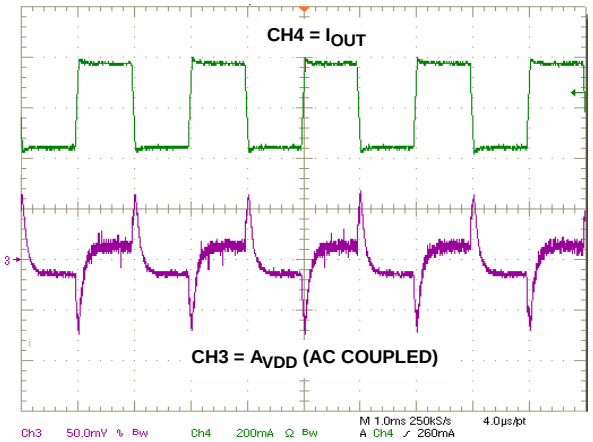


FIGURE 8. BOOST TRANSIENT RESPONSE

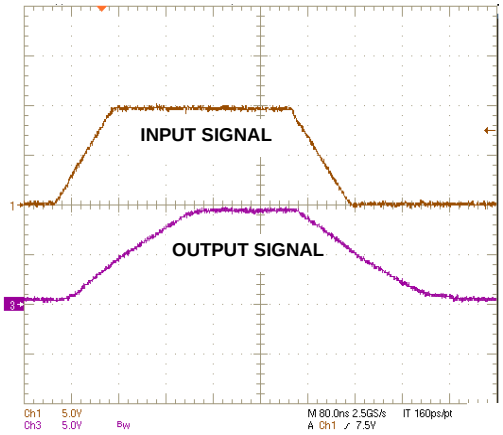


FIGURE 9. VCOM SLEW RATE

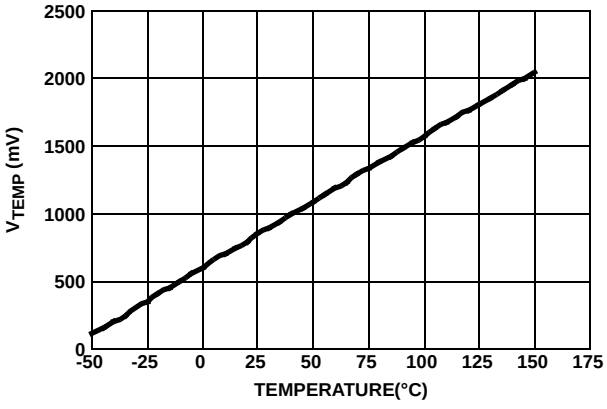


FIGURE 10. TEMPERATURE SENSOR OUTPUT vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

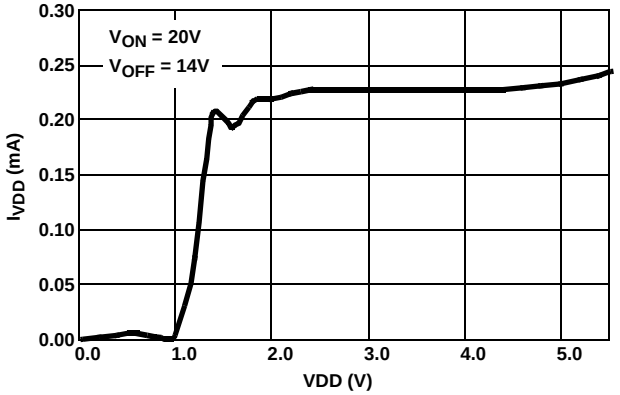


FIGURE 11. VDD SUPPLY CURRENT vs VDD

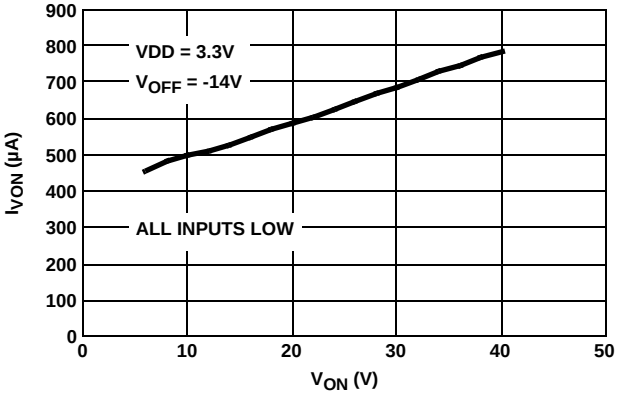


FIGURE 12. V_{ON} SUPLY CURRENT vs V_{ON}

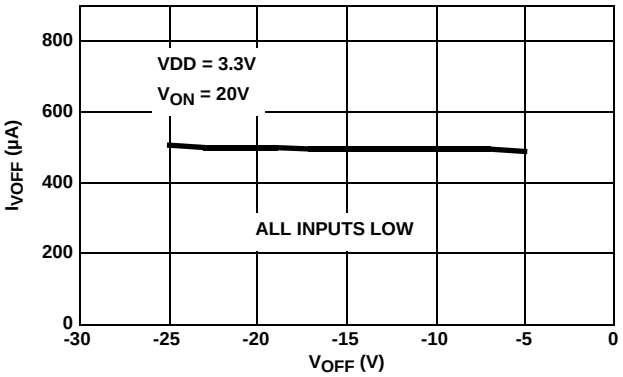


FIGURE 13. V_{OFF} SUPPLY CURRENT vs V_{OFF}

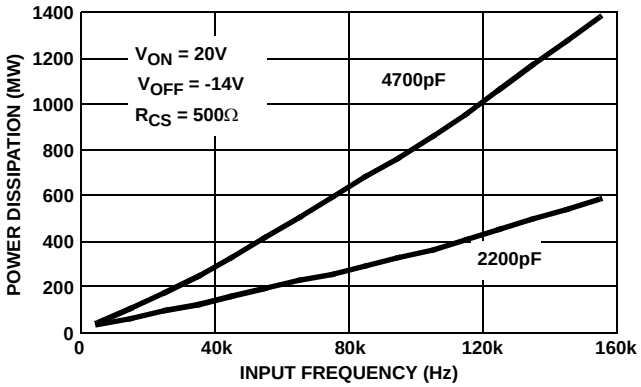


FIGURE 14. LEVEL SHIFT POWER CONSUMPTION vs CPV FREQUENCY

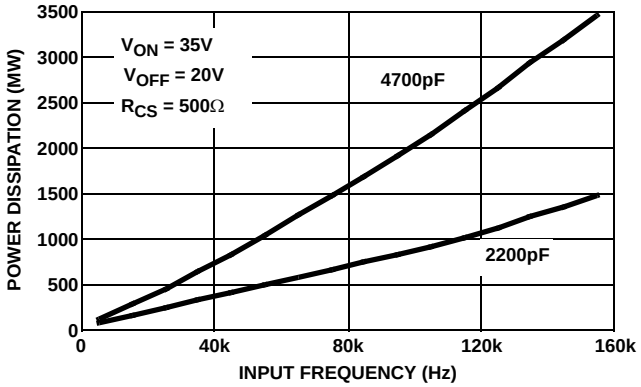


FIGURE 15. LEVEL SHIFT POWER CONSUMPTION vs CPV FREQUENCY

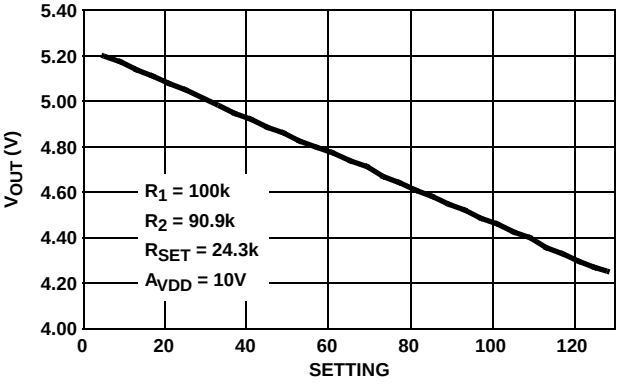


FIGURE 16. V_{OUT} vs SETTING

Application Information

A_{VDD} Boost Converter

The A_{VDD} boost converter features a fully integrated 2.7A boost FET. The regulator uses a current mode, PI control scheme which provides good line regulation and good transient response. A network connected to the COMP pin is used to compensate the device. In normal operation the output voltage is set using a resistor divider to the feedback pin FBB. The feedback reference voltage is set is to 1.23V.

In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{BOOST}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

Where D is the duty cycle of the switching MOSFET.

The boost converter uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 2:

$$V_{BOOST} = \frac{R_1 + R_2}{R_2} \times V_{FB} \quad \text{(EQ. 2)}$$

The current through the MOSFET is limited to $2.7A_{PEAK}$. This restricts the maximum output current (average) based on Equation 3:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

Where ΔIL is peak-to-peak inductor ripple current, and is set by Equation 4:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 4)}$$

where f_S is the switching frequency.

The minimum boost duty cycle of the ISL97648 is ~20% for 1.4MHz. When the operating duty cycle is lower than the minimum duty cycle, the part will not switch in some cycles randomly, which will cause some LX pulses to be skipped. In this case, LX pulses are not consistent any more, but the output voltage (A_{VDD}) is still regulated by the ratio of R_1 and R_2. Because some LX pulses are skipped, the ripple current in the inductor will become bigger. Under the worst case, the ripple current will be from 0 to the threshold of the current limit. In turn, the bigger ripple current will increase the output voltage ripple. Hence, it will need more output capacitors to keep the output ripple at the same level. When the input voltage equals, or is larger than, the output voltage, the boost converter will stop switching. The boost converter is not regulated any more, but the part will still be on and other channels are still regulated.

Boost Converter Input Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of input capacitor should be larger than the maximum input voltage. Some capacitors are recommended in Table 1 for input capacitor.

TABLE 1. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Boost Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH should be selected to match the internal slope compensation. The inductor must be able to handle the following average and peak current shown in Equations 5 and 6:

$$I_{LAVG} = \frac{I_O}{1-D} \quad \text{(EQ. 5)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 6)}$$

Some inductors are recommended in Table 2.

TABLE 2. BOOST INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	VENDOR	PART NUMBER
6.8µH/ $3A_{PEAK}$	7.3x6.8x3.2	TDK	RLF7030T-6R8N3R0
6.8µH/ $2.9A_{PEAK}$	7.6X7.6X3.0	Sumida	CDR7D28MNNP-6R8NC
5.2µH/ $4.55A_{PEAK}$	10x10.1x3.8	Cooper Bussmann	CD1-5R2

Rectifier Diode (Boost Converter)

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements.

Table 3 shows some recommendations for boost converter diode.

TABLE 3. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
SS23	30V/2A	SMB	Fairchild Semiconductor
SL23	30V/2A	SMB	Vishay Semiconductor

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor, as shown in Equation 7.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{AVDD}} \times \frac{1}{f_s} \quad \text{(EQ. 7)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across then increases. C_{OUT} in Equation 7 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

Table 4 shows some selections of output capacitors.

TABLE 4. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Loop Compensation (Boost Converter)

The boost converter of ISL97648 can be compensated by a RC network connected from VC pin to ground. C_C = 4.7nF and R_C = 10k RC network is used in the demo board. A higher resistor value can be used to lower the transient load change A_{VDD} overshoot (however, this may be at the expense of stability to the loop).

The stability can be examined by repeatedly changing the load between 100mA and a max level that is likely to be used in the system being used. The A_{VDD} voltage should be examined with an oscilloscope set to AC 100mV/div and the amount of ringing observed when the load current changes. Reduce excessive ringing by reducing the value of the resistor in series with the COMP pin capacitor.

HVS Operation

When the HVS input is taken high, the ISL97648 enters HVS test mode. In this mode, the output of A_{VDD} is increased by switching RSET-HVS to ground to select the test voltage.

Fault Protection

The ISL97648 integrates OVP, OCP and over-temperature protection.

Temperature Sensor

The ISL97648 also includes a temperature output for use in system thermal management control. The integrated sensor measures the die temperature over the 0°C to +150°C range. Output is in the form of an analog voltage on the TEMP pin in the range of 0.5V to 2.0V. Temperature accuracy is ±5°C.

Soft-Start

The ISL97648 integrates the soft-start function and the timing diagram is shown in the Figure 17. The boost switch goes through soft-start sequence after the EN pin is pulled to high.

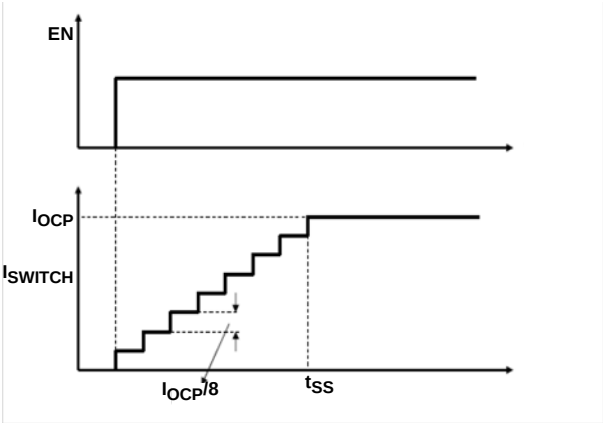


FIGURE 17. BOOST SOFT-START OF CURRENT LIMIT

High Performance VCOM Amplifiers

The VCOM Amplifiers are designed to control the voltage on the back plate of an LCD display or to drive the repaired column lines. The plate is capacitive coupled to the pixel drive voltage which alternately cycles positive and negative at the line rate for the display. Thus, the amplifier must be capable of sourcing and sinking capacitive pulses of current, which can occasionally be quite large (a few 100mA for typical applications).

The ISL97648 VCOM Amplifier's output current is limited to 150mA. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained (in this case the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir

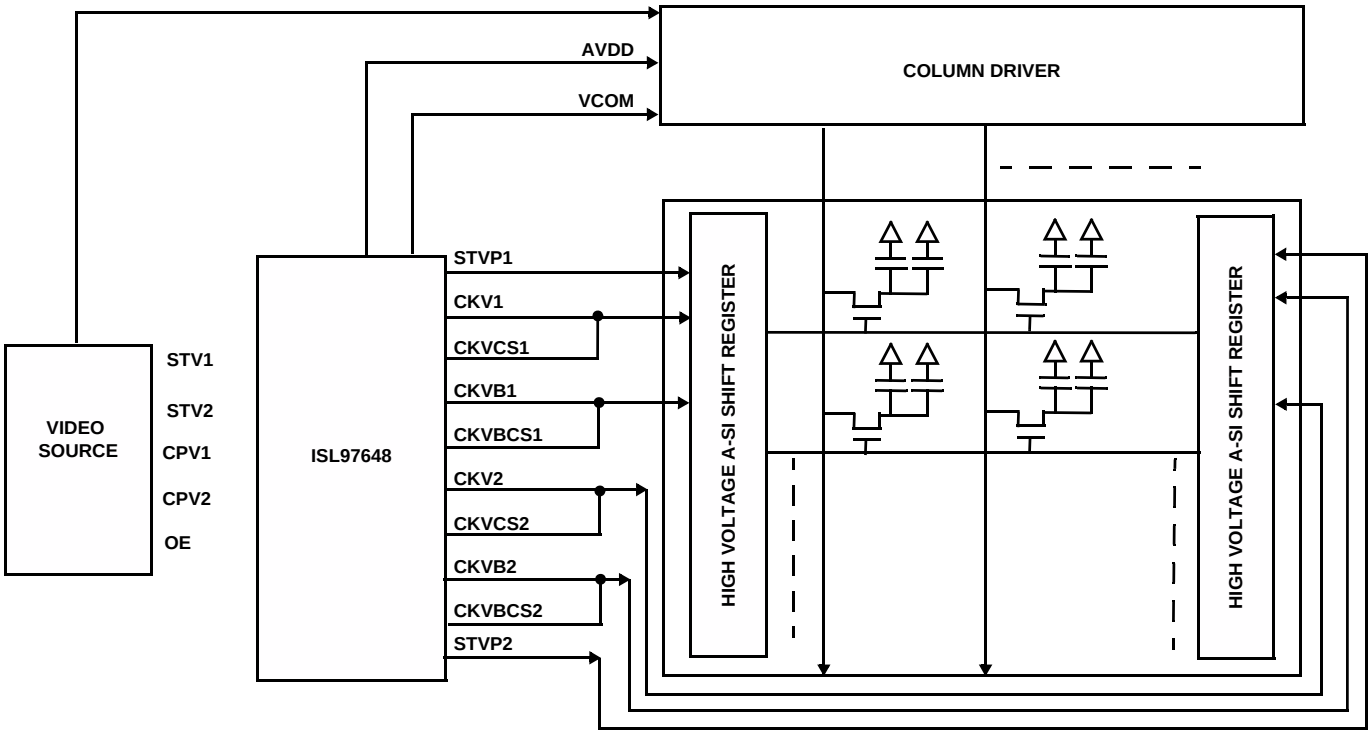


FIGURE 18. SYSTEM BLOCK DIAGRAM RELATED TO LEVEL SHIFT OUTPUT

capacitor back up once the pulse has stopped. This will happen on the µs time scale in practical systems and for pulses 2x or 3x the current limit, the V_{COM} voltage will have settled again before the next line is processed.

Level Shifter

GENERAL DESCRIPTION

The ISL97648 is a high performance 65V TFT-LCD level shifter. It level shifts TTL level timing signals from the video source into 65V peak-to-peak output voltage. Its output is capable of delivering 100mA peak current into 5nF of capacitive load. It also incorporates logic to control the output timings. The logic timing control circuit is powered rom VDD supply. Figure 18 shows the system block diagram related to level shifter part.

Input Signals

The device performs beside of level transformation also logic operation between the input signals:

- STV1 - Vertical Sync Timing signal 1, frequency range from 60Hz to 120Hz
- STV2 - Vertical Sync Timing signal 2, frequency range from 60Hz to 120Hz
- CPV1- Horizontal Sync Timing signal 1, frequency range up to 166kHz
- CPV2- Horizontal Sync Timing signal 2, frequency range up to 166kHz
- OE- Output Enable Write Signal, frequency range up to 332kHz

Output Signals

The output signals, CKV and CKVB are generated by ISL97648 internal switches. Figure 19 depicts the simplified schematic of the output stage and interface.

C_L capacitors model the capacitive loading appeared at the inputs of the TFT-LCD panel for the CKV1, CKVB1, CKV2, and the CKVB2 signals. The C_L is typically between 1nF and 5nF.

In addition to switches SW1, SW2, SW3, SW4, SW5, SW6, SW7, and SW8, the ninth and tenth switches are added to reduce the power dissipation and shape the output waveform. Figure 19 shows the location of the additional SW9 and SW10 switches.

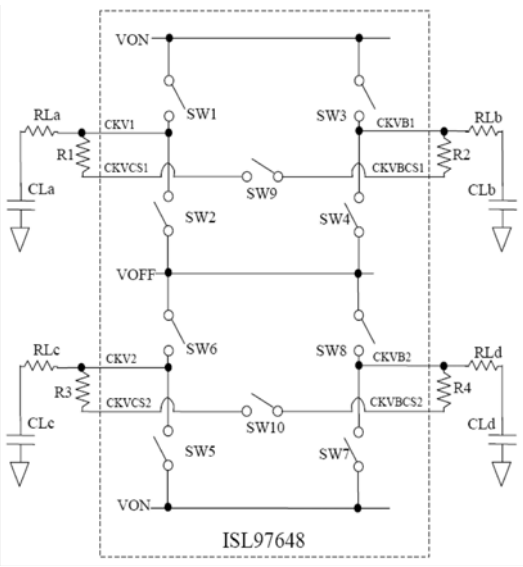


FIGURE 19. SIMPLIFIED SCHEMATIC OF OUTPUT STAGE

In reality, each switch consists of two such switches, one for the positive discharge and one for the negative discharge, see Figure 20..

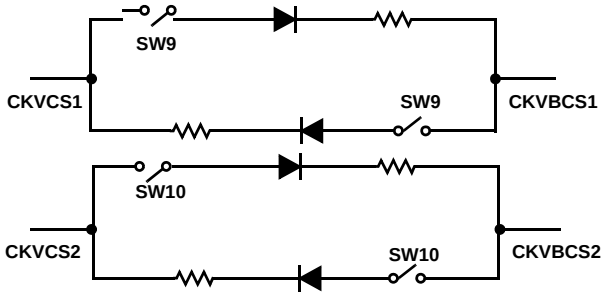


FIGURE 20. BI-DIRECTIONAL SWITCHES

Due to the actual solid-state construction of the switches, the capacitors C_L does not get discharged entirely. The amount of left over charges depends on the value of the voltages of V_{ON} and V_{OFF} on the capacitors.

Internal Logic Block Diagram

Figure 21 shows the internal block diagram. In order to reduce power dissipation, most of the logic circuitry is powered from VDD logic supply. The output of the VDD logic is level-shifted to drive the output switches.

Internal Logic Table

CKV, CKB, CKVCS AND CKVBCS

The Internal logic block of CKV1 and CKV2 are identical and only one logic block and truth table are shown in Figure 21 and Table 5. To generate the CKV, CKVB and charge sharing outputs, the internal logic goes through 3 steps as outlined in the following paragraphs.

Step 1: Generation of internal clock from the inputs,

$$CLK = CPV \oplus (OE \otimes \overline{OECON})$$

$$OECON = Low(STV = High)$$

$$OECON = Hi-Z(STV = Low)$$

TABLE 5. CLK SIGNAL GENERATION

CPV	OE	OECON	CLK
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Step 2: The CLK clock dries a flip-flop with complementary output Q and $\overline{Q}$. The flip-flop is reset by STV signal.

TABLE 6. INTERNAL FLIP-FLOP OUTPUTS

CLK	STV	Q	$\overline{Q}$
0 --> 1	0	$\overline{Q}$(N-1)	Q(N-1)
X	1	0	1

Step 3: The 2 complementary outputs CKV and CKVB can be high, low or high-impedance, as shown in Table 7:

TABLE 7. CKV, CKVB, CKVCS AND CKVBCS

CLK	$\overline{Q}$	STV	CKV	CKVB
0	0	0	Hi-Z	Hi-Z
0	1	0	Hi-Z	Hi-Z
1	0	0	Low	High
1	1	0	High	Low
0	0	1	NA	NA
0	1	1	Low	High
1	0	1	NA	NA
1	1	1	High	Low

Hi-Z is output high impedance and charge sharing is enabled. NA is illegal state and cannot occur.

STVP

STVP output is controlled by STV input and the internal CLK signal. Table 8 shows the relationship:

TABLE 8. STVP OUTPUT

CLK	STV	STVP
0	0	Low
0	1	High
1	0	Low
1	1	Hi-Z

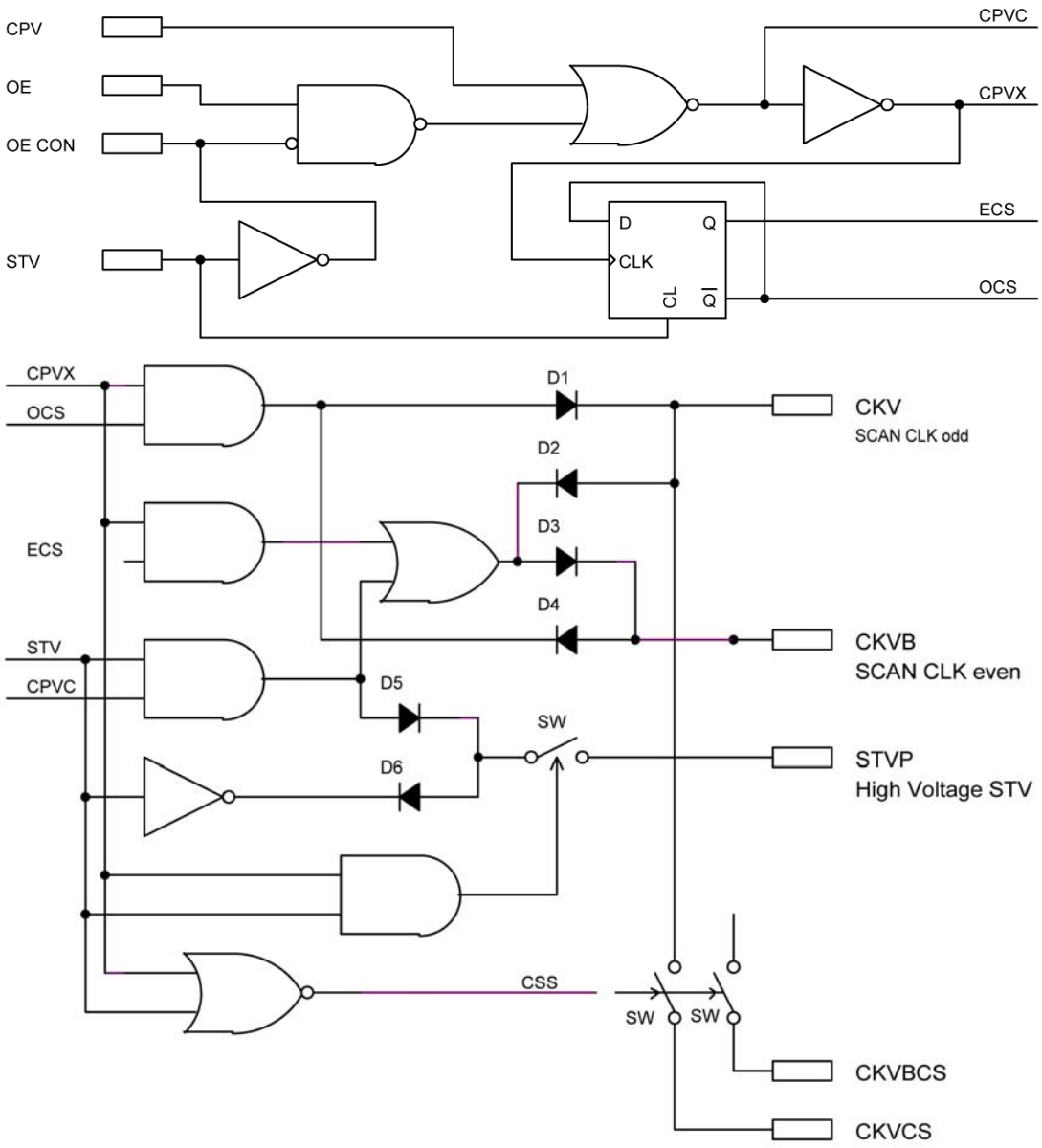


FIGURE 21. INTERNAL LOGIC BLOCK DIAGRAM

Output Waveforms

Figure 22 shows a typical CKV and CKVB output waveforms. The output droop rate depends on the external discharge resistor value and the output capacitor load.

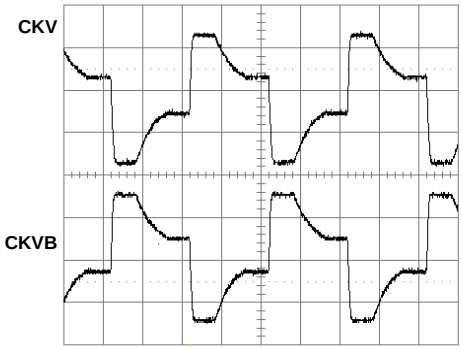


FIGURE 22. CKV AND CKVB OUTPUT WAVEFORMS

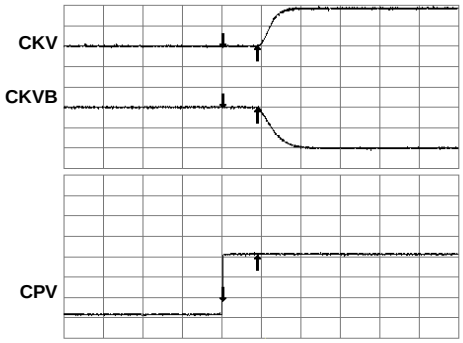


FIGURE 23. CPV TO CKV/CKVB DELAY

Figure 23 shows the delay time between the incoming horizontal sync timing pulse CPV and the generated output pulses. Δt is dependent mainly on the value of C_L. Figure 24 shows the effect of STV..

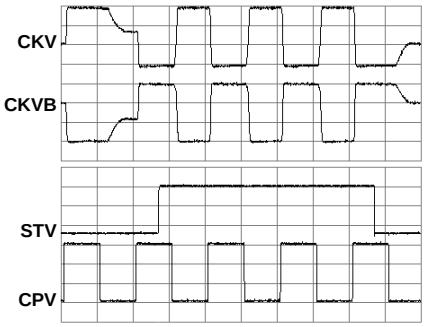


FIGURE 24. EFFECT OF STV

Auxiliary Functions

DISH: It discharges V_{OFF} when the logic power voltage level drops out, when 'DISH' is < -0.6V (V_{CC} system power turns off), V_{OFF} is connected to ground level by 1kΩ.

OECON: It provides continuos polarity changes to the TFT-LCD panel during the vertical blanking.

Power Dissipation

The dissipated power of chagrge sharing in R_1 and R_2 could be calculated as follows:

We assume that:

- V_{ON} = 40V
- V_{OFF} = -20V
- H_{SYNC} timing (CPV); frequency = 60kHz
- C_L = 5nF

The value of V_L, the left over voltage in the capacitors in that case is 23V for the positive discharge and 3.0V for the negative discharge.

The voltage change across the capacitor is therefore 23V (see Figure 25).

The stored energy in the capacitor is shown in Equation 8:

$$1/2 \times V^2C = 1/2 \times 23^2 \times 5 \times 10^{-9} = 1.32\mu W \quad \text{(EQ. 8)}$$

The energy which is stored in the capacitor will be dissipated on the resistor (see Figure 26). The switch will close 60,000 in every second.

Since the process will be repeated 2x, for the CKV and the CKVB. In 60,000 cycles per second the power dissipation in R_1 and R_2 becomes Equation 9.

$$2 \times 1.32 \times 10^{-6} \times 60x10^3 = 160mW \quad \text{(EQ. 9)}$$

The dissipated power of level shift driving in R_{la} and R_{lb} could be calculated as follows:

The voltage change across the capacitor is 37V when the level shift driving the capacitor to V_{ON} or V_{OFF} (see Figure 27).

The stored energy in the capacitor is calculated in Equation 10:

$$1/2 \times V^2C = 1/2 \times 37^2 \times 5 \times 10^{-9} = 3.42\mu W \quad \text{(EQ. 10)}$$

Consequently, in 60,000 cycles per second the power dissipation in R_{la} and R_{lb} becomes Equation 11:

$$2 \times 3.42 \times 10^{-6} \times 60x10^3 = 410mW \quad \text{(EQ. 11)}$$

Since there are also the same power consumption at R_3, R_4, R_{lc} and R_{ld}, the total power dissipation is Equation 12:

$$2x(410 + 160) = 1140mW \quad \text{(EQ. 12)}$$

Figures 25, 26, 27, and 28 show the total power dissipation over a range of possible voltages, operating frequencies and loads. The values of the R_1 and R_2 must be selected such that the capacitor C_L is discharged via R_1 or R_2 resistor in one half period of the H_{SYNC} timing. Care should be taken to prevent the power from exceeding the maximum rating of the package.

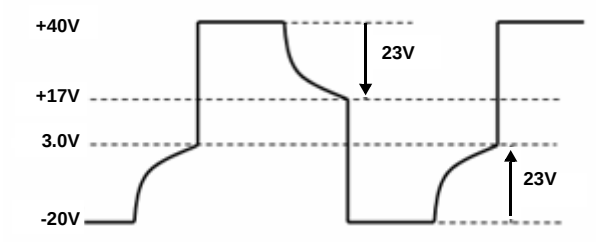


FIGURE 25. VOLTAGE CHANGE ACROSS THE CAPACITOR WHEN CHARGE SHARING BETWEEN CKV AND CKVB

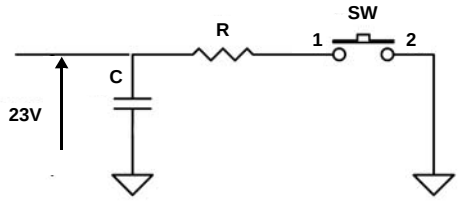


FIGURE 26. ENERGY DISSIPATED ON THE RESISTOR WHEN CHARGE SHARING

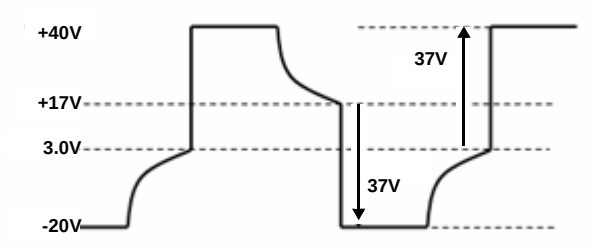


FIGURE 27. VOLTAGE CHANGE ACROSS THE CAPACITOR WHEN DRIVING

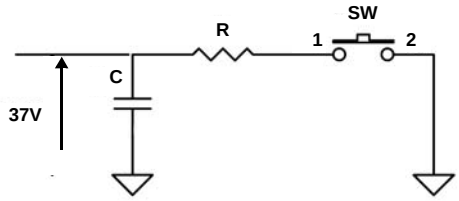


FIGURE 28. ENERGY DISSIPATED ON THE RESISTOR WHEN DRIVING

I^2C LCD Module Calibrator

Truth Table

TABLE 9. DVR WRITE PROTECTION TRUTH TABLE

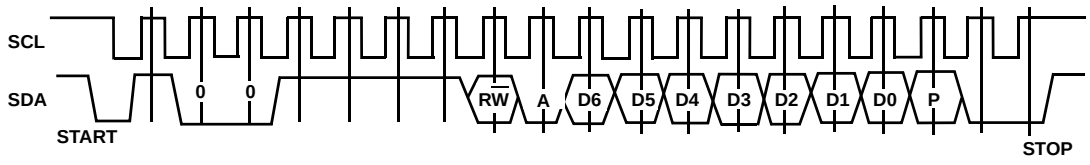
INPUT			OUTPUT		
WPn	**SCL_S**	**SCL**	**WPp**	**REGISTER**	**EEPROM**
LOW	UNUSED	INPUT	HIGH	Write Protect	Write Protect
HIGH	CONNECTED TO SCL	CONNECTED TO SCL_S	LOW	Writeable	Writeable
HIGH to LOW	DISCONECTS FROM SCL	DISCONECTS FROM SCL_S	LOW to HIGH	EEPROM is Read into Register	EEPROM is Read into Register
FLOAT (Pull-Down Resistor Included)	UNUSED	INPUT	HIGH	Write Protect	Write Protect

NOTE: When the device is not write-protected SCL_S and SCL signals should not be driven at the same time. When SCL_S signal is “Unused” should be left floating.

I^2C Bus Format

START	SLAVE ADDRESS							W R	A	DATA								A	STOP
	1	0	0	1	1	1	1			D6	D5	D4	D3	D2	D1	D0	P		

P: PROGRAM



When Read Operation, don't care P.
P = 1: Register Writing
P = 0: EEPROM Writing (Program)

Output Connection

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the VCOM voltage during production test and alignment. A 128-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current (see Figure 29).

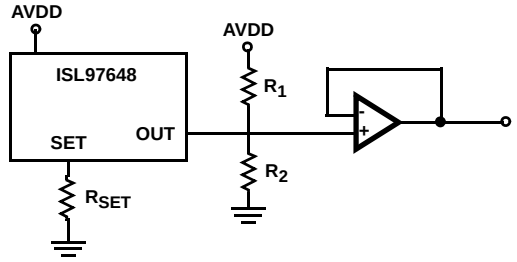


FIGURE 29. OUTPUT CONNECTION CIRCUIT EXAMPLE

The adjustment of the output is provided by the 2-wire I^2C serial interface.

Adjustable Sink Current Output

The device provides an output sink current which lowers the voltage on the external voltage divider. Equations 13 and 14 control the output. See Figure 29.

$$IOUT = \frac{Setting}{128} X \frac{AVDD}{20(RSET)} \quad \text{(EQ. 13)}$$

$$VOUT = \left(\frac{R2}{R1+R2}\right) VAVDD\left(1 - \frac{Setting}{128} X \frac{R1}{20(RSET)}\right) \quad \text{(EQ. 14)}$$

Note: Where setting is an integer between 1 and 128.

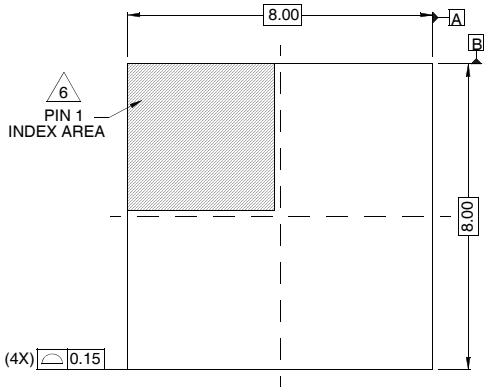
Ramp-up of the VDD Power Supply

It is required that the ramp-up from 10% VDD to 90% VDD level be achieved in less than or equal to 10ms to assure that the EEPROM and Power-on-reset circuits are synchronized and the correct value is read from the EEPROM Memory.

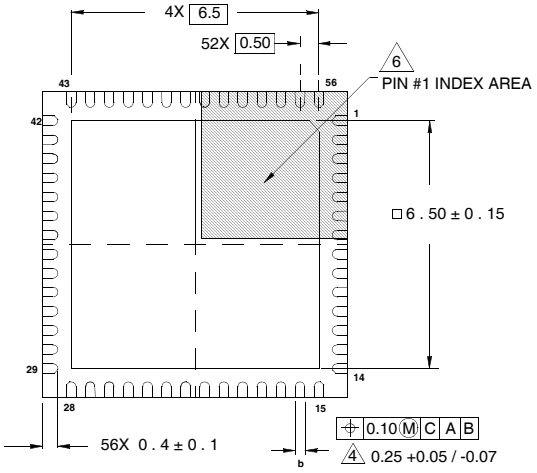
Package Outline Drawing

L56.8x8D

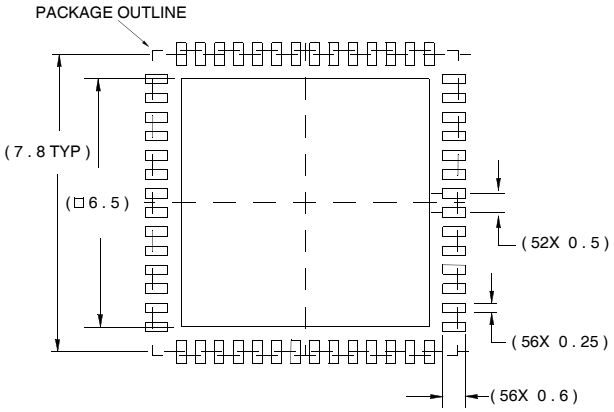
56 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 04/07



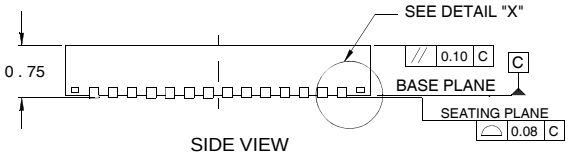
TOP VIEW



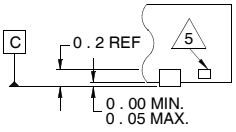
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.