M2005-01

Frequency Translator

DESCRIPTION

The M2005-01 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for reference clock frequency translation and jitter attenuation in a high speed data communications system. The device is similar to the M2004-01 but includes a frequency hold-over feature that allows the output frequency to be maintained in the event of a disrupted input reference clock. Internal divider ratios are user selectable, and external loop filter components allow tailoring of the PLL loop response.

FEATURES

- **Integrated SAW (surface acoustic wave) delay line**
- **Output clock frequency up to 700MHz (Consult factory for available frequencies)**
- **RMS Jitter <1ps RMS (12kHz-80MHz)**
- **Hold-over error +10ppm max**
- **Single 3.3V supply**
- **Small 9x9mm SMT package includes SAW device**
- **Ideal for OC-48, SDH-12, 10GbE transmit clock**

ABSOLUTE MAX RATINGS

Inputs, V_I: ..... -0.5 to V_{CC}+0.5V
Output, V_O: ..... -0.5 to V_{CC}+0.5V
Supply Voltage, V_{CC}: ..... 4.6 V
Storage Temperature, T_{STO}: ..... -45°C to +100°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics *or* AC Characteristics *is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.*

ISO 9001 Registered

FUNCTIONAL BLOCK DIAGRAM

The internal PLL will adjust the VCSO output frequency to be M (feedback divider) divided by P (input divider) times the selected input reference clock frequency. Note that the ratio of M/P times input frequency must be such that it falls within the "lock" range of the VCSO. The M divider (17-bits) can be programmed for a maximum value of 131,071 and a minimum value of 4. The P divider (9-bits) can be set to a maximum value of 511 and a minimum value of 1. The N output divider can be programmed to divide the VCSO output frequency by 1, or 4 and provide a 50% output duty cycle.

The M2005-01 is serially programmed via a 3 wire interface. Figure 1 shows the timing diagram for serial programming.

The relationship between the VCSO frequency, the M & P dividers, and the input REF_CLK is defined as follows:

$$F\ VCSO = F\ REF\_CLK \times \frac{M}{P}$$

When the N output divider is included, the complete relationship for the output frequency is defined as:

$$FOUT = \frac{F\ VCSO}{N} = F\ REF\_CLK \times \frac{M}{N \times P}$$

The N1 input can be hard wired to set the N divider to a specific state that will automatically occur during power-up.

Serial operation occurs when S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW to- HIGH. The M divider and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK.

When the HOLD input is asserted the M2005-01 will revert back to the initial accuracy of the VCSO and remain at that frequency until the HOLD signal is returned LOW.

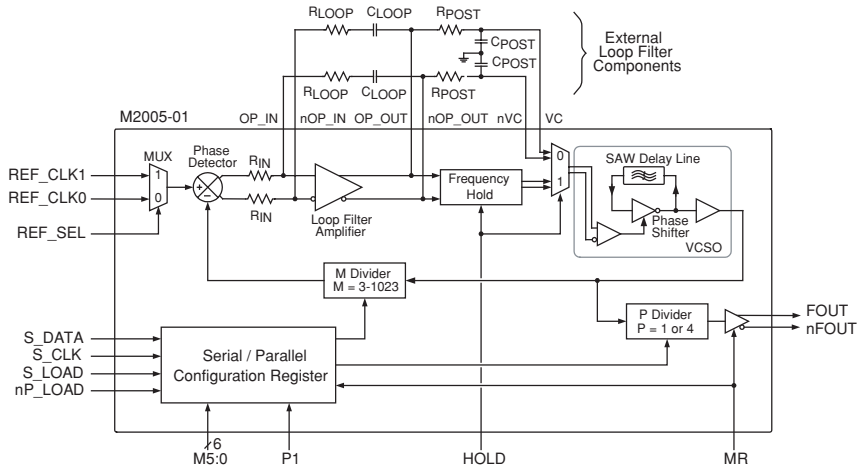
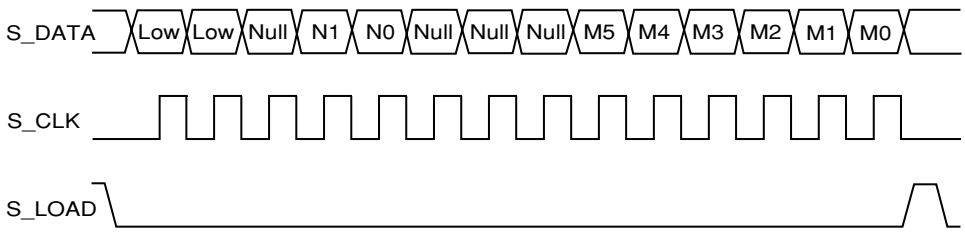


FIGURE 1



FUNCTIONAL DESCRIPTION

LOOP FILTER

The M2005-01 requires the use of an external loop filter via the provided filter pins. Due to the differential design, the implementation requires two identical RC filters as shown in Figure 2.

FIGURE 2

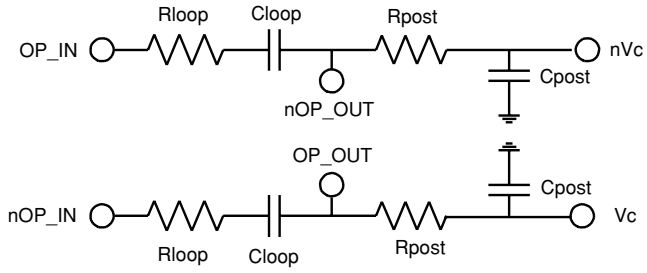


TABLE 1. RECOMMENDED LOOP FILTER VALUES

REF_CLK Frequency	VCSO Frequency	M	N	FOUT	Rloop	Cloop	Rpost	Cpost
19.44MHz	622.0800MHz	32	1	622.0800MHz	5kΩ	1MF	50kΩ	100pf

PIN DESCRIPTIONS

TABLE 2

Pin Number	Name	I/O	Configuration	Description
1, 2, 3	GND	GND		Power Supply Ground
4, 9	OP_IN, nOP_IN	Analog I/O		Used for external loop filter. See Figure 2.
5, 8	nOP_OUT, OP_OUT	Analog I/O		Used for external loop filter. See Figure 2
6, 7	nVC, VC	Input		VCSO Differential Control Voltage Input Pair
10, 14, 26	GND	GND		Power Supply Ground
11, 19, 22, 33	Vcc	Power		Positive Supply Pins
12	HOLD	Input	Pull - down	When HIGH the device operates in digital HOLD mode. LVCMOS / LVTTL interface levels.
13	N1	Input	Pull - down	Determines the output divider value as defined in Table 3C. LVCMOS / LVTTL interface levels.
15, 16	FOUT, nFOUT	Output	Unterminated	Differential output, 3.3V LVPECL levels.
17	MR	Input	Pull - down	Logic HIGH resets the reference frequency and N output dividers. Logic LOW enables the outputs. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pull - down	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK.
20	S_DATA	Input	Pull - down	Shift register serial input. Data is sampled on the rising edge of S_CLOCK.
21	S_LOAD	Input	Pull - down	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels
23	REF_CLK 1	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
24	REF_CLK 0	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
25	REF_SEL	Input	Pull - down	Selects between the different reference clock inputs as the PLL reference source. See Table 3D. LVCMOS / LVTTL interface levels.
27, 28, 29, 30, 31 32, 34, 35, 36	N/C			No connection. Internal test pins.

PIN CHARACTERISTICS

TABLE 4

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

PARALLEL & SERIAL MODES FUNCTION

TABLE 5A

Inputs							
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	Conditions
H	X	X	X	X	X	X	Reset, Forces outputs LOW.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

Note: L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

PARALLEL MODE FUNCTION

TABLE 5B

Inputs N1	Inputs N2	N Divider Value	Output Frequency (MHz) Min	Output Frequency (MHz) Max
0	0	1	311	700
1	0	4	77.75	175

SERIAL MODE FUNCTION

TABLE 5C

Inputs REF_SEL	Inputs Reference
0	REF_CLK0
1	REF_CLK1

POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			162		mA

V_{CC}= 3.3V ±5%, T_A= 0°C to 70°C

LVCMOS/LVTTL DC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
V_{IH}	Input High Voltage	REF_SEL, S_LOAD, S_DATA, S_CLOCK, N1, MR		2	VCC + 0.3	V
		REF_CLK0, REF_CLK1		2	VCC + 0.3	V
V_{IL}	Input Low Voltage	REF_SEL, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, MR		-0.3	0.8	V
		REF_CLK0, REF_CLK1		-0.3	1.3	V
I_{IH}	Input High Current	N1, MR, S_CLOCK, S_DATA, S_LOAD, REF_SEL, REF_CLK0, REF_CLK1	V_{DD} = V_{IN} = 3.465V		150	µA
I_{IL}	Input Low Current	N1, MR, S_CLOCK, S_DATA, S_LOAD, REF_SEL, REF_CLK0, REF_CLK1	V_{DD} = 3.465, V_{IN} = 0V	-5		µA
V_{OH}	Output High Voltage; NOTE 1			2.6		V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

Note 1: Outputs terminated with 50Ω to V_{CC} /2. See Parameter Measurement section, 3.3V Output Load Test Circuit.

LVPECL DC CHARACTERISTICS

Symbol	Parameter	Signal	Min	Max	Units
V_{OH}	Output High Voltage	FOUT, nFOUT	Vcc – 1.4	Vcc – 1.0	V
V_{OL}	Output Low Voltage	FOUT, nFOUT	Vcc – 2.0	Vcc – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	FOUT, nFOUT	0.6	0.85	V

Note 1: Output terminated with 50Ω to V_{CC}–2.V

INPUT FREQUENCY CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
F_{IN}	Input Frequency	REF_CLK0, REF_CLK1		0.3	166	MHz
		S_CLOCK			50	V

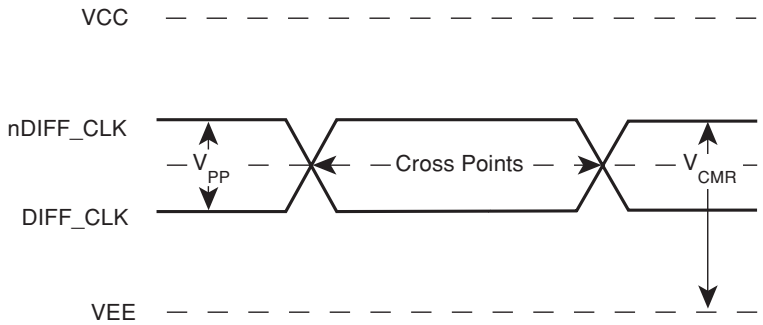
Note: Output terminated with 50Ω to V_{CC}–2.V

AC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency			77.75		667	MHz
ØNOISE	Single Side Band Phase Noise		1kHz offset		-72		dBc/Hz
			10kHz offset		-94		dBc/Hz
			100kHz offset		-123		dBc/Hz
J (t)	Jitter (RMS)		12kHz to 20 MHz		0.69		ps
odc	Output Duty Cycle				50		%
t_R	Output Rise Time	FOUT = 155MHz	20% to 80%, each	300		800	ps
t_S	Setup Time	M, N, to nP_LOAD		5			ns
		S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_H	Hold Time	M, N, to nP_LOAD		5			ns
		S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_{LOCK}	PLL Lock Time					1	ms
t_{PW}	Output Pulse Width	S_LOAD				TBD	ns
F_{HOLD}	Initial Frequency Accuracy in Digital HOLD Mode		Stable Input Clock Selected Until Entering Digital Hold		10		ppm

PARAMETER MEASUREMENT INFORMATION

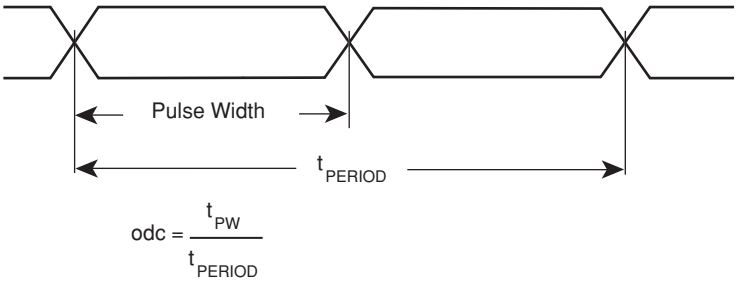
DIFFERENTIAL INPUT LEVEL



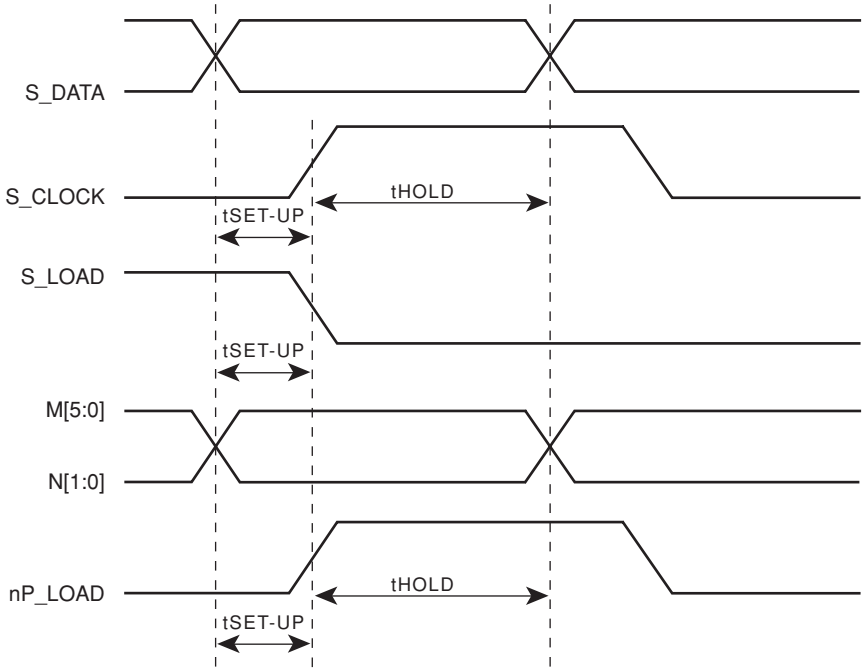
INPUT AND OUTPUT RISE AND FALL TIME

PARAMETER MEASUREMENT INFORMATION

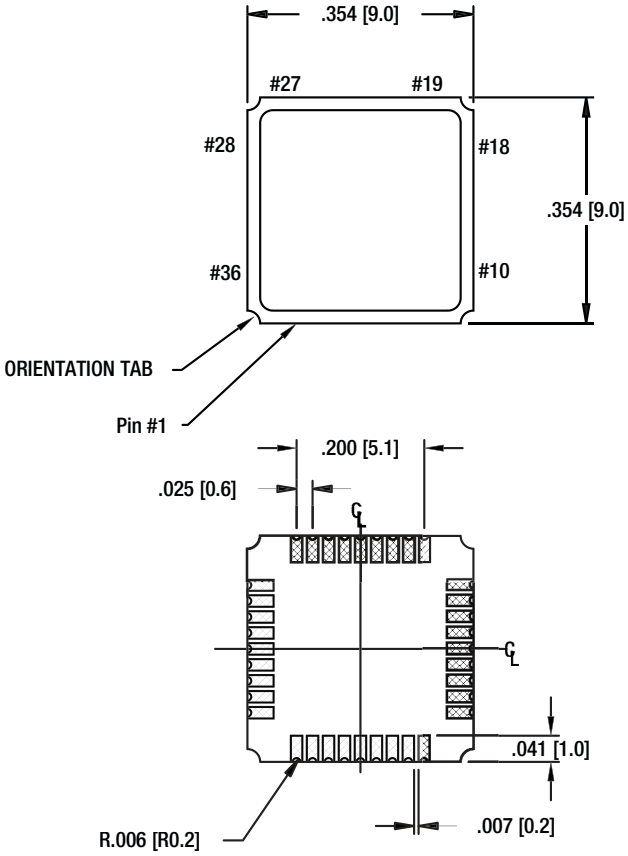
ODC & t_{PERIOD}

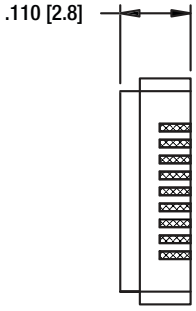


SETUP AND HOLD TIME



MECHANICAL DIMENSIONS & PIN CONFIGURATION





PIN#	DESIGNATION
1	GND
2	GND
3	GND
4	OP_IN
5	nOP_OUT
6	nVC
7	VC
8	OP_OUT
9	nOP_IN
10	GND
11	VDD
12	HOLD
13	N1
14	GND
15	FOUT
16	nFOUT
17	MR

PIN#	DESIGNATION
18	S_CLOCK
19	VDD
20	S_DATA
21	S_LOAD
22	VDD
23	REF_CLK1
24	REF_CLK0
25	REF_SEL
26	GND
27	N/C
28	N/C
29	N/C
30	N/C
31	N/C
32	N/C
33	VDD
34, 35, 36	N/C

1. DIMENSIONS ARE IN INCHES, ( ) ARE IN MM.

ORDERING INFORMATION

Part Number **M2005-01 - 622.0800**

Series
Model
VCSO Frequency
(i.e. 622.0800MHz)

Available VCSO Frequencies

622.0800	669.1281
625.0000	669.3266
627.3296	672.1600
644.5313	690.5692
666.5143	693.4830

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