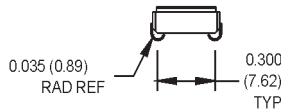
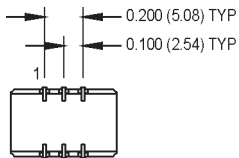
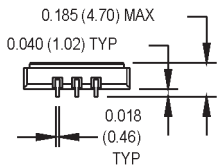
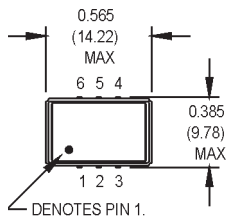


# MPV3J & MPV5J Series

## 9x14 mm, 5.0 or 3.3 Volt, PECL/LVDS, VCXO

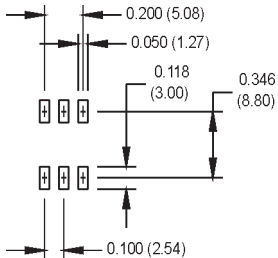


- Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz
- Ideal for low noise PLL applications



All dimensions  
in inches (mm).

### SUGGESTED SOLDER PAD LAYOUT



### Ordering Information

MPV3J/MPV5J	1	0	B	1	P	J	00.0000 MHz
<b>Product Series</b> MPV3J = 3.3 Volt MPV5J = 5.0 Volt							
<b>Temperature Range</b> 1: 0°C to +70°C 6: -20°C to +70°C 2: -40°C to +85°C 8: 0°C to +50°C							
<b>Stability</b> 0: Nominal per APR selection							
<b>Output Type</b> B: Complementary, Enable (Enable High) S: Complementary, Enable (Enable Low) U: Complementary Output							
<b>Absolute Pull Range</b> 1: ±50 ppm (±35 ppm typ. Stability) 8: ±25 ppm (±50 ppm typ. Stability)							
<b>*Symmetry/Output Logic Type</b> P: 45/55% PECL L: 45/55% LVDS Q: 40/60% PECL H: 40/60% LVDS (L and H available with MPV3J only)							
<b>Package/Lead Configurations</b> J: J-lead							
<b>Frequency (customer specified)</b>							

### Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Output Enable or N/C
3	Ground/Case
4	Output Q
5	Output $\bar{Q}$ or N/C
6	+Vcc

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# MPV3J & MPV5J Series

## 9x14 mm, 5.0 or 3.3 Volt, PECL/LVDS, VCXO



Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
	Frequency Range	F	30	800		MHz	(Consult factory for exact frequency availability)
	Frequency Stability	$\Delta F/F$	(See Ordering Information)				See Note 1
	Operating Temperature	T <sub>A</sub>	(See Ordering Information)				
	Storage Temperature	T <sub>S</sub>	-55		+125	°C	
	Input Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	MPV3J
			4.75	5.0	5.25	V	MPV5J
	Input Current	I <sub>dd</sub>		60	70	mA	
	Symmetry (Duty Cycle)		40		60	%	@ V <sub>cc</sub> -1.3 VDC
	(Per Symmetry Code)		45		55	%	
	Load						See Note 2
	Rise/Fall Time	Tr/Tf		.35	.55	ns	@ 20/80%
	Logic “1” Level	V <sub>oh</sub>	V <sub>cc</sub> -1.02			V	PECL
	Logic “0” Level	V <sub>ol</sub>			V <sub>cc</sub> -1.63	V	PECL
	Phase Jitter	φ J					Integrated 12 kHz - 20 MHz
	@ 77.76 MHz			0.6	0.9	ps RMS	
	@ 155.52 MHz			0.3	0.55	ps RMS	
	@ 622.08 MHz			0.25	0.5	ps RMS	
	Phase Noise (Typical)	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	Offset from carrier
	@ 77.76 MHz	-80	-110	-133	-144	-147	dBc/Hz
	@ 155.52 MHz	-80	-110	-133	-144	-147	dBc/Hz
	@ 622.08 MHz	-70	-100	-125	-135	-137	dBc/Hz
	Unwanted Mode Suppression		-50			dB	
	Differential Voltage	V <sub>o</sub>	250	340	450	mV	LVDS
	Modulation Bandwidth	f <sub>m</sub>	10			kHz	-3 dB bandwidth
	Input Impedance	Z <sub>in</sub>	50			KΩ	
	Control Voltage	V <sub>cc</sub>	0	1.65	3.3	V	Pin 1 voltage (MPV3J)
			0		5.0	V	Pin 1 voltage (MPV5J)
	Center Frequency	V <sub>c0</sub>		1.65		V	MPV3J
				2.5		V	MPV5J
	Linearity			5	10	%	
	Pullability	APR	(See Ordering Information)				See Note 3
	Enable/Disable Logic		CMOS high, V <sub>cc</sub> or N/C - enables output				Output Option B
			CMOS low or GND - disables output				
			PECL low, GND, or N/C - enables output				Output Option S
		PECL high - disables output					
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C					
	Vibration	Per MIL-STD-202, Method 201 & 204					
	Reflow Solder Conditions	See “Figure 2” on page 147					
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 <sup>-8</sup> atm.cc/s of helium)					
	Solderability	Per MIL-STD-883, Method 2003					

1. Stability given for deviation over temperature.

2. PECL load - see load circuit diagram #5 on page 149.

3. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.

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